X-X: Single-Crystalline Si TFTs Fabricated with μ-Czochralski (grain-filter) process

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Abstract

This paper reviews an advanced excimer-laser crystallization technique enabling precise location-control of the individual grains. With the developed μ-Czochralski (grain-filter) process, the large grains having a diameter of 6 μm can be set precisely at predetermined positions. We will also discuss the performance of the single-crystalline Si TFTs that are formed within the location-controlled Si grains. The field-effect mobility for electrons is 430 cm^2/Vs on average, which is well comparable to that of TFTs made with silicon-on-insulator wafers.

1. Introduction

Excimer-laser crystallization of a-Si film [1] is a powerful technique to fabricate pixel and driver circuitries for LCDs and OLEDs, since poly-Si TFTs can be formed on glass substrates without thermal damage. The field-effect mobility of the poly-Si TFTs fabricated with conventional excimer-laser crystallization is around 100 cm^2/Vs, which limits the use of the TFTs for the other circuitries, such as DAC and pixel memory. The limitation of the mobility is caused by the fact that the trap states at grain boundaries (GBs) are charged and form potential barriers, which carriers must overcome. The trap states at the GBs also contribute to carrier generation when it is depleted at the off-state near the drain edge. It is experimentally verified [2], by direct comparison between electrical measurement and the number of GBs, that reducing the number of the GBs improves both the field effect mobility and off-current. Lateral grain growth and the formation of the TFT channel parallel to the growth direction [3,4] will be a promising candidate to decrease the total number of the GBs in the TFTs. The improvement of TFT performance, however, will be limited, since the GBs are neither straight nor controlled in their positions, and thus can not be completely eliminated from the TFTs. For the realization of further integration of CPUs and memories, i.e.,``system-on-glass", location-control of the individual grains is necessary so that the TFTs can be formed inside a single grain: single-crystalline-Si (c-Si) TFTs [5]. The technique will also allow the application to the 3D monolithic integration of ICs, as the c-Si TFTs can be stacked upon each other with many levels using low-temperature process. This paper reviews an advanced excimer-laser crystallization technique which enables a precise location-control of the individual large grains and its application to the c-Si TFTs.

2. Location-Control of Grains with Structural Variation by Photolithography

Forming very large grains with an alleviated location control is one way of fabricating the c-Si TFTs. The method, however, wastes a lot of area, since the area outside of the small Si islands of TFTs will be etched away after all. Instead, location control of a large grain will be an attractive approach for fabricating the c-Si TFTs. Here, the grain size needs not to be extremely large, as only the active channel region, including the drain depletion region, in the TFTs should be grain boundary free. If the position of the grains can be controlled very accurately, grain size of 5 μm would be large enough to cover the entire active channel region, considering the minimum feature size (3 μm) and overlay accuracy in the current LCD fabrication process. The minimum required grain size will be reduced with the down scaling of TFTs in LCDs. Furthermore, it will be appreciated for some application if the grains can be set side by side as a regular array.

In crystallization, controlling the positions of the large grains needs both the position control of the crystal seeds and suppression of nucleation outside during the solidification. In pulsed-laser crystallization of Si film, it was suggested [6] that at the beginning of the laser irradiation the film is first converted into fine-grain poly-Si by explosive crystallization. The notion was recently confirmed by combined transient optical reflectivity (TROR) and TEM observation. From this knowledge one can derive a way to control the position of the large Si grains in pulsed-laser crystallization: leaving locally the solid particles (crystal seeds) while completely melting the rest of the area. Indeed, by spatially modifying the incident energy, the position of surviving crystal seeds can be controlled. The shaping of beam intensity can be attained by using, for example, shadowing masks [3] or diffractive phase elements [7]. It should be noted that the accurate location control of single grains is far from straight forward due to the necessity of alignment of the optical image to the lithography image. In contrast, we have carried out local structural and/or material variations of the underlying materials using conventional photolithography. At the early stage, we have demonstrated that the location of the unmelted region can be controlled by the local modification of heat extraction rate towards the substrate [8,9]. The number of large grains can be controlled to unity by making the number of remnant crystal seeds equal to one. The results confirm an advantage of the method that the position of the individual grains can be accurately controlled in 3D. The required number of the laser pulse is one, which is also the advantage in terms of the throughput.

3. μ-Czochralski (Grain-Filter) Process

The μ-Czochralski (grain-filter) process [10] is a promising method among the grain location-control techniques using the structural variations in the substrate by photolithography. The method basically uses two phenomena: the dependence of complete melt threshold on a-Si film thickness [11] and the occlusion of the grains by geometric selection through a constriction. As depicted in Fig. 1, the structure has a locally increased thickness of the a-Si film. The structure is irradiated with excimer-laser light having an energy density above the complete melting threshold of the surrounding thin a-Si film and below that for the thick Si. With this condition, at the end of the laser pulse, a residuary poly-Si, which was formed by the

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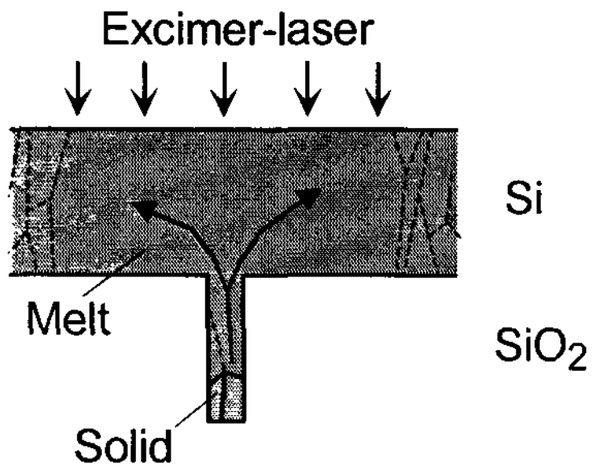

Figure 1. Schematic viewgraph of μ-Czochralski (grain-filter) process

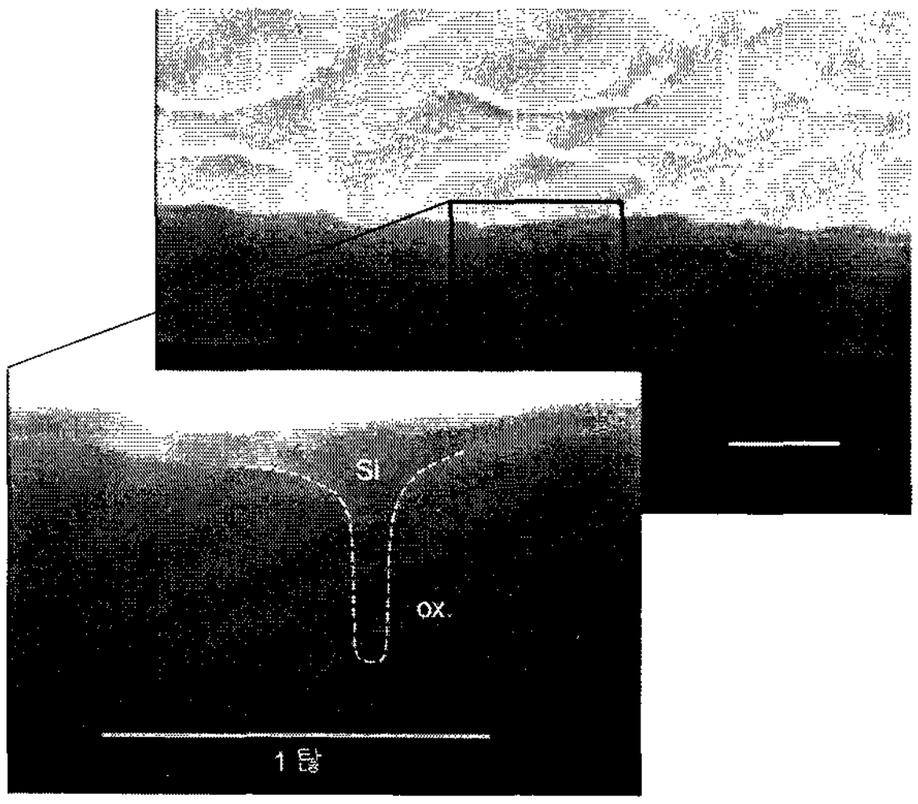

Figure 2. Slant SEM images before (a) and after (b) irradiation of excimer-laser the structure used for the Grain-Filter process.

explosive crystallization, will be left at the bottom of the grain filter. The unmolten Si will subsequently seed the grain growth. Ideally, the diameter of the Si column is sufficiently small so that only one solid-seed will remain. Even if more than one seed remain in the Si column, a single grain is expected to be filtered out during the vertical growth along the Si column (grain-filter), because of the competitive grain growth depending on crystallographic orientation. It should be noted that the maximum energy density will be either the complete melting for the Si column or the agglomeration threshold for the surrounding thin Si film. It is noteworthy that the irradiating energy density can be much higher than the complete melting of the thin Si film, which is normally the limit for a conventional laser crystallization. This allows more heat to be deposited near the substrate surface, which lowers the cooling rate of the melt and thus delays the time for nucleation in the melt. As a result, the lateral growth continues longer before it collides with grains nucleated in the undercooled melt. Experimentally, the narrow hole with a diameter of around 100 nm is formed with two process steps as follows. First, holes having a relatively large diameter varying from 900 to 1050 nm are formed by a conventional i-line photolithography and anisotropic dry etching in 750 nm thick SiO_2 layers deposited on c-Si wafer. Successively 875 nm-thick SiO_2 layer was deposited by TEOS PECVD at a substrate temperature of 350°C. By the conformal deposition of SiO_2, the diameter of the holes is reduced to values varying from 70 to 100 nm, while the depth of the hole was kept at around 1 μm. Then a-Si films with thickness varying from 90 nm to 250 nm were deposited by LPCVD at a temperature of 545°C. The structure filled with 100 nm thick a-Si film is shown in Fig. 3 (a). Finally, a single pulse of XeCl excimer-laser (308nm, 56ns) irradiated the structure with an energy density ranging from 0.6 to 1.5 J/cm^2.

Figure 2(b) shows a slant SEM view after the laser irradiation. The regular array of the circular grains having a diameter of 2.5 μm were grown from the grain filters formed with a spacing of 3 μm. It is noteworthy that, after the laser irradiation, the original indentation of Si formed on top of the grain-filter is planarized by the surface tension driven mass transport of the molten-Si during the solidification. The edge of the grain can be seen as the hillocks.

Figure 3 shows SEM images of the Si film (181 nm) after irradiation of the laser light with various energy densities and defect delineation etching. It can be seen that the number of the grains induced by the grain filter decreased with increasing energy density. This can be explained from the fact that the melt depth in the grain-filter increases as the irradiation energy increases. The longer path of the vertical growth enhances the effect of grain

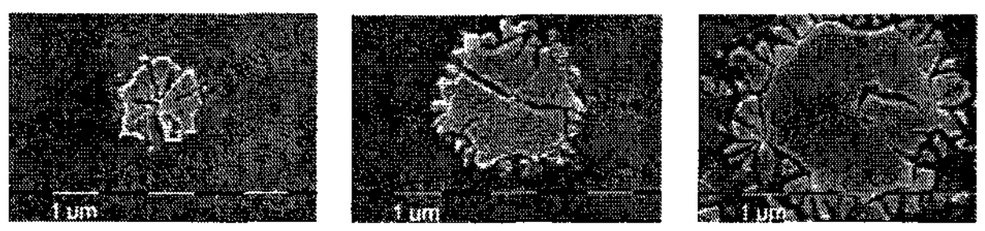

Figure 3. SEM images of the Si film (181 nm) after irradiation of: (a) at 0.64 J/cm^2, (b) at 0.87 J/cm^2, and (c) at 1.13 J/cm^2.

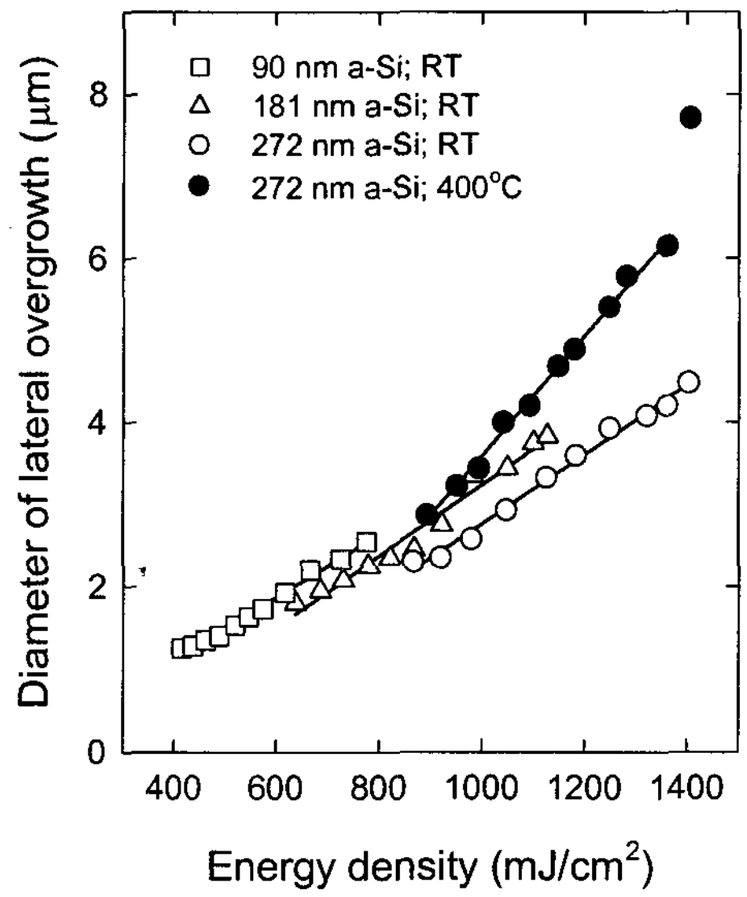

Figure 4. Diameter of grain as a function of energy density for various a-Si thickness and substrate temperatures.

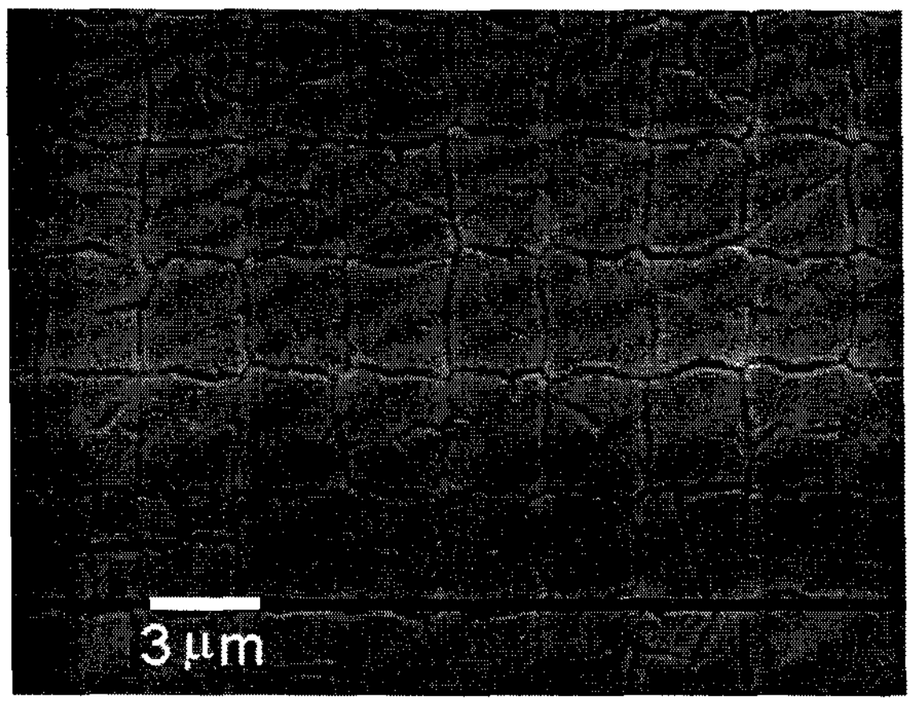

Figure 5. SEM image of the grid of square shaped grains formed by μ-Czochralski (grain-filter) process

occlusion. Furthermore, it can be seen that the lateral overgrowth length increases with increasing the irradiation density, because of the reduced cooling rate in the melt and the resultant delay of the time for the nucleation. Fig. 4 shows the lateral overgrowth length of the grains as a function of irradiation energy density for various film thickness. By increasing the film thickness from 90 nm to 270 nm, the maximum overgrowth length of the location-controlled Si grain was increased from 2.8 μm to 4.5 μm. This is because the agglomeration threshold energy density, which limits the maximum energy density, is increased with the a-Si thickness. It is noteworthy that the location controlled grains can be obtained with an energy density window of as wide as 50% of the maximum energy density. A further increase in grain size was observed for irradiation with 1.40 J/cm^2 to the 272 nm thick film. In this case, as the separation between two holes is small, the lateral diffusion of latent heat released during solidification heats the crystallization front and further suppress the spontaneous nucleation.

A SEM image of a grid of location controlled grains, after defect delineation etching, is shown in Fig. 5. The Si film thickness is 250 nm. Since the spacing between the holes is 3 μm, which is larger than the grain diameter of 6 μm, the grains collide with each other and form a grid of square shaped grains. Some of the grains have the planar defects which are generated either from the center of the film or from the rim of the grain filter. An electron backscatter diffraction (EBSD) analysis of such grains showed that the planer defects generating from the holes are mainly Σ3 twin boundaries, followed by Σ9 and Σ27, which are reported to be electrically less active than the high-angle GBs.[12] The planar defects at the periphery of the grain are found to be low-angle GBs. It was also found that there are no clear preferred surface crystallographic orientations of these grains.

It was found recently that the grains can be enlarged also by elongating the pulse duration of the excimer laser, as it is reported that, during the long pulse duration, more heat can diffuse and accumulate in/near the substrate surface [11]. Using a 225 ns long pulse, a grain size of 6 μm was obtained with the 150 nm thick Si film.

4. Single-Crystalline Si TFTs Inside A Location-Controlled Grain

Single-crystalline Si (c-Si) TFTs were fabricated inside the location controlled grain. In this TFT process, the grain filter structure is planarized by CMP. The deposition of the precursor a-Si film with a thickness of 250 nm was followed by implantation of boron ions with 1x10^{16}cm^{-3} as a channel doping. After formation of the location controlled grains, the Si film was patterned into the active Si islands by dry etching. The channel region was defined so that a grain covers the entire active area. Then, a SiO_2 film with a thickness of 165 nm was deposited by LPCVD at a temperature of 424°C. The gate electrode was then formed with Al and, successively, implantation of phosphorous

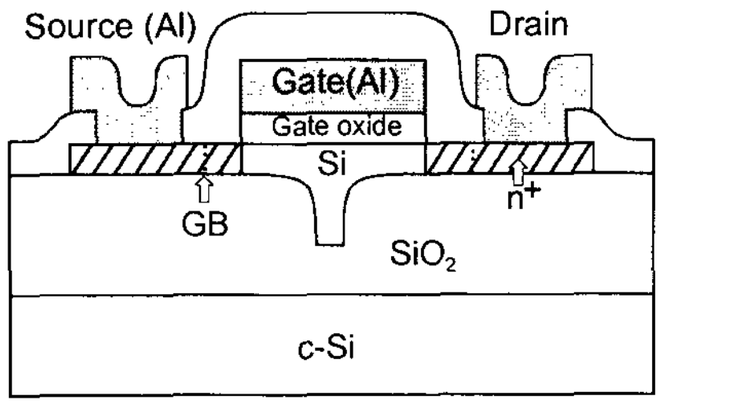

Figure 6. Schematic view of the c-Si TFTs

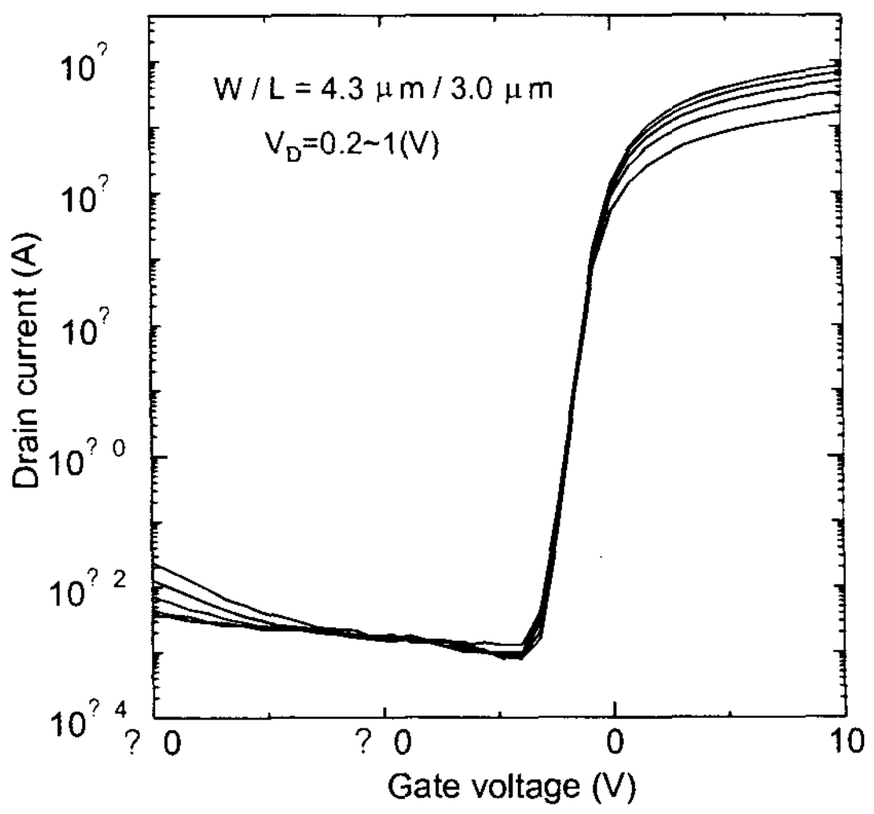

Figure 7. I_D-V_G characteristics of the c-Si TFTs fabricated inside a location-controlled grain

ions (1x10^{16}cm^{-2}) defined source and drain regions with a self-alignment manner. After activation of the implanted atoms by excimer-laser irradiation (300 mJ/cm^2), passivation oxide and the drain and source electrodes were formed. The channel length and width were measured to be 3.0 μm and 4.3 μm, respectively. For reference purpose, TFTs were fabricated also with {100} oriented silicon-on-insulator (SOI) wafers with an identical process as the c-Si TFTs except the thickness of the channel (100nm). The samples were annealed in hydrogen plasma ambient with a substrate temperature of 350°C and a duration of 30 minutes. Figure 7 shows a I_D-V_G characteristics of the c-Si TFT after the hydrogen plasma annealing. The field-effect mobility for electrons

evaluated in a linear regime at a low V_D was as high as 430 cm^2/Vs, which is well comparable to that (590 cm^2/Vs) for the TFTs made with the SOI wafer. This confirms that the Si film of the TFTs has better crystal quality than that of the poly-Si TFTs. A relatively large spread (120 cm^2/Vs) of the field-effect mobility compared to that for the SOI-TFTs, however, could be due to the fact that the surface crystallographic orientation, which determines the effective mass, is random. The spread in the number of the twin defects inside the grain might also be the cause. The subthreshold swing of 0.39 V/dec and the off-current of 0.3pA are higher than that for SOI-TFTs. These suggests that the density of bulk defects, such as point defects and micro-twins, is higher than that of SOI. Passivation of the bulk defects by plasma treatment before the gate oxide formation will effectively improve the both TFT parameters. The subthreshold swing will be further improved by decreasing the thickness of the Si or the gate SiO_2. The other way of improving the subthreshold swing is to employ a gate SiO_2 which has better Si-SiO_2 interface property.

Table 1. Characteristics of the crystal-Si TFTs

	c-Si TFTs	**SOI TFTs**
μ_{FE} (cm^2/Vs)	430±120	590±18
SS (V/dec)	0.39±0.07	0.28±0.03
I_{off} (A)	0.3p±0.1p	0.1p±0.1p
V_{TH} (V)	-0.1±0.33	-3.2±0.5

6. Conclusions

Local structural variations of the substrate using photolithography allow accurate location-control of the large Si grains in excimer-laser crystallization. With μ-Czochralski process, a single grain is filtered out during the vertical regrowth stage and large (6 μm) grains were obtained at a predetermined position. The crystal-silicon TFTs that are formed in the location-controlled Si grains showed a high field-effect mobility for electrons of 430 cm^2/Vs, which is well comparable to that of TFTs made with SOI wafers. This grain location-control technique is suited for implementation in system integration on glass and 3D integration of ICs.

6. Acknowledgements

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