Effect of ramp-type erase pulse waveform on the high Temperature driving characteristics of ac PDP

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Abstract

This paper deals with the effect of ramp-type erase pulse waveform on the high temperature driving characteristics of ac PDP driven by ramp up-down reset waveform. The experimental results show that the discharge characteristics in the reset period are significantly affected by the erase pulse waveform and ambient temperature. The firing voltage is increased with ambient temperature. This can cause misfirings during the sustain period and should be avoided. As one of possible solutions, we propose the optimization of erasing pulse shape.

1. Introduction

The ac Plasma Display Panel (PDP) that utilizes gas discharges is an attractive device for high-definition television (HDTV). Thus, a variety of intensive efforts have been undertaken to improve the luminance, luminous efficiency and image quality of the devices and to lower the cost of ac PDP in order to compete with other technologies.[1-3]

Especially, ac PDP require correct discharge in order to realize good image quality for HDTV. But it is well known that some misfiring of discharge cell in ac PDP occur at low or high temperature. However, few reports discussed this phenomenon. The effects of ramp-type erase pulse waveform on the temperature-dependent driving characteristics of ac PDP are discussed in this paper.[4]

2. Basic Concept of ac PDP

Figure 1 shows the principal structure of a discharge cell in ac PDP. On the front substrate, paired paralleled display electrode Z and scan electrode Y are fabricated. Each electrode is composed of transparent and narrow bus electrodes to emit the luminance effectively. A dielectric layer covers these electrodes, and the MgO protecting layer is prepared on the dielectric layer by E-Beam evaporation method. On the rear substrate, striped address electrodes are arranged. Striped barrier ribs are on both side of the address electrodes to separate the adjacent discharge cells and to eliminate the optical cross-talk between them. Three primary color phosphor material for red, blue, green colors are deposited in the neighboring channels made by the ribs and the dielectric layer. The structure has realized good performances such as a high luminance, a high luminous efficiency and a wide viewing angle. The substrates are assembled each other with about 130μm gap. A Ne-He-Xe gas mixture is introduced between the gaps. The panel structure is the simplest one of conventionally developed color PDPs and the fabrication process is simple enough to mass-produce, so it has advantages such as a low cost process, easiness to manufacture large area panel and high-resolution panels. [1-3]

As a driving method of ac PDP, Address Display Separation (ADS) scheme has been widely used. In ADS method, a picture of one frame is divided into eight sub-fields. Each sub-field has reset, address and sustaining periods as shown in Figure 2. The role of the reset period is to erase the wall charge accumulated on the dielectric surface in previous sub-field, that make a same surface condition before next addressing. The role of addressing period is to make new wall charge on the dielectrics of each discharge cell by applying the addressing pulses between scan and address electrodes. The role of sustaining period is to make an image on the panel by applying the ac sustaining pulses to all display electrodes. In this case, only the selected discharge cells, which have been addressed in the addressing period are turned on. The number of sustaining pulses is decided corresponding to the weight of luminance for each sub-field.[5]

3. Experimental

Table 1 shows the specifications of 7-inch test model ac PDP used in our experiment. The panel has about 14400 cells and XGA resolution.

Figure 2 shows the driving waveform of ADS method used in this study. The total period is 1.63㎳. In the reset period, the ramp rising time is 100μs and the ramp falling time is 150μs. The width of scan pulse is designed as 3μs which is the same pulse width with the conventional 40-inch PDP and total address period is designed as about 1㎳. The width of sustain pulse is designed as 5μs. The rising time of ramp erasing pulse in the sustain period is designed as about 35μs.[5]

Figure 3 shows the schematic diagram of driving circuit to measure the effect of ramp-type erase pulse waveform. We added resistors (R1,R2,R3) connected parallel to a pair of diodes in the driving circuit. Through these resistors, we can measure the discharge current of each electrode. R1, R2 and R3 are 70, 90 and 280ohm, respectively.

4 Results and Discussion

Figure 4 shows the static voltage margin of 7-inch ac PDP as a parameter of temperature. The firing voltages of surface and facing discharge increase with increasing ambient temperature. The total increment of firing voltage is 8V and the rate of increment is 1.6V per 10℃. Figure 5 shows the static voltage margin of non-sealed 7-inch ac PDP as a parameter of temperature. This experiment was performed in the vacuum chamber, which was filled to a given pressure 400Torr at room temperature. As temperature rises to 80C, the pressure increases to 420 Torr. All characteristic voltages increase with ambient temperature. These results agree well with the results obtained from 7" sealed panel

Figure 6 shows the static voltage margin of non-sealed 7-inch ac PDP as a parameter of temperature under constant pressure of 400Torr. In this case, number density of the gas particle varies with temperature. We can clearly see that the firing and sustain voltage remain constant value under constant pressure regardless of the ambient temperature

From the above results, we can forecast the interesting phenomenon that the firing voltage of ac PDP is under the influence of temperature. Moreover, it is impossible to control working pressure of ac PDP after manufacture. The origin of these results is not clear now. However the problem is that these behaviors of voltage characteristics can give bad effects to the driving stability of the panels and can induce temperature-dependent misfiring.

As a first step of characterizing the effect of high ambient temperature on the real driving sequence, we examined current profile during ramp-up part of reset period in ADS scheme. The driving waveform is shown in Figure 2.

Figure 7 shows the current of sustain electrode for two different temperature conditions. Two current profiles correspond to room temperature and elevated temperature (85C) condition respectively. Figure 8 shows the current profiles of address electrode.

As shown in Fig.7 and 8, the discharge current is delayed and the total charge decreases for the high temperature condition. This reflects the increment of firing voltage. The decrease in the amount of charge accumulated on the address can cause addressing failure.

Figure 9 shows the current profiles of sustain electrode in the ramp up voltage region of reset period at the room temperature (23℃) for the different rising time conditions of ramp erasing pulse in the sustain period. The white curve is the discharge current for the rising time of 15μs and the gray is for 35μs. Figure 10 shows the current profiles of address electrode in the ramp up voltage region of reset period. The experiment conditions are the same with above experiment.

From figure 9 and 10, we can see that effective firing voltage decreases when the rising time of erase pulse decreases. This is thought to be due to the fact that the erase pulse having the rising time of 15μs sufficiently removes wall-charges from the each electrode in the sustain period. These results imply that we can compensate the increment of firing voltage and suppress the temperature-dependent misfiring by optimizing the shape of erasing pulse.

5 Conclusion

This paper show that the firing voltage of the plasma display panel increase with ambient temperature and it is quite closely related to the pressure variation. The characteristics of reset discharge in ADS driving scheme are also influenced by temperature. Since the alterations of characteristic voltage can induce some misfirings in ac PDP, it is necessary to develop driving method free from these problems. As one of possible solution, we proposed the optimization of erasing pulse shape.

7. References

[1] Chung-Hoo Park et al, "A Study on the New Type Sustaining Electrode Showing High Luminous Efficiency in AC PDPs" *IEEE Transactions on Electron Devices*, vol. 48, no.10, pp2255-2259, 2001

[2] Sung Hyun Lee et al, "A New Method to Reduce Reset Period in AC Plasma Display Panel", *Trans. KIEE*. vol. 50C, no. 10, pp517-521, October, 2001

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[4] Larry F. Weber, "The Promise of Plasma Display for HDTV". *Information Display (SID)*, vol. 16, no. 12, pp16-20, 2000

[5] C. H. Park et al "Improvement of Addressing Time and its Dispersion in AC Plasma Display Panel", IEEE Transactions on Electron Devices, vol. 48, no.10, pp2260-2265, October 2001.

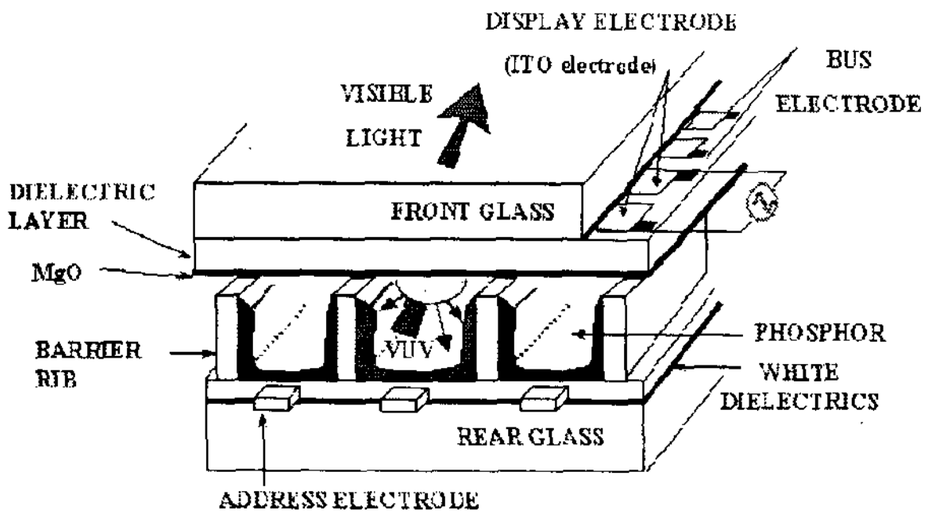

Fig. 1 Principal structure of a discharge cell in ac PDP

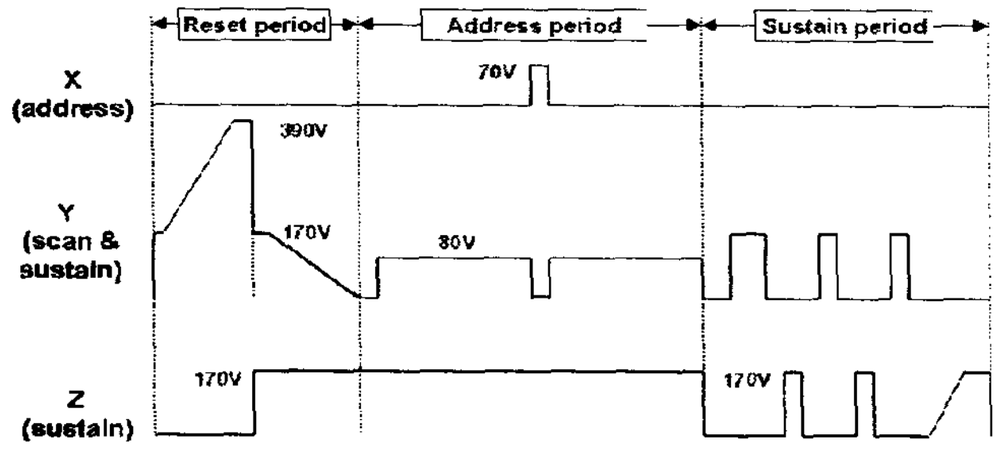

Fig. 2 Schematic diagram of driving waveform

Table 1 Specification of 7-inch ac PDP

Front panel		Rear panel	
ITO width	270㎛	Address electrode width	100㎛
ITO gap	65㎛	White back thickness	15㎛
Bus width	85㎛	Rib height	130㎛
Dielectric thickness	40㎛	Rib pitch	270㎛
MgO thickness	5000Å	Rib width	75㎛
Working gas : Ne+He(9.6%)+Xe(4%)		Phosphor thickness	20㎛
Working gas preasure : 400 Torr			

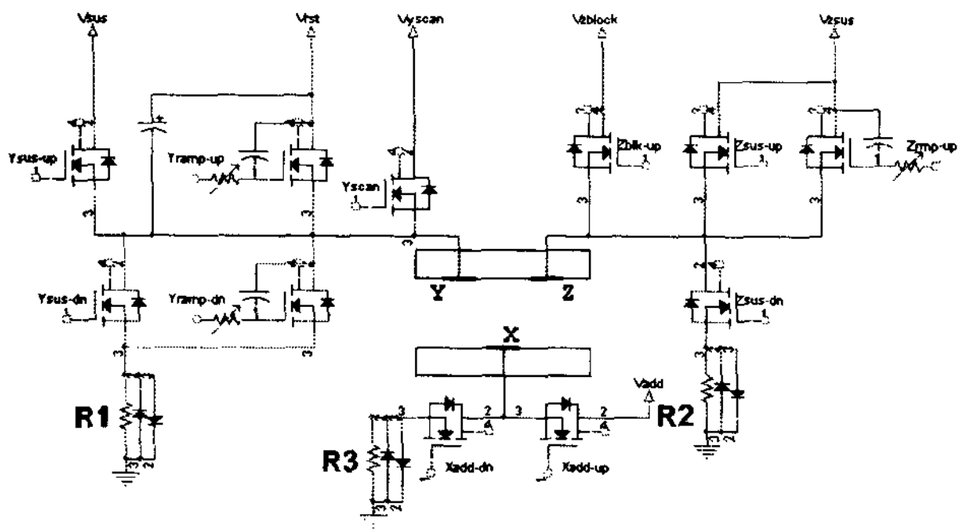

Fig. 3 The schematic diagram of driving circuit to measure the effect of ramp-type erase pulse waveform on the ADS driving method

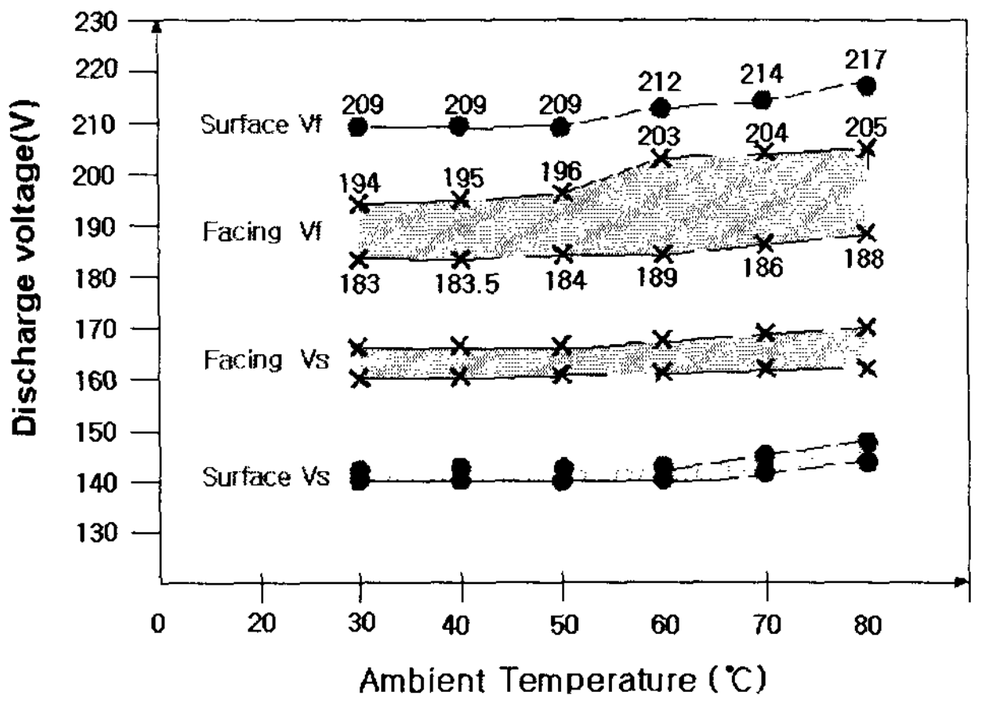

Fig. 4 The static voltage margin of sealed 7-inch ac PDP as a parameter of temperature

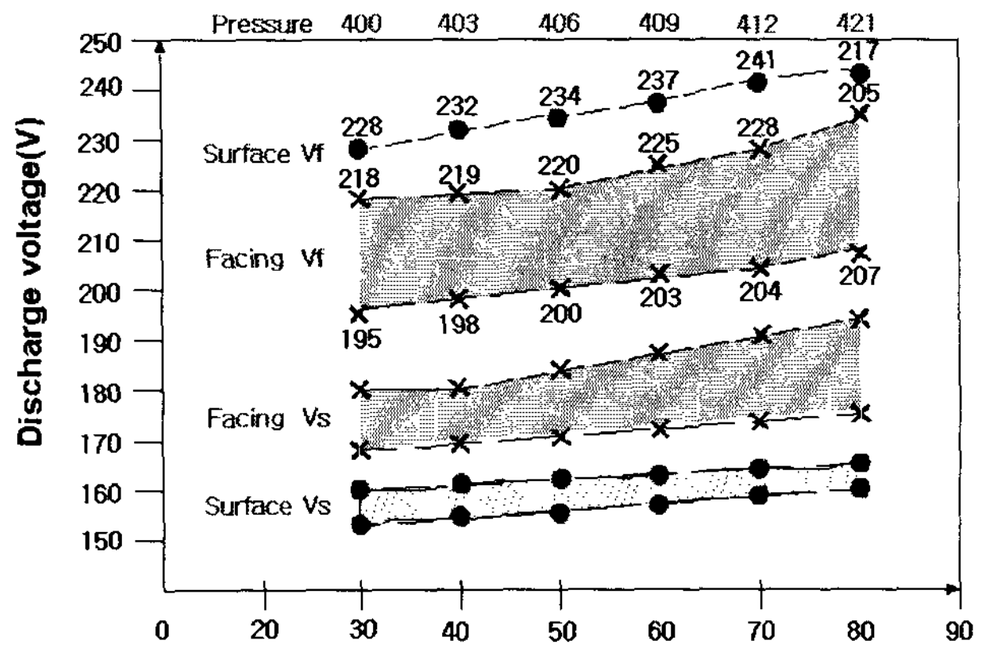

Fig. 5 The static voltage margin of non-sealed 7-inch ac PDP as a parameter of temperature.

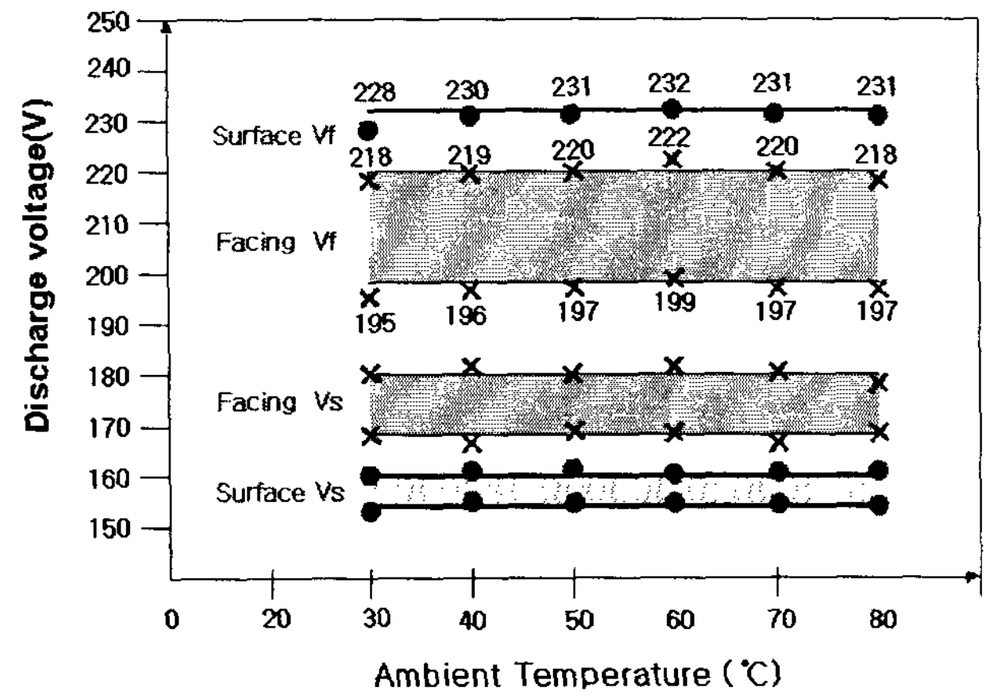

Fig. 6 The static voltage margin of non-sealed 7-inch ac PDP as a parameter of temperature under constant pressure of 400Torr.

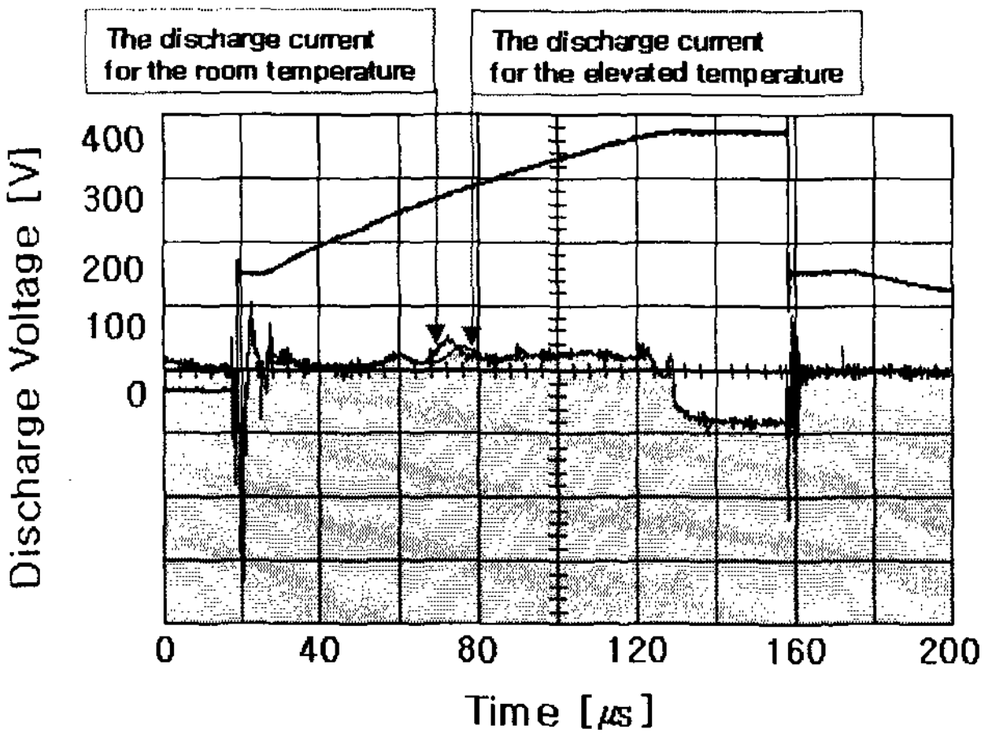

Fig. 7 The currents of sustain electrode at the reset-up region for two different temperature conditions as a parameter of temperature. Gray : room temp(23℃) / White : elevated temp(80℃)

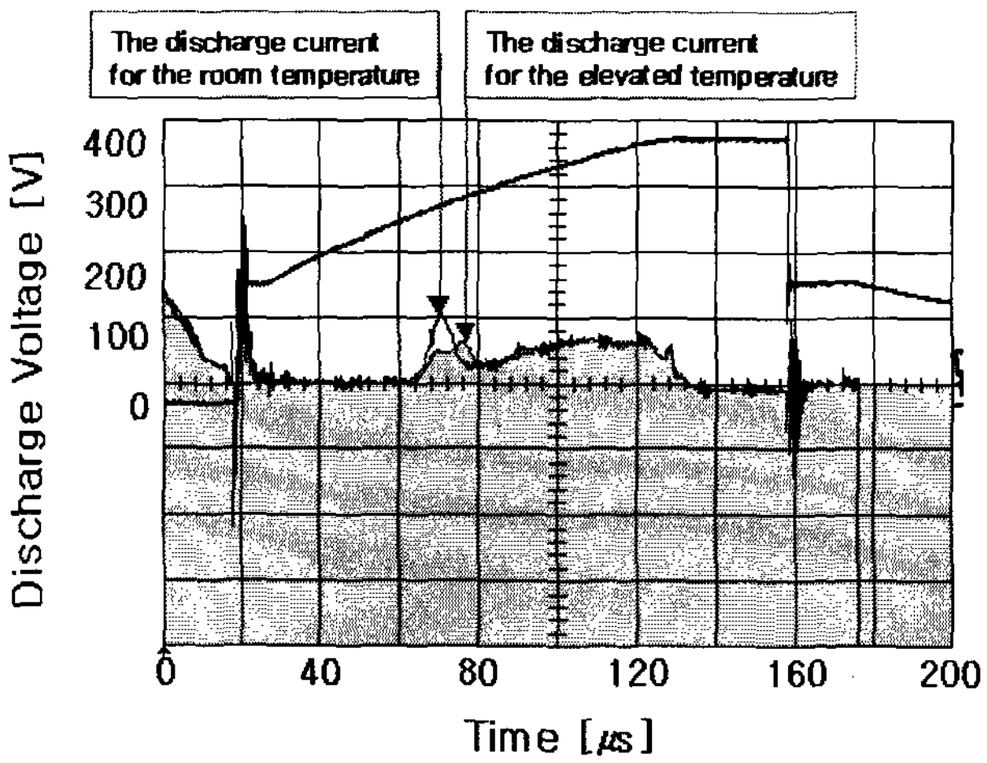

Fig. 8 The currents of address electrode for two different temperature conditions. Gray : room temp.(23℃) / White : elevated temp.(80℃)

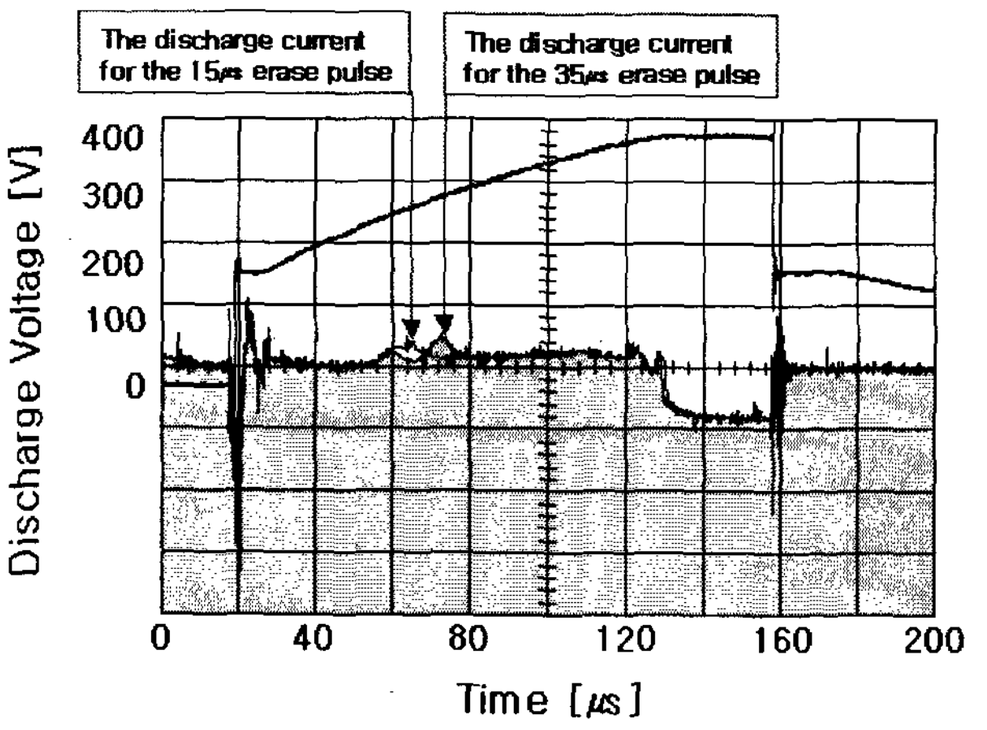

Fig. 9 The current profiles of sustain electrode in the ramp up voltage region of reset period at the room temperature (23℃) for the different rising time conditions of ramp erasing pulse in the sustain period. Gray : the rising time-35μs / White : the rising time-15μs

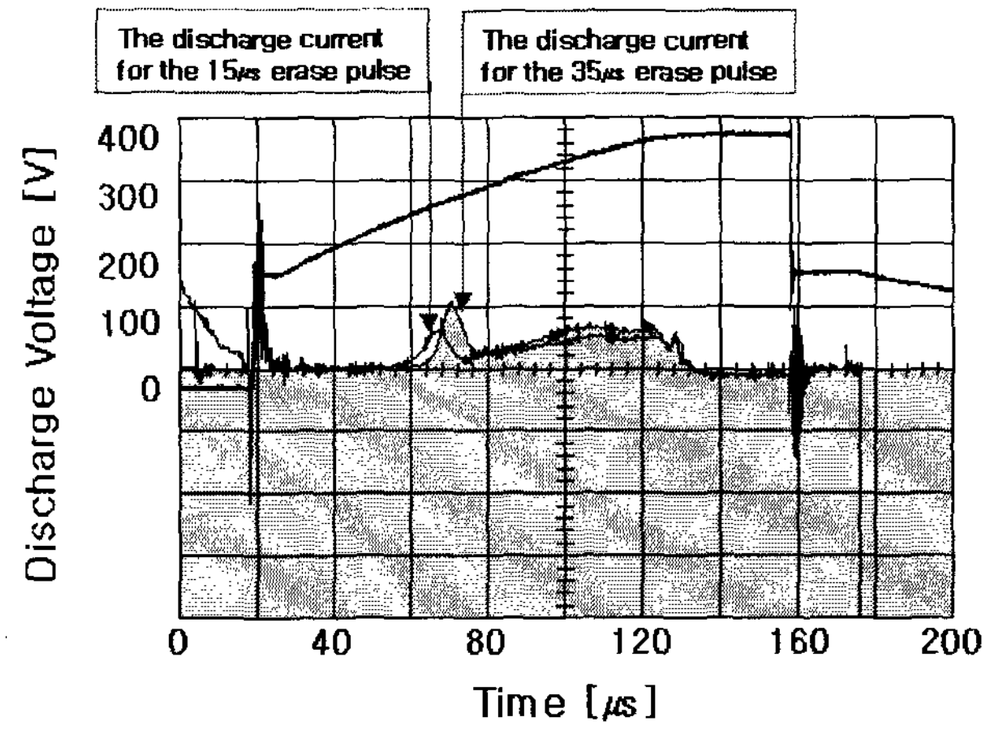

Fig. 10 The current profiles of address electrode in the ramp up voltage region of reset period as the rising time of ramp erasing pulse are 35μs,15μs, respectively. Gray : the rising time-35μs / White : the rising time-15μs