Low Temperature Poly-Si TFT Technology for Small Sized TFT-LCDs

Yong-Min Ha
LG.Philips LCD Co., Ltd.
642-3 Jinpyung-dong, Gumi-city, Kyungbuk 730-726, Korea
e-mail : ymha@lgphilips-lcd.com

Abstract
Small sized LTPS TFT-LCDs are developed and evaluated. Sine the fabrication process is optimized for the productivity of huge glass substrate, the pattern size is above 5㎛. The panels with integrated digital data drivers are not satisfactory to compete with a-Si technology. Therefore, LTPS panels are implemented by PMOS technology and it is proved that they can be competitive with a-Si TFT-LCDs in terms of performance and cost.

1. Introduction

LTPS technology has some potential advantages for small sized AMLCDs in terms of cost and quality. Driving circuit integration on glass substrates makes the modules more compact and cost efficient even with the current LTPS technology. More competitive module can be achieved by integrating more complicate circuitry on the glass in accordance with the improvement of the device performances and the shrinkage of the patterning size and the device feature size in the near future.

However, it dose not seem that the current situation of LTPS technology is so bright because of a few aspects. First, the market volume of small sized AMLCDs is still small to be aggressive in the investment for LTPS business. Second, the LTPS solution of the driver integration should compete with a chip on glass (COG) solution in terms of cost, compactness, and power consumption. Next, the LTPS technology should be improved further more to integrate advanced circuits on the glass. In addition, as the screen size of LTPS TFT-LCDs increases, the cost benefit diminishes since the fabrication process consists of much more steps than a-Si TFT process.

We have suggested one approach to succeed in the LTPS business[1-3]. It is PMOS technology applicable for large sized TFT-LCDs for notebook PCs or monitors. The main feature is to reduce the fabrication cost by simplifying the process, which enables to compete with a-Si TFT-LCDs. However, if the fabrication line is optimized for the high productivity and the low fabrication cost, it would be difficult to produce highly integrated CMOS TFT-LCDs efficiently. In the following sections, our recent achievement and approaches for small sized LTPS TFT-LCDs are discussed.

2. Fabrication process

Both PMOS and CMOS processes have been developed using facilities adequate for large size and PMOS LTPS TFTs. Based on the PMOS process, three doping steps and photo lithography steps are added for the CMOS process. Gate and source metal layers are patterned by wet etch which has been well developed for large sized a-Si TFTs. Interlayer insulators and passivation insulators are also patterned by wet etch instead of dry etch. This approach can be helpful to reduce the fabrication cost gap between LTPS TFTs and a-Si TFTs.

The result of contact hole patterning have showed that the minimum design rule should be larger than 5 ㎛. Even though 4 ㎛ contact holes and metal lines can be formed, the failure rate is too high to be accepted in a mass production line. Therefore, we have designed and fabricated PMOS panels and CMOS panels with 5 ㎛ design rule.

3. CMOS panel implementation

2.2" CMOS LTPS TFT-LCDs are implemented with the integration of driving circuits on the peripheral area of the display. The pixel numbers are 176 X 3 X 220. We have developed three kinds of panels that have different driving schemes. The data driving schemes are very similar to those implemented on silicon ICs for a-Si TFT-LCD panels shown in Fig. 1.

The data driver structure of type I is shown in Fig. 2. It has almost same circuit architecture with conventional silicon driver ICs. It includes level shifters, shift registers, latches, capacitor type DA converters, op-amps, and demultiplexing switches.

One major difference is that one stage of DAC and op-amp covers multiple data lines by demultiplexing analog signals. Otherwise, it is difficult to implement the latch circuits in one pixel pitch with the current patterning size. However, the data driver needs more area than COG a-Si panels. The breadth for the type I data driver is about 8.5 mm, which is 1.5 mm broader than that of COG.

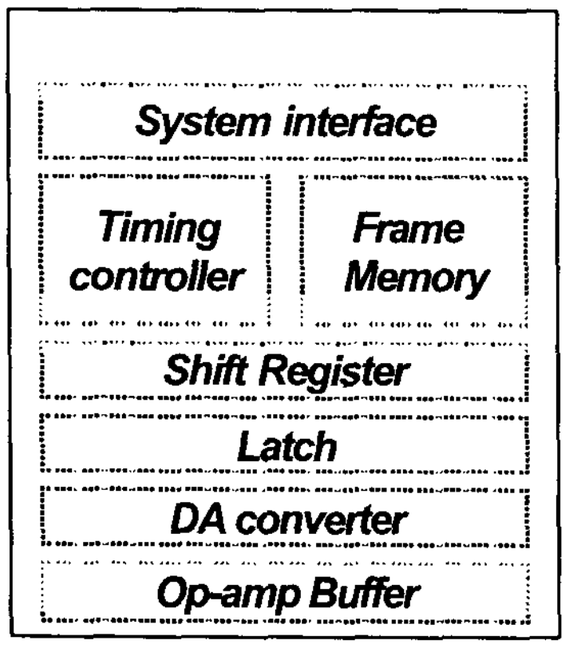

Fig. 1 The schematic diagram of a data driver for a-Si TFT-LCDs.

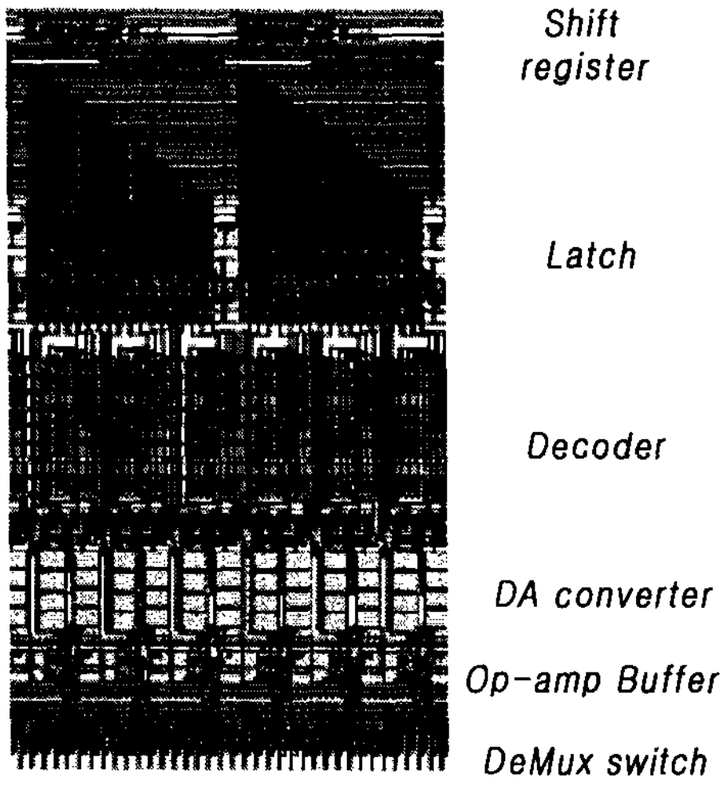

Fig. 2 The layout of a part of the type I data driver.

One of key issues of the type I driver is the accuracy of op-amp output. Since the characteristics of LTPS TFTs are not uniform enough to be used for op-amps in data drivers, vertical stripe dim can be seen on a uniform gray pattern. Therefore, it needs to develop new driving schemes to compensate the non-uniformity of TFTs or to eliminate the op-amps.

So, data drivers that eliminate the op-amps are implemented. Type II data driver has the same structure with that of type I except that it employs resistor(R) type DA converters and it doesn't include op-amp buffers. Since the display size is small and the resolution of the panel is low, it is possible to drive the pixels without op-amp buffers by charging the data lines through the resistor strings in R-type DA converters. Another data driver (type III) is described in Fig. 3. R-type DA converters are located before the shift registers and convert digital input data into analog signals asynchronously. The shift registers select the analog switches sequentially just one time in a horizontal period. By this scheme, the area for the data driver can be reduced more than two other types.

The layout of a part of the type III data driver and the fabricated panel are shown in Fig. 4 and in Fig. 5, respectively. The circuit breadth of the data driver is 7.5 mm. The picture quality, especially, the uniformity of display is better than that of type I.

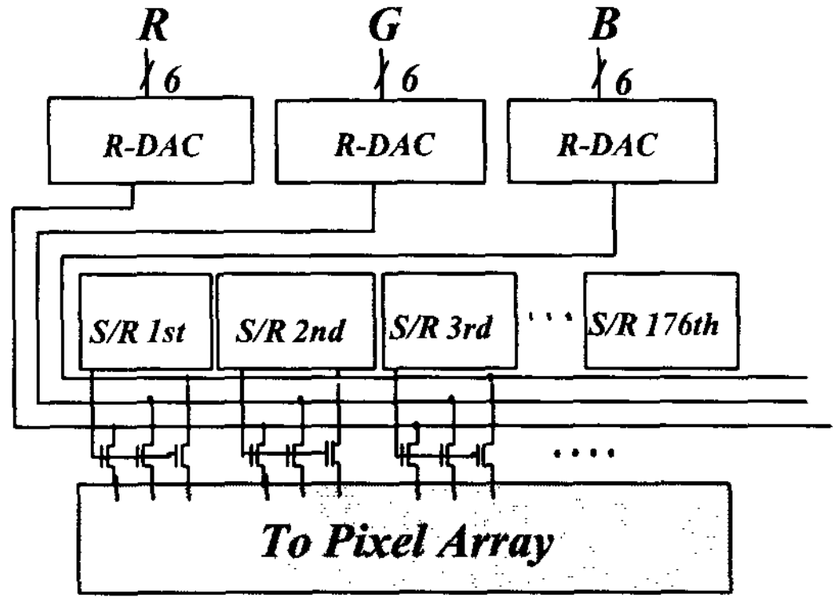

Fig. 3 The block diagram of type III data driver using analog sampling method.

We have implemented and evaluated gate and data driver integrated LTPS panels. However, it is difficult to find better points than a-Si panels in terms of power consumption and compactness. If we optimized panel design, it would be possible to reduce the circuit area and the power consumption furthermore. However, it is considered that the design rule of circuits should be shrunk and the performance of LTPS TFTs should be improved still more to be competitive with a-Si

technology. In addition, more area is needed to integrate complete data drivers for higher resolution panels than mobile phone TFT-LCDs.

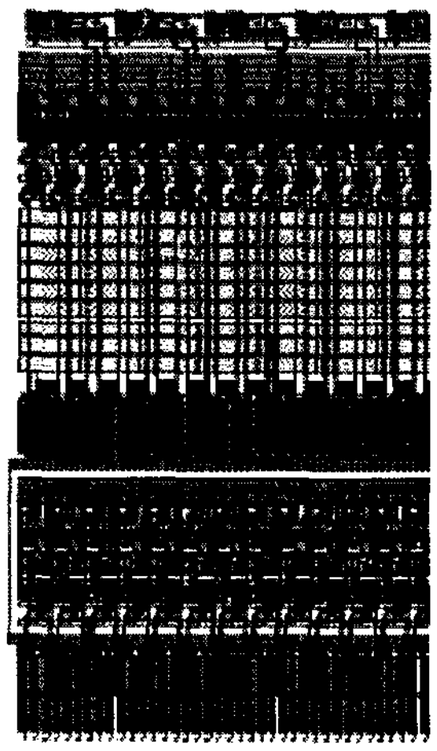

Fig. 4 The layout of a part of the type III data driver.

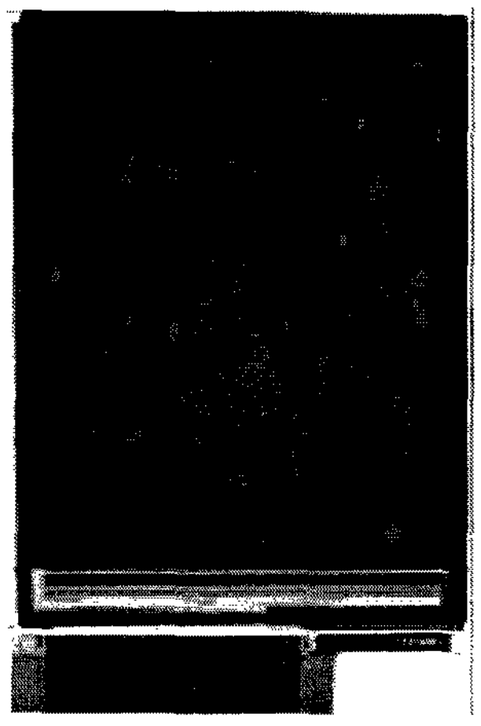

Fig. 5 The display photograph of type III driver integrated panel.

4. PMOS panel implementation

Small sized LTPS TFT-LCD products have been also developed using the PMOS process technology. The block diagram of the module is shown in Fig. 6. Very high pixel density of 4 " VGA (202 PPI) have been implemented. Even though gate driver is fully integrated, only analog sampling switches are integrated for the data driver in order to minimize the peripheral area of the display and the power consumption of the module. Therefore, an external DAC driver IC is needed to make analog signals for the pixels. In addition, another external IC is required to generate clock signals to control the integrated PMOS circuits.

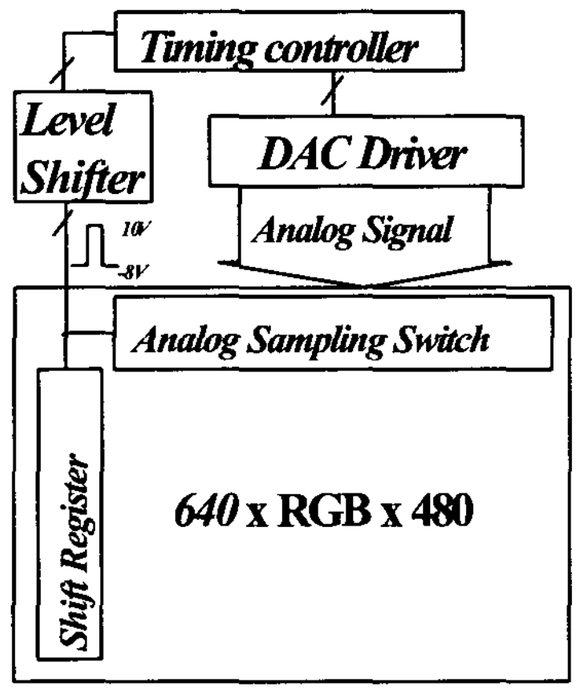

Fig. 6 The structure of PMOS 4" VGA TFT-LCD.

The specifications of the module and the picture of the display are shown in Table 1 and Fig. 6, respectively. Low power consumption has been achieved while maintaining high picture quality by dot inversion method. Another outstanding feature is the narrow and symmetric edge region in the horizontal direction. The 4" modules can be applicable to PDAs.

Table 1 Key characteristics of the module.

Display size	4" (diagonal)
Pixel numbers	640X480
Source driver breadth (Circuit + Seal area + Pads)	6.2 mm
Gate driver breadth (Circuit + Seal area)	3.2 mm
Inversion method	Dot inversion
Display mode	Transflective mode
Power consumption (including DC-DC, w/o BL)	270mW (@ 60 Hz)

In order to make more compact modules, an advanced PMOS module concept has been developed. The block diagram of the module is shown in Fig. 8. Shift registers and level shifters are integrated for both the data driver and the gate driver. The clock signals

coming out from the external level shifter part swing from 0V to 10V and the shift registers generate selection pulses with these signals. Then, the integrated level shifters pull down 0V of the lower level of the selection pulses to −8V. The integration of the shift registers in the data driver makes it possible to reduce the pin number for the interconnection between the panel and the external DAC driver.

Fig. 7 The photograph of 4 " VGA PMOS LTPS TFT-LCD.

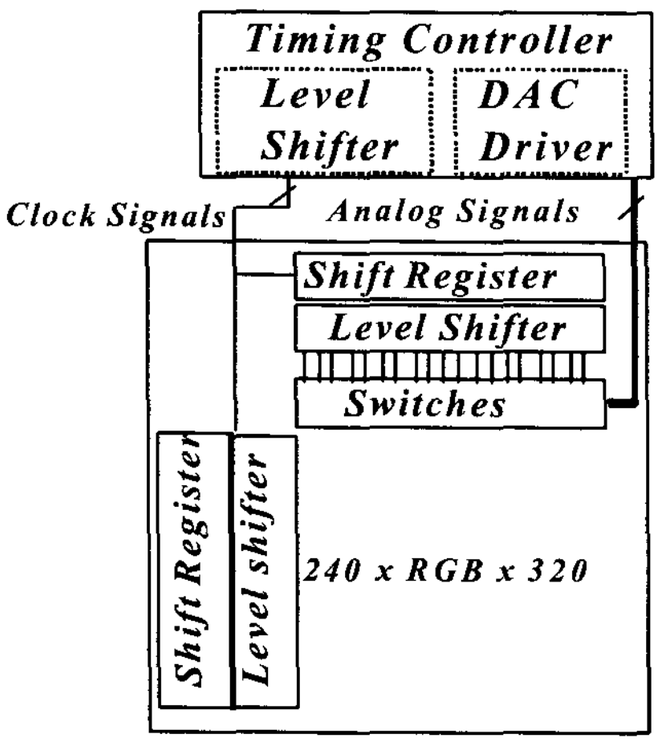

Fig. 8 The block diagram of a module that integrate level shifters on the panel.

Another important merit by the integration of level shifter on the panel is merging the external ICs into one chip. It is difficult to merge the level shifters and the timing controller into one chip in case of the 4 " VGA module since level shifter needs a high voltage process above 20V. Furthermore, additional power consumption can be occurred in pulling down the low level to minus voltage. Eliminating minus voltage in silicon chip helps to reduce the chip size and the power consumption. And also, the power consumed at the clock lines of the panel can be reduced due to the decrease of the pulse swing voltage.

5. Conclusion

We have developed and evaluated several kinds of small sized LTPS TFT-LCDs using a conventional CMOS process and a simplified PMOS process. Even though it has been proved that the picture quality of the CMOS circuit integrated panels are applicable to mobile phone display, it has some limit in the power consumption and the peripheral area if the current fabrication process developed for high productivity are employed. Therefore, we have chosen the approach minimizing the increase of peripheral area and the power consumption resulting from the circuit integration. By transferring the DA converter part into silicon chip, we could develop small sized LTPS TFT-LCDs having low power consumption and compact edge region even with the PMOS technology. In other words, we have developed very competitive PMOS technology for small sized TFT-LCDs in terms of performance and cost. Therefore, it has become possible to produce small and large size panels in a factory with a very cost effective PMOS process.

Acknowledgement

Most of the results mentioned in this paper have been achieved by the P-Si Development team and the PI 1 team in LG.Philips LCD Co., Ltd. The author thanks all the team members.

References

[1] Y. Ha, Y. Jung, B. Kim, K. Kim, J. Kim, S. Yoon, G. Ahn, H. Choi, and H. Soh, "12.1 inch XGA low temperature poly-Si TFT-LCD", Proceeding of the 18th IDRC (ASIA DISPLAY 98). pp. 947 ~ 952.

[2] Y. Ha, " P-type technology for large size low temperature poly-Si TFT-LCDs", SID 2000 Digest, pp. 1116~1119.

[3] B. Kim, K. Kim, K. Ahn, H. Choi, and Y. Ha, " A 14.1 inch UXGA low temperature poly-Si TFT-LCD", Proceedings of the 2th IDMC 2002, pp. 69 ~ 72.