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직렬형 멀티레벨 인버터를 사용한 무효전력보상장치의 수동 파라메타 설계

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Design of Passive Parameters for A Cascade Multilevel Inverter Based Static Var Compensator

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Abstract - This paper examines the application of high voltage static var compensator(SVC) with cascade multilevel inverter which employs H-bridge inverter(HBI). The SVC system is modeled using the d-q transform which calculates the instantaneous reactive power. This model is used to design a controller and analyze the SVC system. From the mathematical model of the system, the design procedures of the circuit parameters L and C are presented in this thesis. To meet the specific total harmonic distortion(THD) and ripple factor of the capacitor voltage, the circuit parameters L and C are designed. Simulated and experimental results are also presented and discussed to validate the proposed schemes.

I. INTRODUCTION

In the large power system network, the active control of reactive power is indispensable to stabilize the power systems and to maintain the supply voltage. A static var compensator(SVC) using the voltage source inve- rters(VSIs) have been widely accepted as the next generation of the reactive power controllers of power system. Several SVCs based on GTOs and a special zig-zag transformer have been developed and put into operation in recent years[1-2]. It has been recognized that these SVCs have advantages over the conventional SVCs of generating less harmonic current to the system and requiring a much smaller reactor. However, zig-zag transformers used in these SVCs are bulky, expensive and unreliable. SVCs based on multilevel voltage source inverter have been widely studied due to its capability of eliminating the zig-zag transformer. In this multilevel VSI based SVC category, there are mainly three different system configurations. They are 1) diode-clamped converter configuration[3-4], 2) flying-capacitor converter configuration[5] and 3) cascading converter configuration[6]. The first and second configurations require a very large number of clamping diodes or flying capacitors, respectively. But the third one has the advantages of using small number of diodes and capacitors. It is constructed by cascading several voltage source H-bridge inverters. Although the above merits, it suffers the disadvantages.[9]

In this paper to solve these problems above, the main objective is to improve the unbalanced DC voltages of the SVC based cascade type multilevel inverter and analyze the performance of the designed prototype. One of the major limitations of the multilevel inverters was the DC voltage unbalancing between each HBI cell. To solve this problem, the novel fundamental rotated switching scheme of fundamental frequency was newly developed. From the model of the system, the design procedures of the circuit parameters L and C are developed. The circuit parameters L and C are designed so as to meet the specific THD and ripple factor of the capacitor voltage(RF). In the simulation and experiment, the proposed SVC system is verified on the transient response such as unit step change, most severe var commend.

II. CONFIGURATION OF POWER CIRCUIT

The simplified block diagram of the SVC system presented in this paper is shown in Fig.1. This system consists of a 7-level inverter, a set of linked reactors and series connected DC capacitors, DSP control board and the ac source mains. In this system, the three phase source volt-ages mean v_{sa}, v_{sb} and v_{sc}, and the three phase currents i_a, i_b and i_c, and the three phase inverter output voltages of SVC, v_{ca}, v_{cb} and v_{cc},, respectively. Fig. 2(a) shows the three phase unit structure of H-bridge inverter(HBI) constructed IGBT devices. It consists ofthe connection diagram for a wye connection 7-level inverter. Fig. 2(b) shows one module(cell) of the H-Bridge inverter with IGBT. Each HBI can generate

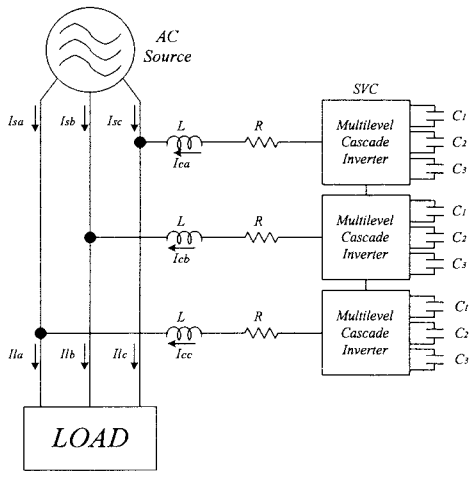

Fig.1. Structure of the SVC with cascade multilevel inverter.

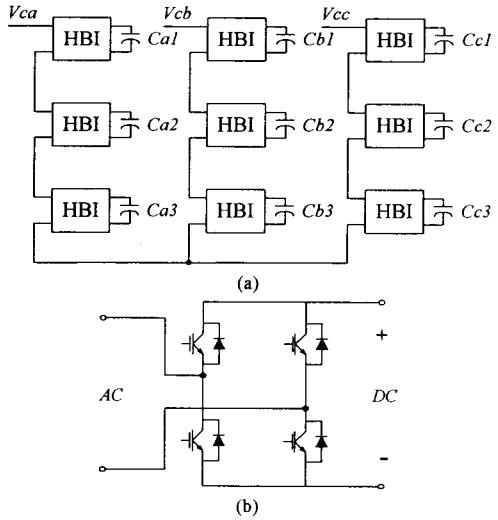

Fig. 2 Three phase cascade multilevel inverter.
(a) Main circuit of cascaded 7-level inverter,
(b) H-bridge inverter(HBI) with IGBT.

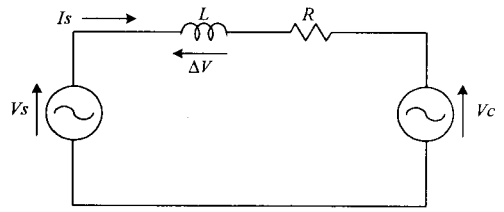

Fig. 3. Single phase equivalent circuit

three level outputs, $+V_{dc}$, 0 and $-V_{dc}$.

The operating principles of the SVC system can be explained by considering the single fundamental equivalent circuit. An equivalent voltage source, V_s is connected to the AC mains through a linked reactor, L and a resistor R representing the total losses in the transmission line, including inverter, as shown in Fig. 3. By controlling the phase angle, α of the inverter output voltage with respect to the phase of source voltage, the DC capacitor voltage V_{dc} can be changed. Thus, the amplitude of the inverter output voltage, V_c can be controlled. Fig. 4(a), (b) and (c) show the phasor diagram for leading(capacitive), zero and lagging (inductive) var generation, respectively. When the inverter output voltage, V_c is higher than the ac system voltage V_s, leading reactive current is drawn from the system(var is generated). When the inverter output voltage V_c is equal to the ac system voltage V_s, reactive power exchange is zero. When the inverter output voltage V_c is lower than the ac system voltage V_s, lagging reactive current is drawn from the system (vars are absorbed). Accordingly, a large amount of reactive power drawn by the SVC can be controlled by adjusting the phase angle α by the small amount. Fig. 5 shows the synthesized phase voltage waveform of a 7-level cascaded inverter with three H-bridge inverters. For each phase of the compensators, the power circuit consists of a cascade multilevel voltage inverter of independent HBI modules.

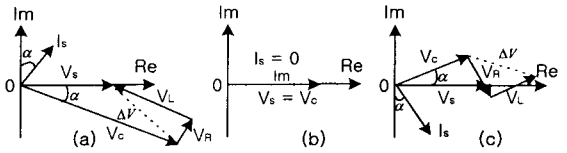

Fig. 4. Phasor diagram of the SVC.
(a) Leading current (b) Zero currnet (c) Lagging current

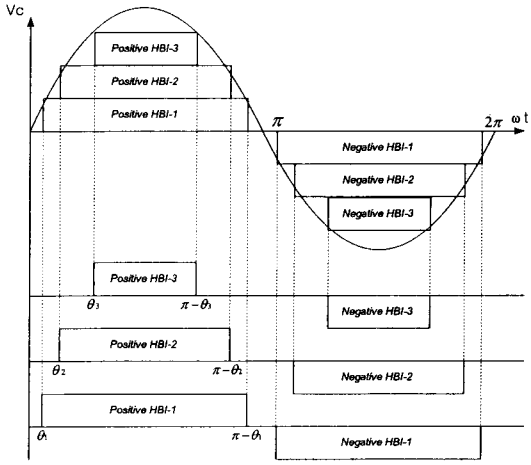

Fig. 5. Waveforms of the 7-level cascade inverter.

III. System Analyses

A. Steady state analysis

Therefore, the real power P and the reactive power Q drawn by the inverter system are expressed as

$$P = V_{sq}I_q + V_{sd}I_d = \frac{V_s^2}{2R}\{1-\cos(2\alpha)\} \quad (1)$$

$$Q = V_{sq}I_d - V_{sd}I_q = \frac{V_s^2}{2R}\sin(2\alpha) \quad (2)$$

Fig. 6 shows the magnitude of P and Q as a function of the specific circuit parameters given in Table 1. The real power P corresponds to the total losses in the inverter. Note that in the range of small α, i.e., $|\alpha| < 5°$, the amount of reactive power is almost proportional to α. In addition, V_{dc}, is dependent on the M of switching pattern and the value of L, but independent of the value of C.

Table.1 Circuit components for parameter design.

Meaning	Symbol	Value
rated power	VA	1[MVA]
rms line to line voltage	V_s	3300[V]
resistance	R	0.5[Ω]
linked reactor	L	5[mH]
dc capacitor	C	2200[μF]
fundamental frequency	f	60[Hz]
Modulation index	M	0.8

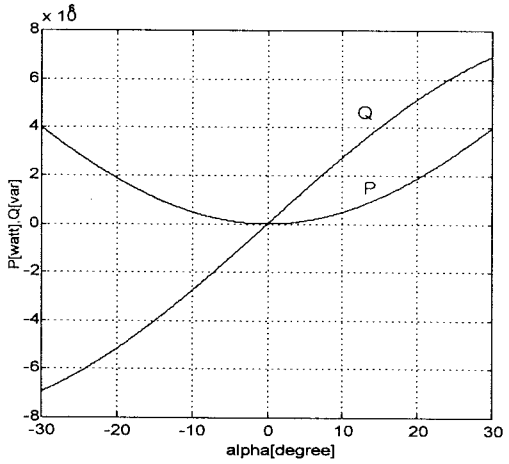

Fig. 6 Plot of Q and P drawn by the cascade inverter vs. α.

Based on the DC analysis, the effective resistance R and the maximum phase difference α_{max} for the rated var can be obtained theoretically.

B. Design of inductance L

The inductance of the reactor L has a major effect on the THD_i of the line current and the maximum value of dc capacitor voltage. THD_i of the line current is one of the important specification. Therefore, the inductance L, is to be designed so as to meet the requirement of the specific THD_i. To solve the THD_i, per phase equivalent circuit is considered under the assumption that R is negligible because it is much smaller than the impedance ωL and DC capacitor voltage V_{dc} is ripple free. The inverter phase voltage(v_{ca}) consists of the fundamental and its harmonic components.

$$v_{ca} = S_a^{12}(\omega t)MV_{dc} = \sqrt{2/3}MV_{dc}\sum_{k=1}^{\infty} m_k \sin(k\omega t + \phi_k) \quad (3)$$

where S_a^{12} is the switching function in a phase and $m_1 = 1$, m_k is the amplitude of k-th harmonic component normalized by the fundamental component. Hence the per-phase equivalent circuit can be separately for fundamental and for k-th harmonics shown in Fig. 7. Therefore, for the rated capacitive var operation, rms value of output voltage of SVC V_c can be written in the following form:

$$V_c = MV_{dc} \quad (4)$$

$$V_{ck} = MV_{dc}m_k \quad (5)$$

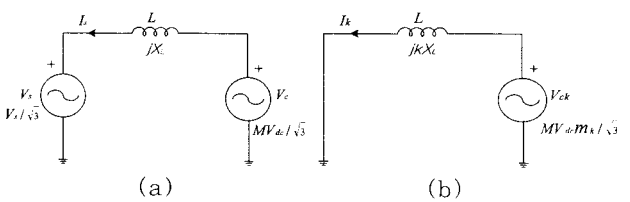

Fig. 7 Per phase equivalent circuit: (a) for fundamental (b) for k-th harmonic component.

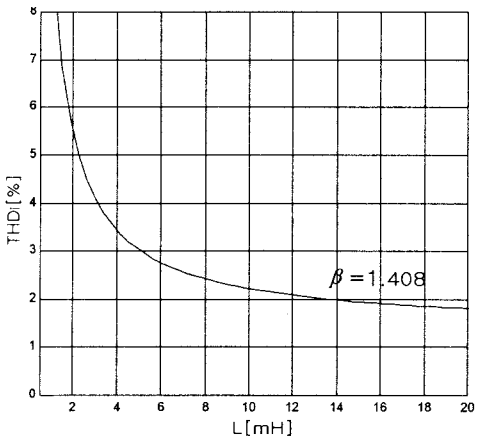

Fig. 8 THDi curve of line current.

The fundamental current component can be expressed by:

$$I_{s1} \cong \frac{|V_{c1} - V_{s1}|}{\omega L} \quad (6)$$

The k-th harmonic current is given by:

$$I_{sk} \cong \frac{V_{ck}}{k\omega L} \quad (7)$$

THDi of the ac line current becomes:

$$\begin{aligned} THD_i &= \frac{\left[\sum_{K=2}^{\infty} I_{sk}^2\right]^{1/2}}{I_s} \\ &= \frac{MV_{dc}\left[\sum_{k=2}^{\infty}\left(\frac{m_k}{k}\right)^2\right]^{1/2}}{|MV_{dc} - V_s|} \\ &= \beta\frac{MV_{dc}/V_s}{MV_{dc}/V_s - 1} \end{aligned} \quad (8)$$

where

$$\beta = \left\{\sum_{k=2}^{\infty}\left[\frac{m_k}{k}\right]^2\right\}^{1/2}$$

From this equation, THD_I curve is shown in Fig. 8 and thus the inductance designed so as to meet the specific THD_I for a β determined by the switching pattern used in inverter.

C. Design of Capacitance C

The capacitance C determines the ripple factor(RF) of the DC capacitor voltage. The RF has an effect on the THD of the line current and thus it is to design in order to satisfy the specific RF. The RF of the capacitor voltage(RF_v) is completely determined by the input DC current i_{dc} for the rated capacitive var operation. Assuming that the three phase line currents are balanced and sinusoidal, i_d can be expressed by:

$$i_{dc} = \sum_{k=1}^{\infty} \sqrt{2} I_{dc,k} \cos(k\omega t + \theta_k) \qquad (9)$$

I_{dck} is the rms value of the k-th harmonic component. By definition, the RF of the voltage V_{dc} is given by:

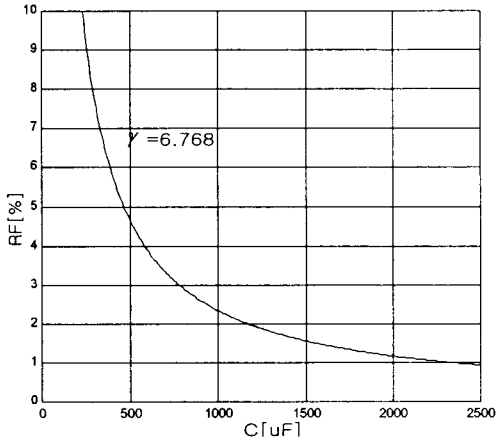

Fig. 9 RFv curve vs. capacitance C.

$$RF_v = \frac{\sum_{k=1}^{\infty}[\ V_{dck}^2]^{1/2}}{V_{dc}} = \frac{\frac{1}{\sqrt{2}\omega C}\sum_{k=1}^{\infty}\left\{\left(\frac{I_{dck}}{k}\right)^2\right\}^{1/2}}{V_{dc}} = \frac{1}{\sqrt{2}\omega C V_{dc}}\sum_{k=1}^{\infty}\left[\left(\frac{I_{dck}}{k}\right)^2\right]^{1/2} = \frac{X_c}{\sqrt{2}\,V_{dc}}\gamma \qquad (10)$$

where $\gamma = \left\{\sum_{k=1}^{\infty}\left[\frac{I_{dck}}{k}\right]^2\right\}^{1/2}$

The factor γ is completely determined by the fundamental switching pattern of the inverter. Fig. 9 shows the RF_v values for the X_c.

Ⅳ. CONTROL STRATEGIES

This means that each switching devices in HBI modules is turned on and off equally. So, the DC voltage of capacitor is balanced in each HBI module.

From the transfer function [7], a controller can be designed in order that the SVC system has fast dynamic characteristics. The SVC system equation (11) is modeled using the d-q transform which calculates the instantaneous reactive power.

$$\frac{\Delta Q}{\Delta \alpha} = C(sI - A)^{-1} = \frac{I(s)}{H(s)} \qquad (11)$$

where $I(s) = V_s^2[\ \frac{s^2}{L} + s\frac{R}{L^2} + \frac{M^2}{L^2 C}]$,

$$H(s) = s^3 + 2\frac{R}{L}s^2 + s(\omega^2 + \frac{R^2}{L^2} + \frac{M^2}{LC}) + \frac{M^2R^2}{L^2C}$$

This model is used to design a control strategy based on the control of the phase angle, α of the fundamental switching pattern also. Fig. 10 shows the control diagram of this system constructed by PI controller. Reactive power feedback using a PI controller makes it possible to improve the transient response of the reactive power. The calculated reactive power Q and reference reactive power Q^* are applied to the PI controller. The output of the PI controller is reference signal representing the phase angle. α The counter produces the phase information, ωt from a signal generated by a phase locked loop(PLL) circuit. The phase comparator compares α

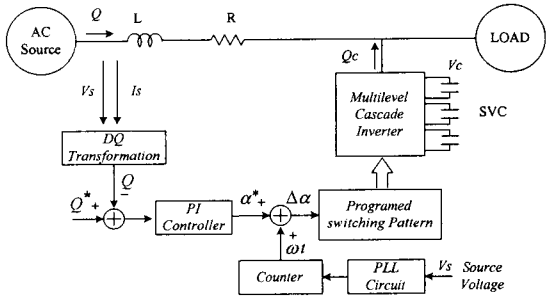

Fig. 10. Block diagram for SVC control.

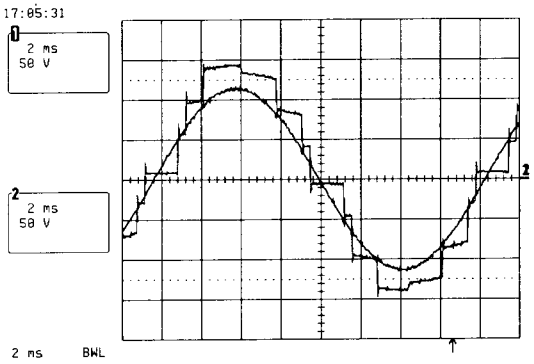

Fig. 11. Source voltage v_{sa} and output voltage v_{ca} of capacitive var generation for Q^* = -0.8[kvar].

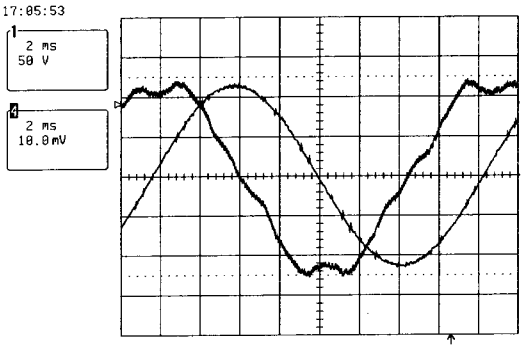

Fig. 12. Source voltage v_{sa} and current i_a of capacitive var generation for Q^* = -0.8[kvar].

with ωt, and determines the times which the corresponding switching devices are turned on and off. Each time the a angle is changed the

DC capacitor voltage keeping a new stable operation voltage. Because the DC voltage changes, the output voltage of cascade multilevel inverter does too, altering its amplitude. The amount of reactive power generatedor absorbed) is basically dependent on the difference of amplitude between the source voltage and output voltage of cascade multilevel inverter.

V. EXPERIMENTAL RESULTS

To confirm the validity of the proposed design methods and

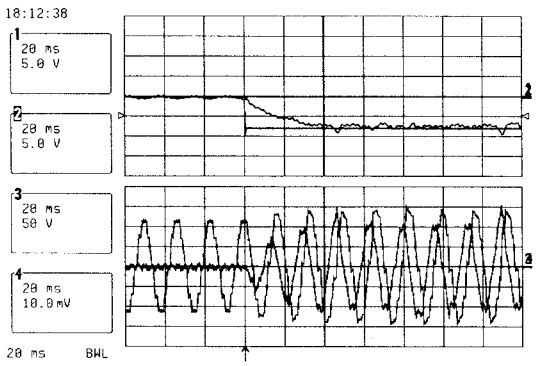

Fig. 13. Transient response for step change of reactive var commend Q^*. (capacitive var generation: from 0 to -0.8kvar)

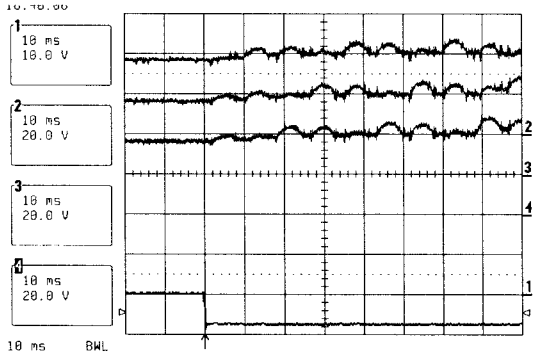

Fig. 14. HBIs DC voltages for step change of reactive var commend Q^*.(capacitive var generation : from 0 to -0.8kvar)

scheme, an experimental 5kVA prototype is implemented and tested also. This system consists of a 7-level inverter, a set of linked reactors and series connected DC capacitors, DSP control board (TMS320C31) and the ac source mains. This SVC system is constructed with the values given as follows: rms line to line voltage V_s=130[V], frequency f=60[Hz], other system parameters L=5[mH], R=0.2[Ω], C=2200[uF]. Fig. 11 plots the ac source voltage v_{sa} of phase A and the inverter output voltage v_{ca} of phase A. Fig. 12 is presented in the ac source voltage of phase A and the ac line current i_a, respectively. When var commend is changed from 0 to -0.8kvar, Fig.13is plotted in the transient state result for capacitive var generation. Fig.13 is shown in the var commend reactive var Q, the phase output voltage v_{sa} and ac line current i_a. Fig. 14 is plotted in the var commend Q^* and the separate DC capacitor voltages of each HBI module. Fig. 15 is show in the harmonic spectrums of current in capacitive var generation. A THD of current is 4.3[%], which is satisfied with the design value below 5[%].

VI. CONCLUSION

This paper presents the high power application of SVC system using cascade multi-level inverter. From the mathematical model of the system, the design procedures of the circuit parameters L and C is pre-

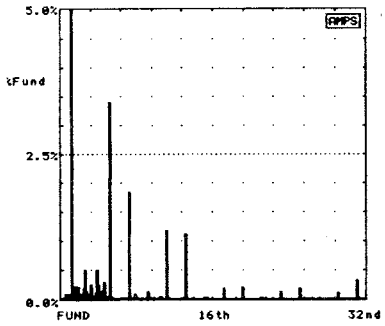

Fig. 15. Harmonic spectrums of current in capacitive var generation.

sented. From the simulated and experimental results, the circuit parameters L and C is designed so as to meet the line current THD and ripple factor of the capacitor voltage. In the experiment, the SVC system is verified on the transient response such as unit step change, most severe var commend. This cascade multilevel inverter is also suited for transformer-less high power application such as FACTS.

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