EFFECTS OF PROCESS INDUCED DEFECTS
ON THERMAL PERFORMANCE OF FLIP CHIP PACKAGE

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ABSTRACT

Heat is always the root of stress acting upon the electronic package, regardless of the heat due to the device itself during operation or working under the adverse environment. Due to the significant mismatch in coefficient of thermal expansion (CTE) and the thermal conductivity (K) of the packaging components, on one hand intensive research has been conducted in order to enhance the device reliability by minimizing the mechanical stressing and deformation within the package. On the other hand the effectiveness of different thermal enhancements are pursued to dissipate the heat to avoid the overheating of the device. However, the interactions between the thermal-mechanical loading has not yet been address fully, in articular when the temperature gradient is considered within the package. To address the interactions between the thermal loading upon the mechanical stressing condition, coupled-field analysis is performed to account the interaction between the thermal and mechanical stress distribution. Furthermore, process induced defects are also incorporated into the analysis to determine the effects on thermal conducting path as well as the mechanical stress distribution. It is concluded that it feasible to consider the thermal gradient within the package accompanied with the mechanical analysis, and the subsequent effects of the inherent defects on the overall structural integrity of the package are discussed.

1. Introduction

Heat is an unavoidable by-product of every electronic device and circuit, and is normally detrimental to the device's performance and reliability if the ability of the package in dissipating the heat is unsatisfactory. Under the high silicon integration level and elevated clock speeds, but smaller package size, the design of thermal management of the package is further challenging. Definitely the incorporation of heat sink accompanied with

forced air condition is desirable to dissipate the majority of heat through the package/die top surface. Yet, the space to accommodate the heat sinks or fans is not always available, like the read/write pre-amplifiers in a hard disk drive [1], and it is important to identify the available thermal paths of the package like in this case to lower the device temperature.

To meet the high I/O and miniaturization era, flip chip package provides a viable solution to the needs. In comparisons with the PQFP and BGA packages, the majority of heat from the chip is dissipated to the PCB board under nature convection and no heat sink condition, as summarized in Table 1 [2]. It can be noticed that the typical thermal paths within a flip chip package include die/solder bumps/board (26.1%), die/underfill/board (72.4%) and die top/ambient (1.5%), in which the percentage of heat getting through from the die have been included [3]. It worths to note that the majority of the heat is conducted through the underfill to the PCB board for heat dissipation under nature convection and no heat sink condition [2-3].

Table 1. Heat paths of various packages

Package Type	Heat to board	Heat via pkg top
PQFP	80 – 95%	5 – 20%
BGA	80 – 97%	3 – 20%
Flip Chip	95%	5%

Even though flip chip package provides the lowest junction-to-board thermal resistant (θ_{jb}), in fact it is typically less than 5% of the junction-to-ambient thermal resistant (θ_{ja}), and the board-to-ambient thermal resistant (θ_{ba}) is the governing factor. The junction-to-ambient thermal resistant (θ_{ja}) is defined as follows:

$$\theta_{ja} = \theta_{jb} + \theta_{ba} \tag{1}$$

where $\theta_{jb} = (T_j - T_b)/q$ and $\theta_{ba} = (T_b - T_a)/q$, T_j, T_b, and T_a are the junction, board and ambient temperature respectively, and q is the power of the component. It is observed that even with an underfill having higher thermal conductivity [4], full array bumping compared with peripheral array [5], or bump voids [4], all have insignificant effects on the junction-to-ambient thermal resistant (θ_{ja}). In brief, the impact of the underfill properties on the thermal performance of basic FCOB is minute [1-6]. Modification should be focused on the board level. Table 2 compares the improvement on θ_{ja} by different thermal enhancements on the boards [1].

Nevertheless, the underfill material is still the primary conductive heat path from the device junction to the PCB board for heat dissipation. Table 3 shows that the presence of underfill in FCOB minimized 30% of the total thermal resistance when compared with the case without, and both the θ_{jb} and θ_{ba} were reduced [4]. However, voids are often presence owing to solvent evaporation/outgassing or incomplete underfilling. Delamination is also encountered under thermal cycling or humidity aging environment. Voids are responsible for weak adhesion, die lifting, increased thermal resistance, and poor power-cycling performance. A relatively large contiguous void create a large temperature gradient in the silicon since the heat must flow around the void, and the thermal

performance of the device is reduced due to the temperature gradient [7]. It has been reported that up to 16.5% increase in θ_{ja} when air gap was presence in the underfill layer [1].

Table 2. Effects of thermal enhancement on junction-to-ambient thermal resistant.

Thermal Enhancement	Power, W	θ_{ja}, C/W	Improvement, %
FCOB	0.6	173.8	-
FCOB & Al stiffener	0.6	122.2	29.7
FCOB, thermal via & Al stiffener	0.6	117.7	32.3
FCOB, Cu plate on top	0.6	168.1	3.3

Table 3. Thermal resistances of FCOB with different underfills.

	θ_{ja} (°C/W)	θ_{jb} (°C/W)	θ_{ba} (°C/W)
FCOB without underfill (air = 0.026W/mk)	39	5.9	33.1
FCOB with underfill 1 (= 0.5W/mk)	27	1.3	25.7
FCOB with underfill 2 (= 2.5W/mk)	25.5	0.8	23.7

As a continuation of our previous study on process induced defect analysis on flip chip package, the objective of this study is two-fold. Firstly it is observed that even though the underfill properties is insignificant to the package thermal resistant (θ_{ja}), the defects (or delaminations) inside the underfill layer deteriorate the heat dissipation of the package via the PCB board, and thus increase the junction-to-ambient thermal resistant. The effects of size of the delamination on the package thermal resistant were therefore studied. On the other hand, it is also of interest to study the stress fields within the package under various defects as mentioned under the elevated junction/package temperature.

2. Numerical Modeling

A commercial finite element code ANSYS was employed throughout the study. The present numerical model contained five bumps with $120\mu m$ standoff height, as schematically drawn in Figure 1. It was assumed that the active die surface at 105°C was the merely heat source within the package, and the boundary of the package was at the same temperature as the environment, which was 45°C. Coupled field analysis was employed in order to account the interaction between the thermal and mechanical stress distribution. The material properties of silicon die and FR-4 substrate at different temperatures are summarized in Table 4.

The Young's modulus of 63Sn/37Pb solder is given by:

$$E(T) = 32000 - 88T \text{ (MPa)} \qquad (2)$$

where T is temperature in °C, and the CTE (α) was 21ppm/°C.

The underfill was considered as thermo-elastic material as shown in Figure 2. The CTE values below (α_1) and

above (α_2) the glass transition temperature ($T_g = 140°C$) determined by using a thermo-mechanical analyzer were 40ppm/°C and 114ppm/°C, respectively.
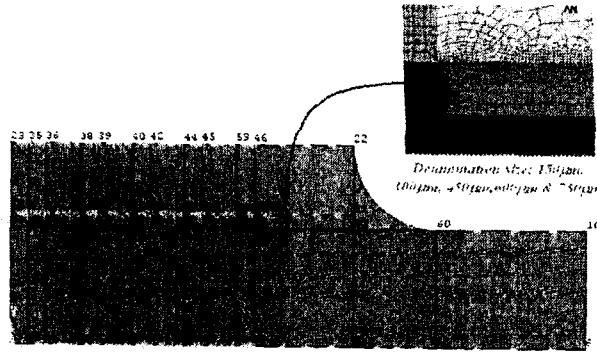

Figure 1. Schematic drawing of the flip chip model.

The thermal conductivities (K) of the package components are also summarized in Table 5, which shows the significant mismatches in their values. Considerable temperature gradient within the package can be expected.

Table 4. Material properties of silicon chip and FR-4 substrate

(Die- E=148GPa; $\mu \approx 0.25$; α=2.5ppm/°C for all temperature; FR-4 substrate)

Temperature (°C)	30	95	125	150
E_1(GPa)	22.4	20.7	19.3	17.9
E_2(GPa)	1.6	1.2	1.0	0.6
E_3(GPa)	22.4	20.7	19.3	17.9
G_{12}(GPa)	0.2	0.19	0.16	0.14
G_{13}(GPa)	0.63	0.60	0.5	0.45
G_{23}(GPa)	0.2	0.19	0.16	0.14
ν_{12}	0.14	0.14	0.14	0.14
ν_{32}	0.14	0.14	0.14	0.14
ν_{13}	0.002	0.002	0.002	0.002
α_1(ppm/°C)	20	20	20	20
α_2(ppm/°C)	86.5	86.5	400	400
α_3(ppm/°C)	20	20	20	20

Table 5. Thermal conductivities of package components within the flip chip.

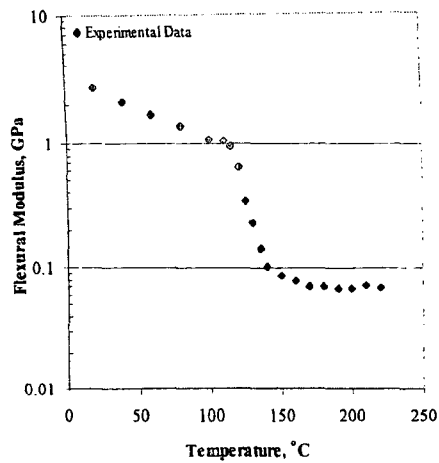| Material	K (W/m °C)
Silicon	120
Printed Circuit Board (FR-4)	0.30
Eutectic solder bump (63Sn/37Pb)	50.60
Polymeric underfill	0.60
Air	0.0314

Figure 2. Variation of flexural modulus of underfill against temperature.

3. Results and Discussions

Figure 3 illustrates the differences between uniform temperature analysis and coupled-field analysis incorporating temperature gradient consideration; in von Mises stress distribution within the package. Although at present there is little experimental works to address the thermal-mechanical interaction in packaging industry, it is reasonable to believe that the coupled-field analysis with the temperature gradient consideration inside is a better-of-fact analysis. Moreover, it can be noticed that the stress distribution within the package showed more detail stress profiles in the coupled-field analysis, which was likely the actual in-situ situation of the components under the operating environment.
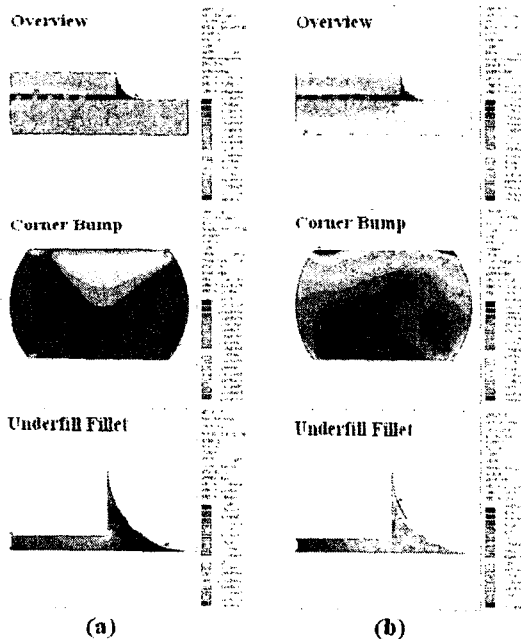

(a)   (b)

Figure 3. von Mises stress analysis: (a) Uniform temperature distribution (45°C→105°C); and (b) Coupled field analysis incorporating temperature gradient within the components

In the presence of delamination near the die edge, the temperature distribution within the package is illustrated in Figure 4 under different delamination size. It is noticed that the thermal distribution around the delamination region varied with the corresponding size. Definitely, due to the poor thermal conductivity of air, heat was unable to dissipate via the original path. It is also of interest to note the corresponding effects on the stress distribution, as shown in Figure 5.
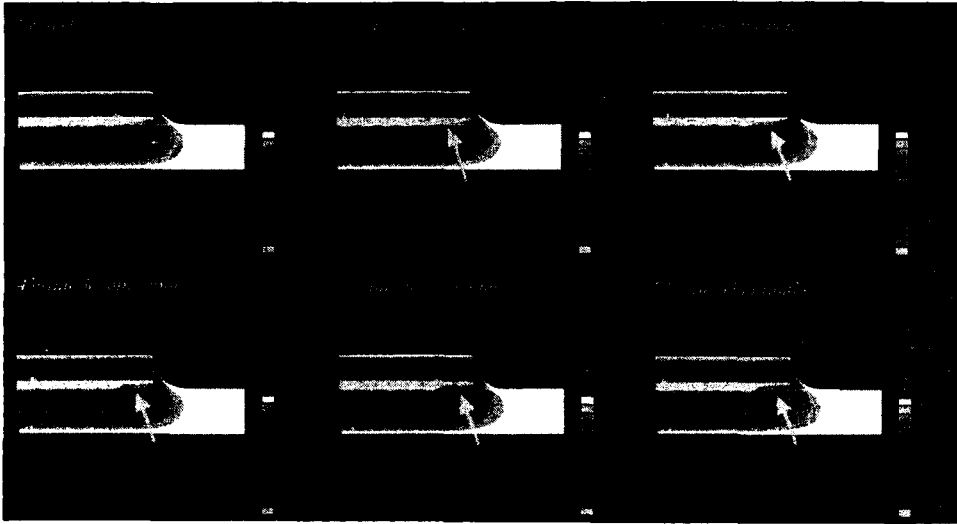

Figure 4. Temperature distribution within the package with different delamination size under operation.
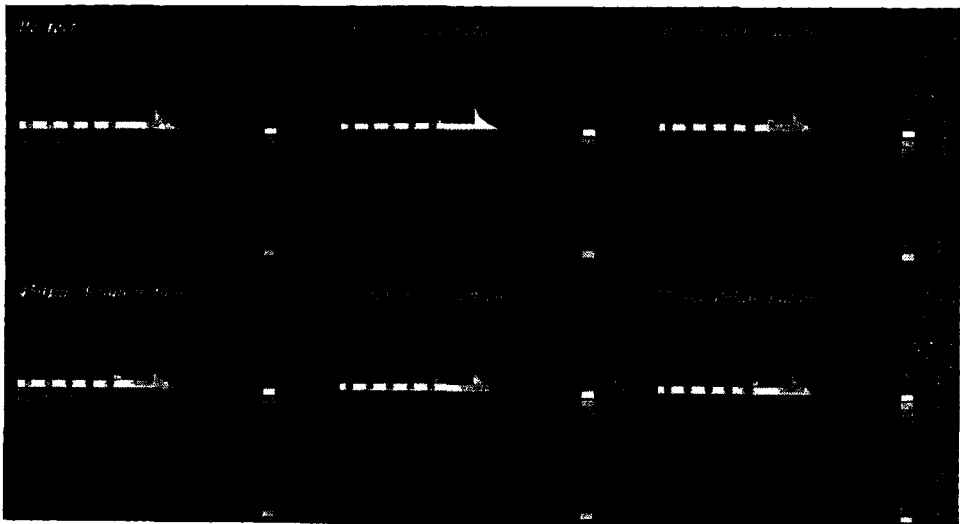

Figure 5. von Mises stress distribution within the package with different delamination size under operation.

As seen in Figure 5, the stress distribution within the package was severely alternated. Accordingly it is important to have more study on the stressing conditions of the solder joint as well as the underfill layer. It is noted that the stress distribution within most of the solder joints were similar with respect to the delamination size, except the corner bump as highlighted in Figure 6. Progressive stress growth was observed with the delmination size, especially along the die interface, and it seems likely that the corner bump lost the strengthening supports due to the delamination near the corner bump. It also worths to mention that the present stress calculation was not only based on the dimensional mismatches amongst the components during heating,

but also the temperature gradient within the entire package as illustrated previously in Figure 4. This approach has promoted the plausible speculation that the multi-physics analysis is necessary as demonstrated in this case with the thermal-mechanical interaction, especially in the case of electronic packaging having different components with great mismatches in thermal conductivities.
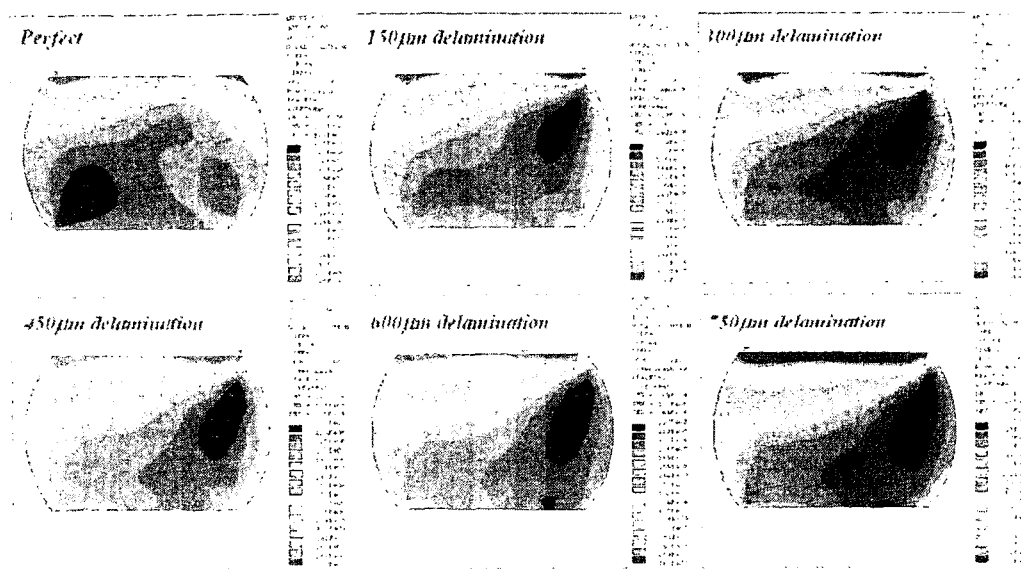

Figure 6. von Mises stress distribution within the corner bump.

The stress distribution within the underfill is illustrated in Figure 7. It is noted that the distribution was also altered with the size of delamination, and the maximum stress shifted from the fillet tip under the perfect condition, to the solder bump corner, and finally to the tip of the delamination. Assuming that the underfill material was isotropic, this result suggests that the failure would initiate at different location depending on the delamination size.
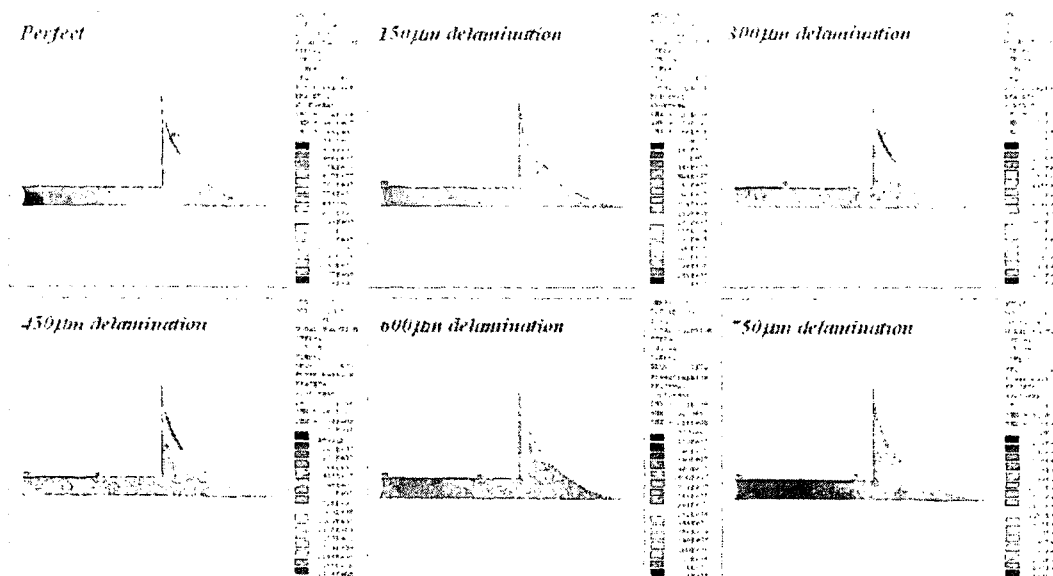

Figure 7. von Mises stress distribution with the underfill fillet.

The shear stress is plotted along the die and substrate interfaces with the underfill. By analogy to many other studies, the stress at the solder joint corners along the die surface was always higher than the stress along the substrate surface. It is also noticed that the effects owing to the delamination size is negligible within the solder joints along both interfaces, even though the progressive growth of the stress inside the corner bump was previously noted. The shear stress at the die-underfill interface was elevated around the delamination tip region, while the shear stress along the substrate surface was fluctuated slightly.
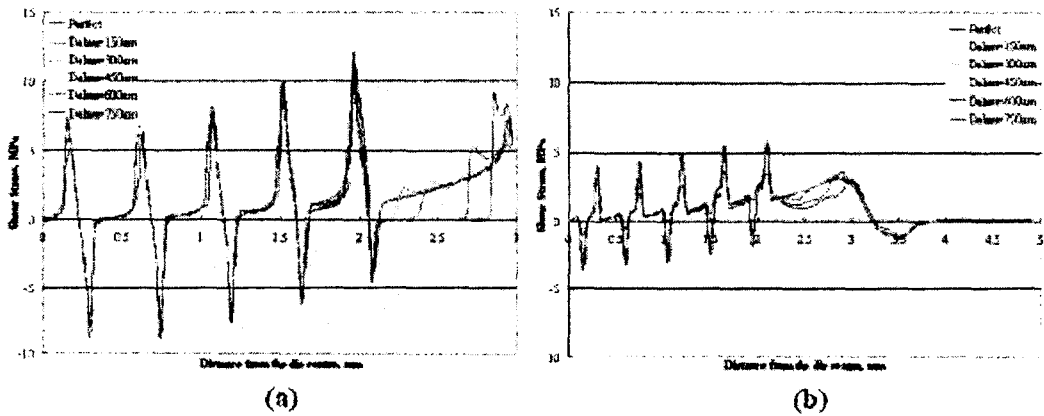

Figure 8. Shear stress profiles along: (a) die-underfill interface; and (b) substrate-underfill interface.

4. Concluding Remarks

In many previous numerical analyses on electronic packaging, the interaction between the thermal-mechanical has not been examined in detail, in particular in the presence of defects. This study demonstrated the feasibility in considering the thermal gradient within the package in analyzing the mechanical stressing conditions within the flip chip package. With the delamination defects not only the overall structural integrity was weakened, but also the thermal distribution was altered. Hence there is an important aspect of considering coupled field analysis in the electronic packaging modeling. Based on the above discussions the following remarks are made:

1. Under the normal operating conditions, dramatic stress variation was observed within the package containing different delamination sizes.
2. Maximum stress level within the underfill near the fillet shifted with the delamination size.
3. The stress within the corner solder bump showed the progressive change with the neighborhood delamination size, even though the stress along the die and substrate surface were almost the same regardless of the delamination size.

References

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