Next Generation Electronic Packaging and Bumpless Interconnection

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Introduction

The rapid advance in high speed and high performance electronic system has led to growth of the system scale and increase in chip size. However, with increase in system scale, we are confronted with severe problems. That are the increase in the number of the multi-level wiring, which will become 9 to 10 layers in 2011, and the delay in signal transmission in global wiring on chip due to the LC coupling effect, which determines the system performance. The SOC might be one of the promising solutions, which is the trend most Japanese semiconductor manufacturers are following. However, the incompatibility of the fabrication process gives us fear for drastic increase in cost for fabrication and delay in turnaround time.

These bottleneck could be solved by the system in package, SiP, if a concurrent and seamless design among chip, package and the system becomes possible. However, such a system LSI in a SiP can be realized only by enabling high speed singnal transmission between chips in a package, and therefore ultrahigh density and fine pitch interconnections of the same level of on-chip interconnection.

However, there is a gap in design rule of interconnections between on-chip wiring and the packaging interconnection: a gap around 1 to 10 micron pitch between them to which the current technology is not capable to reach. In order to preserve the signal integrity and high IO speed in such a system, a new approach is required to incorporate a transmission line structure into the interconnect board, and to make a drastic shrinkage in design rule of the wiring and bonding. The purpose of the present study is to propose a new structure for the next generation interconnect which is expected to overcome the technology gap of interconnection.

Bump-less Interconnect

Figure 1 shows the proposed high density integrated system using the bump-less interconnect concept, where different types of devices, which are fabricated in separated wafers by different processes, and are made extremely thin, are bonded directly on to a global interconnect board composed of transmission line structure as a thin module.

The module should be extremely thin, for example, less than 100 μm in total thickness, then such module could be stacked further as a 3-D module.

The bump-less interconnect means that two structures composed of interconnections and insulating layers are bonded directly without bump-like electrode. The layer structures represent either conbinations of chip on substrate, chip on chip, or wiring layer on active devices. In particular, separation of the global wiring layer from active device layer might improve the yield of the multi-layer interconnection of a system LSI. Also an improvement in signal transmission rate can be expected by incorporating adequate transmission line structure into the substrate and shortening interconnection between devices. Such ultra-fine pitch interconnect may allow to interconnect two different devices, such as analog, RF, digital, or even MEMS devices in a vertical direction.

Surface Activated Bonding (SAB)

Bump-less interconnect of a micron range can not be realized by the conventional bonding technology such as soldering or thermal compresson bonding using high temperature difusion accompanied by formation of intermetallic compounds at the bonded interface.

The surface activated bonding (SAB) method seems the most atractive and promising technique, since all the process for bonding is carried out at a room temperature or lower temperature than those for the conventional bonding methods.

The idea of SAB is based on the fact that two atomically clean solid surfaces under contact develop an extremely strong adhesive force. The clean surfaces can be obtained by dry process such as ion beam bombardment or hydrogen radical irradiation. The bonding is achieved only by contact at a room temperature. Chemical bonds that are established by the

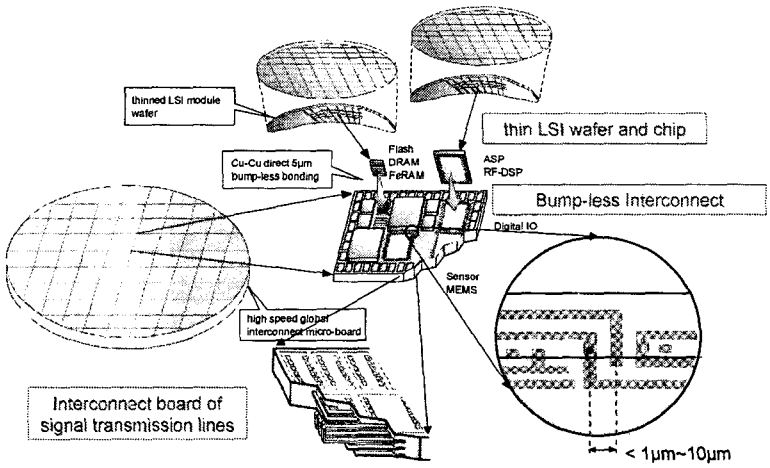

Figure 1. the proposed high density integrated system using the bump-less interconnect concept

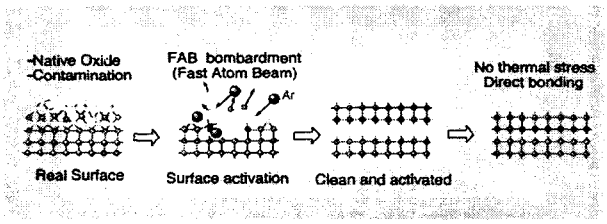

Figure 2. Concept of surface activated bonding

charge transfer across the interfaces between metals and non-metallic materials have been analyzed by means of calculations of the electronic structure of the metal-to-ceramic interfaces. So far, SAB method has been investigated on various metals such as Al, Cu, Ag, Au, Sn, In, Ti, Ni and their alloys, the combinations to ceramics or semiconductor such as SiC, Si_3N_4, Al_2O_3, AlN, diamond and silicon as well as heterojunctions such as Si-GaAs, Si-InP, and GaAs-InP [1](Fig.3-Fig.4).

The bond strength of the most bonded pairs is generally determined by the strength of the weaker part of the joint constituent materials.

Toyokohan Ltd. has adopted the SAB method on their cold rolling process for fabrication of metal laminates, and put it into mass-production of a part for the pressure-safety valve of Li-secondary battery composed of an Al-Al laminate. Also a new fabrication process for high density build-up substrate has been patented using bumping technique of the metal laminates fabricated by SAB method (Fig.5).

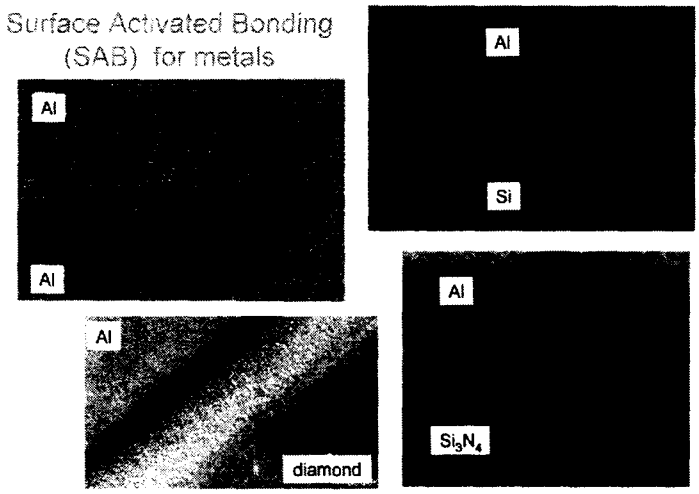

Figure 3. Bonded interfaces of various Al joints fabricated by SAB method.

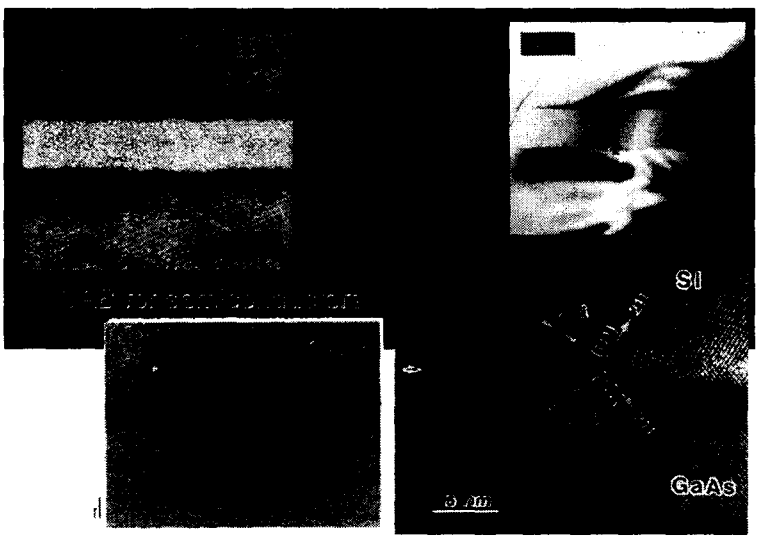

Figure 4. Bonded interfaces of various semiconductors wafer bonding fabricated by SAB method.

Bump-less interconnect using SAB

To investigate the feasibility of the SAB technique in bump-less interconnect, two series of experiments have been conducted.

One is a bonding experiment on usual bump bonding. A Si chip with Au electroplated bumps of 40μm square is bonded directly to another Si substrate with Au, Al or Cu electrodes. The purpose of the experiment was mainly to confirm the possibility of the bonding among these metals, and to investigate the optimum condition for the SAB. It is worthy noting that the bonding is possible even after exposure of the surfaces to the atmosphere. Of course, it must depend on the concentration of residual gases, the oxidation rate of metals, and material combinations. At least, Au and Au are bonded successfully without any difficulty in atmospheric pressure of N_2 or Ar, whereas Cu loses the surface activity slowly, and Al extremely fast, so that Al can be bonded only in vacuum. Some further results have been reported elswhere, showing that Au-Au could be bonded even in Air and we have developed a new flip chip bonder combined by the SAB process. The bonder has a very high accuracy for alignment of chip and substrate better than 0.3 μm, and the room temperature or low temperature flip chip bonding is achieved for Au bump to Au or Cu electrode by means of the surface activation treatment using RF plasma irradiation (Fig. 6). [2-3].

The other experiment is to investigate Cu-Cu direct bonding and its application on bump-less bonding (Figure 7).

The outline of manufacturing process and the detail of the sizes of test vehicle are shown in Fig. 8 (a), (b). First, SiN insulator layer is developed on Si chip after the deposition of barrier metal and the patterning of Cu lower wiring layer. Then

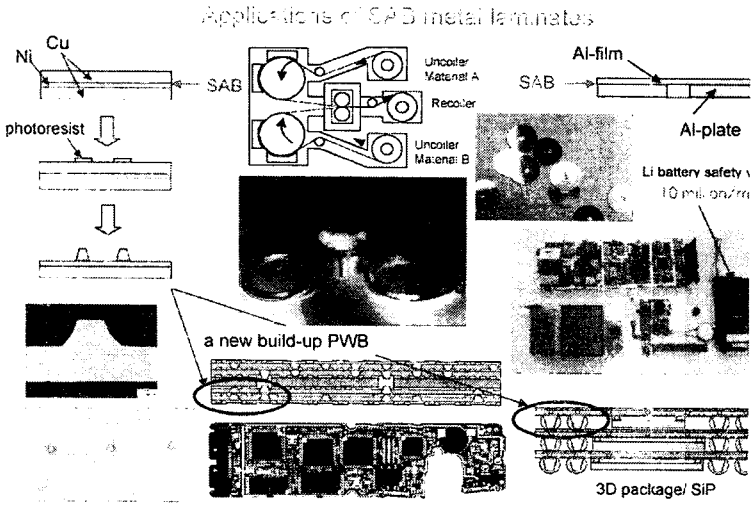

Figure 5. Applications of metal laminates fabricated by SAB method.

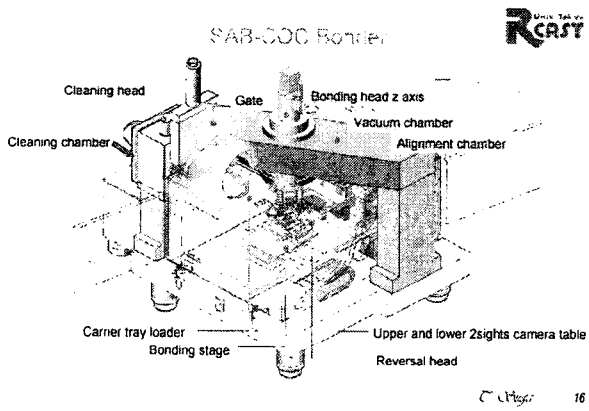

Figure6. high acurate SAB-COC flip chip bonder

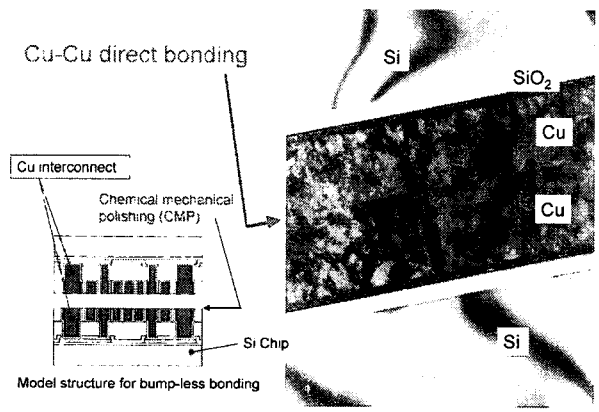

Figure 7. A test vehicle for bump-less interconnect showing the Cu-Cu direct bonding at room temperature.

SiN layer is patterned to fabricate octagonal thorough-hole for bump-less electrode. Then electroplated Cu fills octagonal holes of different sizes of 3~30 μm with the pitches of 10 ~ 100 μm. The surface of Cu thick film is polished back by CMP to expose insulator layer and the electrode surfaces on the same plane. However, since dishing phenomena on Cu surface is evident, the SiN surface is again patterned and slightly etched off to make Cu upheaval to assure the contact between electrodes. After that the surface of electrode is flattened by CMP again. Finally the height of the electrodes is controlled to be several ten nm as indicated in AFM image, which is low enough to maintain the bump-less characteristic. The electrodes whose sizes are 8~30μm forms chain pattern including 1000 connections inside it. The connections are divided equally into 4 areas for resistance measurement. The electrodes of 3μm consist of 100,000 connections divided into each 1000 connections. They were introduced into bonder apparatus and bonded in the vacuum condition of 0.02 Pa□s and the contact load of 50 kgf.

As a result, all electrodes in 20 and 30μm patterns in $(6.4x3.4)mm^2$ are successfully interconnected. Fig. 9 implies the SEM images of debonded interface of 20μm pattern and the results of contact resistance measurement. Although slight misalignment is observed on debonded surface, the bonded area of the interface fails in the state of exfoliation of Cu electrodes, indicating high bonding strength. The resistance of one connection calculated simply from total chain resistance is about 0.1Ω at both pattern. This value seems to be high. However, it is considered that the resistance of wires and pads is dominant in these pattern since the resistance increases in proportion to the numbers of connections. Therefore the contact resistance could be estimated as about 0.12 Ω. Thus real contact resistance of one connection was measured by 4-wire method (3 terminals) at each size of electrodes. The resistance is about 3mΩ at 10μm electrode, 1 mΩ at 20μm electrode and 0.8mΩ at 30μm electrode on average. .

Conclusion

Concurrent and seamless design for chip, package, and the system will become possible only in the interconnect of on-chip, in-package, and bonding between chip and substrate.

Bump-less interconnect could build a bridge over the technology gap in the design rule of interconnections. Bonding at 1 million pins of 1 micron size is a real challenge, and it could be possible if the nature of the solid surfaces is observed and certainly utilized. Thus the surface activation is a new but a quite logical consequence of the demand of the modern high reliable and high density interconnection.

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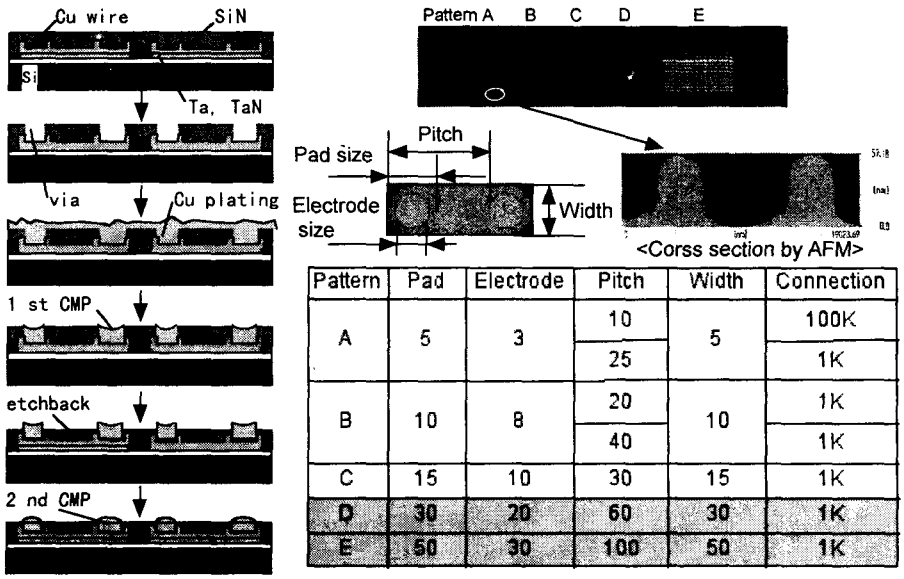

Pattern	Pad	Electrode	Pitch	Width	Connection
A	5	3	10	5	100K
			25		1K
B	10	8	20	10	1K
			40		1K
C	15	10	30	15	1K
D	30	20	60	30	1K
E	50	30	100	50	1K

Figure 8. The preparation of the bump-less test vehicles and series of the measurements.

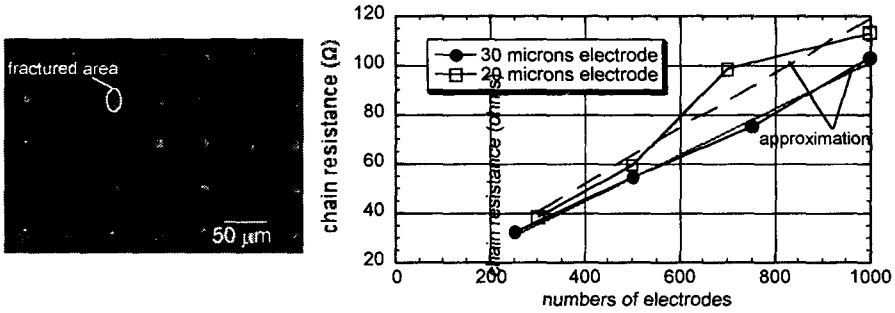

Figure 9. SEM images of debonded surfaces, and the contact resistance.

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