MicroScale

Wafer Bumping Technology

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MICROSCALE CO., LTD

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I. Introduction
1. What is Flip Chip?

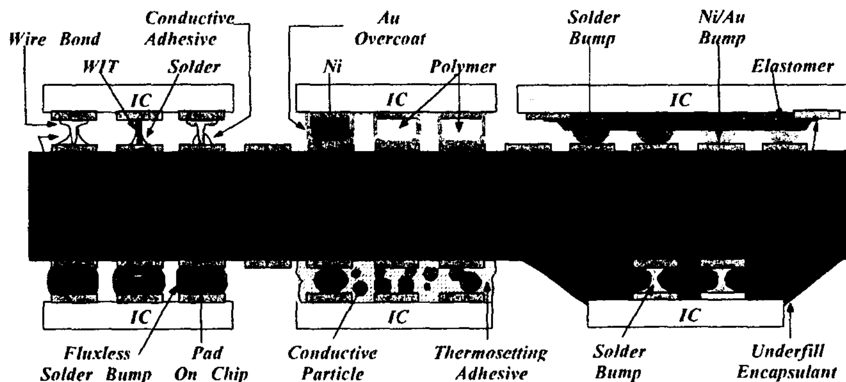
1. Flip Chip is an interconnection technology, not a specific package type.

2. Flip Chip is defined as mounting the chip to a substrate with any kind of materials and methods, as long as the chip surface(active area) is facing to the substrate.

3. Flip Chip Type
: FCIP(Flip chip in package), FCOB(Flip chip on board), FCCSP(Flip chip CSP)

4. Why Flip Chip is important in technology?
: Flip Chip is more than an assembly flow, it's a "technology" with impact in both development and production

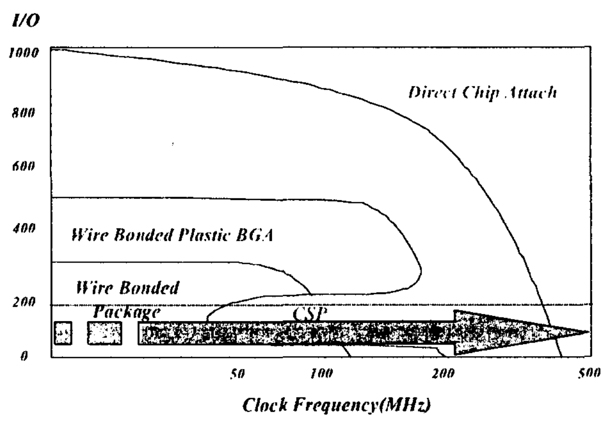
2. Various Flip Chip Technologies



3. Package Trends

Technology Turnover

- **1st Generation**
  Insert Surface Mounting
- **2nd Generation**
  Lead Attach => Ball Attach
- **3rd Generation**
  Wire Bonding => Flip Chip Bonding



II. Market trend

1. Semiconductor Market

(Unit: Million dollars)

ITEM		'98	'99	'00	'01	'02	'03
Memeory	DRAM	15,778	23,104	36,520	58,890	76,000	52,000
	SRAM	3,648	4,461	5,227	6,197	6,570	6,157
	Non-Volatile	5,605	7,063	11,077	14,021	16,012	14,415
	SUM	24,598	35,352	53,625	79,989	99,551	73,531
Micro	Microprocessor	25,496	28,540	33,500	38,000	40,000	42,000
	Microcontroller	10,038	11,806	15,100	18,800	22,000	25,000
	Microperipheral	9,524	11,979	15,732	18,878	19,600	18,400
	DSP	3,853	4,698	7,040	9,630	12,000	15,000
	SUM	48,911	57,023	71,372	85,308	93,600	100,400
Logic		23,619	28,576	36,770	46,197	53,789	56,556
Discrete	Analog	21,182	26,193	33,673	39,197	41,253	41,798
	Discrete	12,771	15,004	18,300	21,470	22,150	20,400
	Optical Device	5,077	6,978	8,374	9,630	10,593	11,122
	SUM	39,030	48,175	60,347	70,297	73,996	73,320
Total		136,158	169,126	222,113	281,790	320,935	303,807

***Source: Data quest 2000.5**

2. Semiconductor Package Market

(Millions of Units)

PKG Type	1998	1999	2000	2001	2002	2003	CAGR(%)
Plastic DIP	1,959	1,222	900	544	418	280	-32.3
Ceramic DIP	137	120	100	95	86	71	-12.3
QFP	14,187	13,429	12,989	12,211	11,654	9,122	-8.5
Ceramic chip carrier	18	12	9	7	4	4	-26.0
Plastic chip carrier	641	566	489	320	280	247	-17.4
SOP	34,516	35,989	39,081	43,000	46,400	41,000	3.5
Ceramic PGA	134	109	101	94	89	62	-14.3
Plastic PGA	98	81	70	62	50	42	-15.6
Ceramic BGA	194	278	378	444	504	512	21.4
Plastic BGA	2,664	3,400	4,521	5,987	7,800	8,000	24.6
Bare Chip	3,042	3,700	4,200	4,577	5,100	5,100	10.9
Chip Scale	356	1,020	2,566	4,540	6,735	7,236	82.6
Other	1,983	2,560	2,980	3,192	3,398	3,400	11.4
Total IC units	59,929	62,486	68,392	75,073	82,518	75,076	4.6

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3. Flip Chip Market(application)

(Millions of Units)

	2000	2001	2002	2003	2004	2005
Computer	288	360	539	783	1,017	1,250
Telecommunication	72	144	283	609	1,057	1,632
Consumer	13	31	71	131	214	370
Automotive	301	328	351	395	460	540
Display		195	365	525	760	1,375
Other	14	33	37	45	51	63
Total	1,095	1,525	2,075	2,945	4,370	5,825

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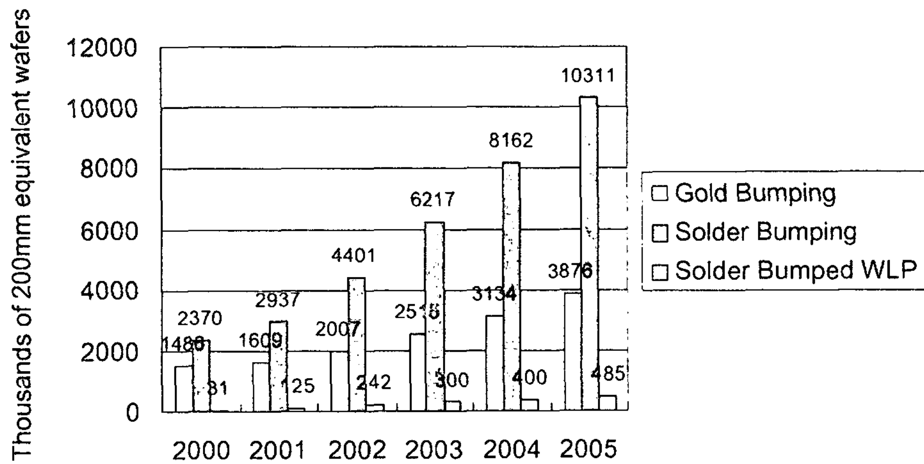
4. Wafer Bumping Market



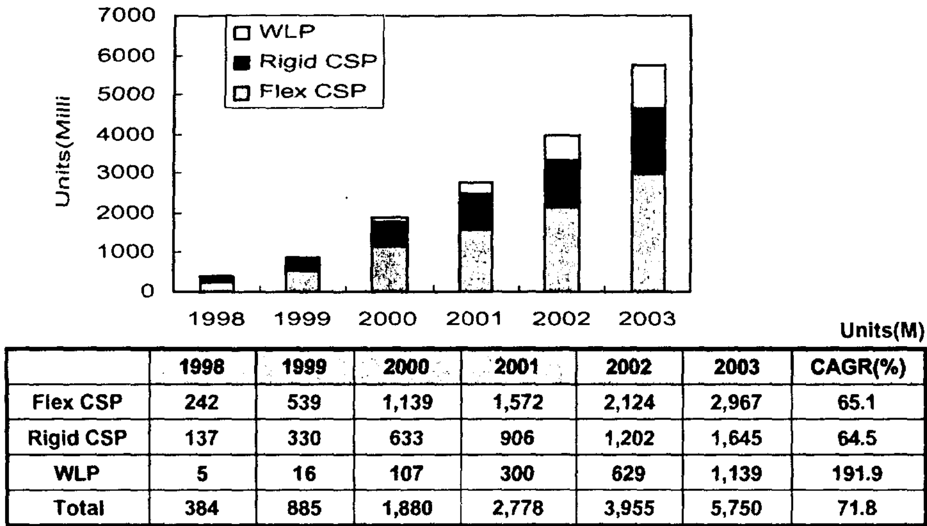
Source :Techsearch International 2001

5. Flip Chip Market(package type)

	1999	2000	2001	2002	2003	CAGR (%)
Flip Chip Units (M)						
PGA FC	68	147	186	240	298	62.6
BGA FC	66	192	457	780	1,118	138.7
CSP FC	31	71	131	214	370	94.8
Total FCIP	165	411	774	1,234	1,787	101.4
FCOB	805	1,012	1,222	1,340	1,525	20.3
Total	970	1,423	1,996	2,574	3,312	38.1

Source : Advanced IC Packaging Markets and Trends

6. CSP Markets



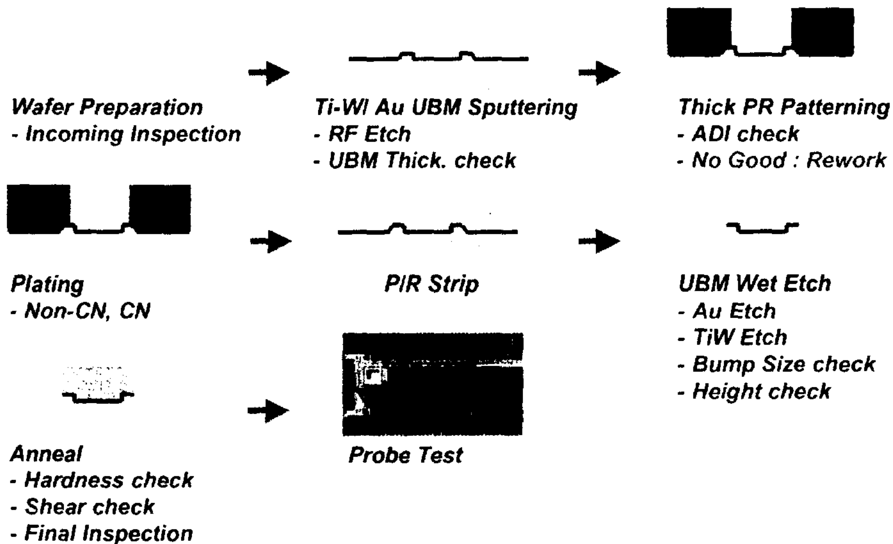
Units(M)

	1998	1999	2000	2001	2002	2003	CAGR(%)
Flex CSP	242	539	1,139	1,572	2,124	2,967	65.1
Rigid CSP	137	330	633	906	1,202	1,645	64.5
WLP	5	16	107	300	629	1,139	191.9
Total	384	885	1,880	2,778	3,955	5,750	71.8

*Source : Advanced IC Markets and Trends

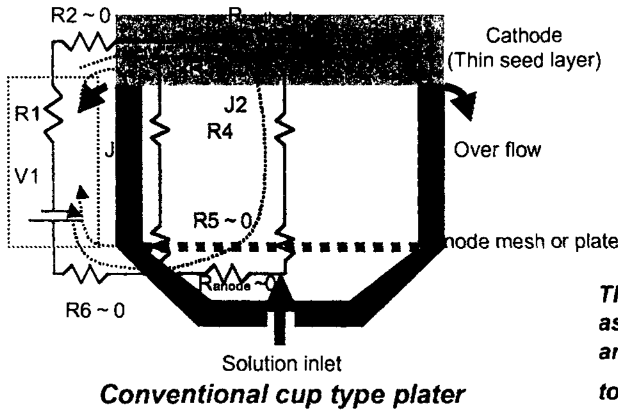
III. Gold bump technology

1. Au Bumping Process flow



2. Hot issues in Gold bump(1)
Large size wafer bumping (Bump Height Uniformity)

Wafer size increases => The bump height at the edge is high than at the center due to terminal effect
What is terminal effect ?



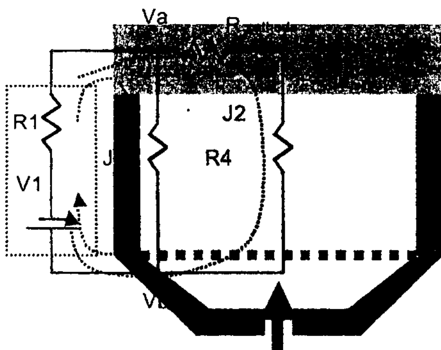
Conventional cup type plater

R1 : Power supply internal resistance
R2 : Power Cable resistance
R3 : Cathode vertical direction resistance
R4 : Plating solution resistance
R5 :Anode vertical direction resistance
R6 : Power Cable resistance
$R_{cathode}$: Seed layer sheet resistance
R_{anode} : Anode layer horizontal direction resistance

This circuit can be simplified assuming that R2, R3, R5, R anode and R6 are approximately equal to 0

2. Hot issues in Gold bump(1)
Large size wafer bumping (Bump Height Uniformity)

Ohm's law and Kirchoff's Laws



Equivalent circuit

$Jt = J1 + J2$
$V1 - JtR1 - J1R4 = 0$
$V1 - JtR1 - J2R_{cathode} - J2R4 = 0$
$V1 - JtR1 = Va - Vb$

$J1 = (Va - Vb)/R4$
$J2 = (Va - Vb)/(R_{cathode} + R4)$

$\mathbf{J1 - J2 = (Va - Vb)R_{cathode}/R4(R_{cathode} + R4)}$

How can we minimize $\Delta J = J1 - J2$?

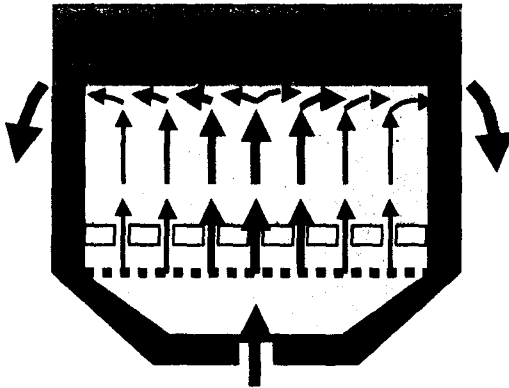
Decrease the Va-Vb : Decrease the Applied Voltage
-> Decrease the depo. Rate

Decrease the $R_{cathode}$: Thicker seed layer, Low resistivity metal -> Decrease the throughput

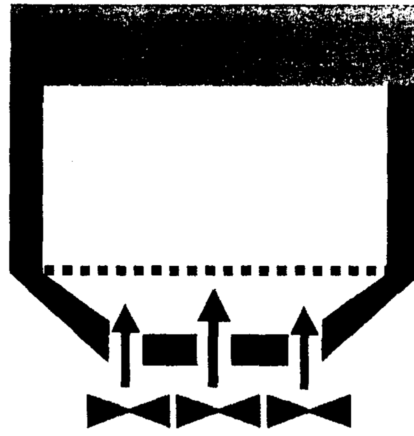
Increase the R4 : **Increase the plating solution resistivity**
-> Increase the Power supply Capa.

2. Hot issues in Gold bump(1)
Large size wafer bumping (Bump Height Uniformity)

How to compensate the terminal effect?



A diffuser is used to compensate the terminal effect



Multi inlet system is used to compensate the terminal effect

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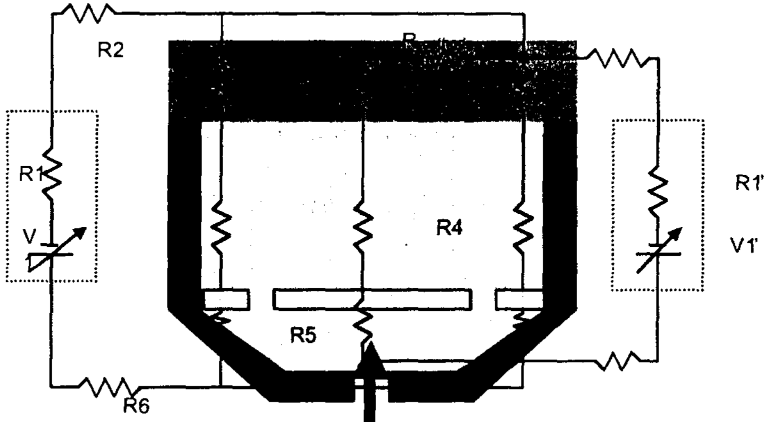
2. Hot issues in Gold bump(1)
Large size wafer bumping (Bump Height Uniformity)

How to compensate the terminal effect?



A Multi-anode system is used to compensate the terminal effect

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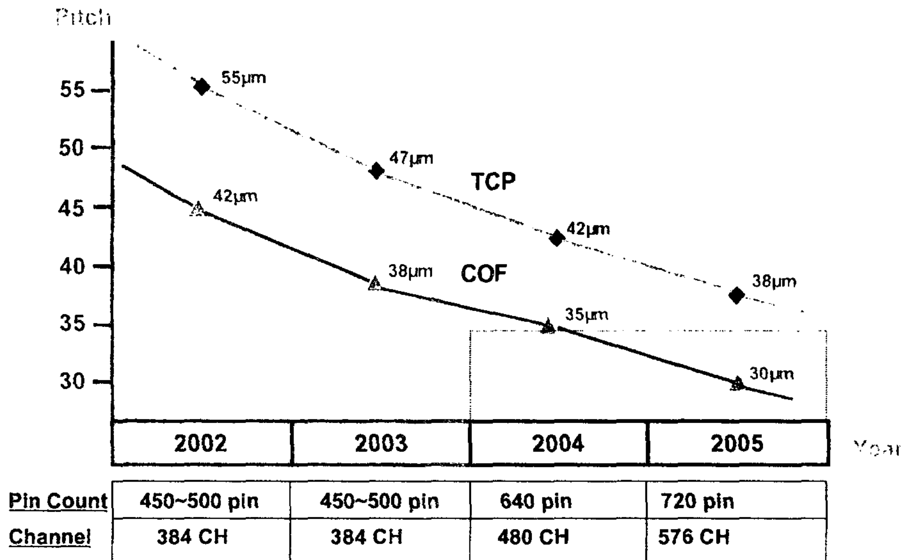
2. Hot issues in Gold bump(2)

Fine pitch accommodation

TCP/COF Roadmap



	2002	2003	2004	2005
Pin Count	450~500 pin	450~500 pin	640 pin	720 pin
Channel	384 CH	384 CH	480 CH	576 CH

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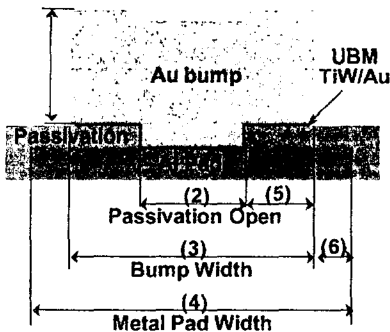
2. Hot issues in Gold bump(2)

Fine pitch accommodation

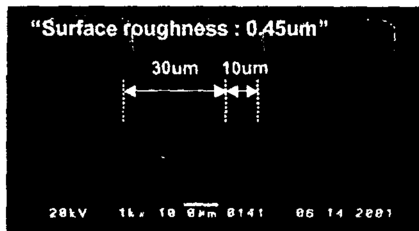
Gold bump design rules



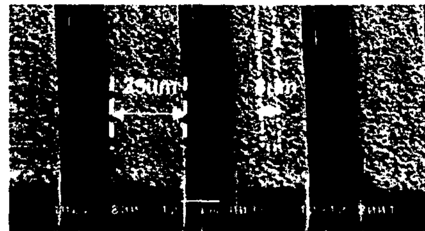
Spec Items	Spec Description
(1) Bump height	18 um (required by customer)
Bump height Tolerance	Within Die ; - 1 ~ +1 um Within Wafer ; - 2 ~ +2 um Wafer to Wafer ; - 3 ~ +3 um
(3) Bump Width	25 um (Typically Bump Top)
Bump to Bump Space	10 um (Typically Bump Top)
(5) Bump & Passivation Overlap	> 5 um
(6) Metal edge to Bump Gap	> 3 um
Bump Mis-align Margin	< 3.0 um (Pad center)

2. Hot issues in Gold bump(2)
Fine pitch accommodation

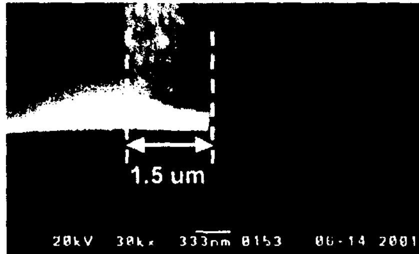
Bump To Bump Min. Space : 10um



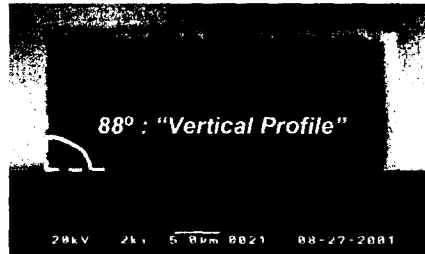
Bump Min. Size : 25um



Under-cut after UBM Wet Etch : 1.5um



Bump Slope : 86~90



2. Hot issues in Gold bump(2)
Fine pitch accommodation

Solutions

- *Decrease the misalign margin :*
  Aligner(~3um) =>Stepper : Decrease the through put ⇒ cost increase
- *Modify the pad design :*
  Increase the pad length
- *Introduce the New materials and M/C*
  Improved UBM etchants => Reduce the under cut
  New thick PR materials => Decrease the bump space
  Improved sputter M/C => Enhance the UBM thickness uniformity
  => Reduce the under cut

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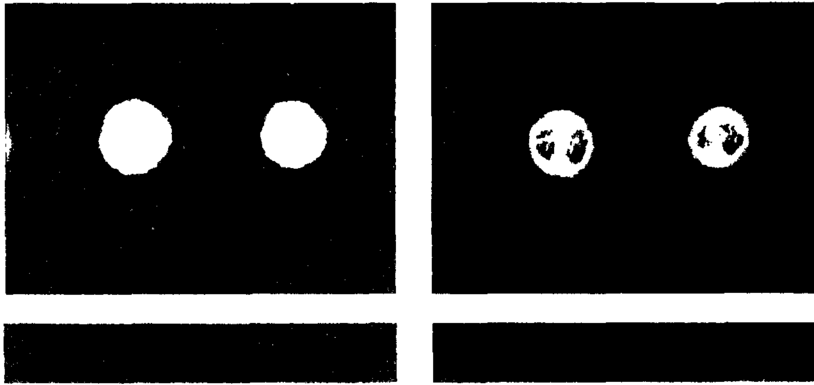
2. Hot issues in Gold bump(3)
EDS test (Tip contamination)



Optical microscope images of the contact points of Probe tip
The contaminants induce the open problem during the EDS test due to the insulating nature of the foreign contaminants

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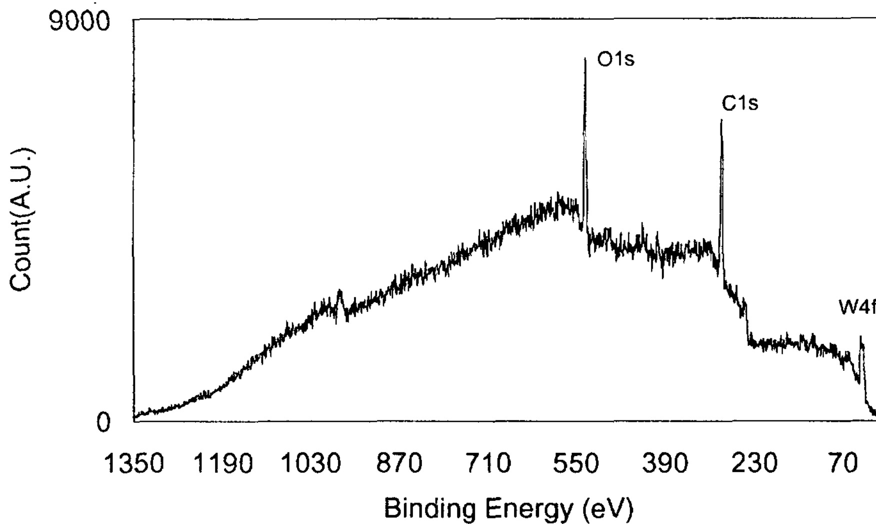
2. Hot issues in Gold bump(3)
EDS test (Tip contamination)



XPS spectrum acquired from the contaminated probe tip
Main contaminants are carbon and oxygen

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2. Hot issues in Gold bump(3)
EDS test (Probe Tip contamination)

The origin of contaminants
- Wafer or passivation debris
- Adsorbed carbon and oxygen on Au bump
- Chemical residue remained on Au bump

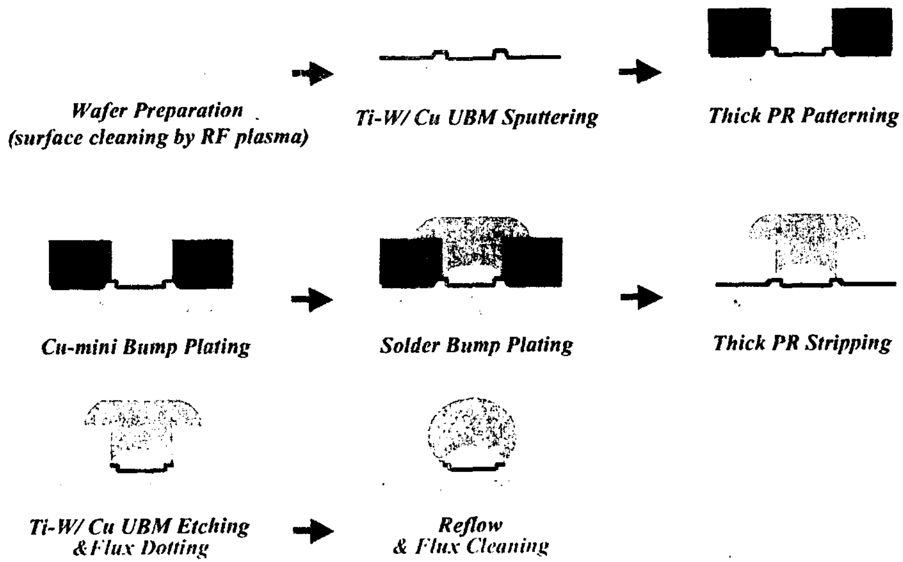
Conventional methods to overcome the probe tip contamination
- Probe tip sanding => Reduce the probe tip life time
- Probe tip cleaning tool => prolong the probe tip life time

The methods that prevent the contaminations
- New probe tip materials
- Thin metal layer formation
- Chemical treatments

IV. Solder bump technology
1. Why Solder Bump in Flip Chip

- ***Low electrical resistance***
- ***High reliability***
- ***Low cost***
- ***Self alignment***

2. Solder Bumping Process by Electroplating



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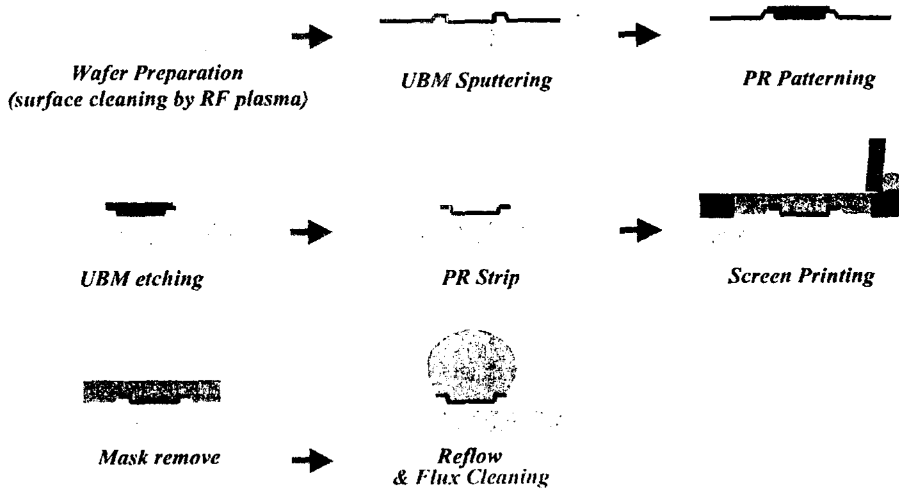
3. Solder Bumping Process by screen printing



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4. Solder bumping processes and their characteristics

	C4 Process	Electroplating	Stencil Printing
UBM	Evaporated CrCu	Sputtered TiW	Electroless Ni/Au Sputtered NiV
Solder Application	Evaporation	Electroplating	Stencil Printing
Solder Material	Pb/Sn-95/5	Sn/Pb-63/37 Pb/Sn-95/5 Au/Sn-80/20 Other	Sn/Pb-63/37 Lead free
Minimal Pitch	250-300 um	100-200 um	150-200 um
Comment	High yield Long experience High Cost	Very fine pitch Different alloys Redistribution	Low cost Different alloys Lead free solder
Bumping cost			

5. Hot issues in solder bump(1)
Large size wafer bumping & Fine pitch solder bumping

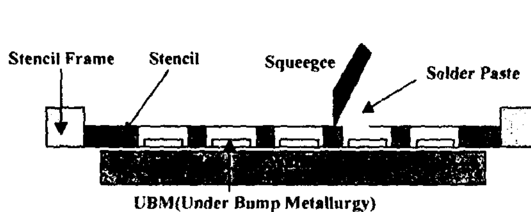
- Electroplating solder bump

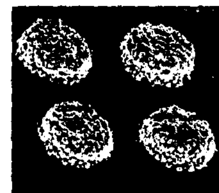
The same methods as electroplating Au bump (Large size wafer bumping)

Fine pitch solder bumping(~ 100 um) is not a critical problem in electroplating process

- Screen printing solder bump

It is very difficult to obtain the highly uniform bumps larger than 6" wafer and the pitch limit is 180 um by conventional screen printing method

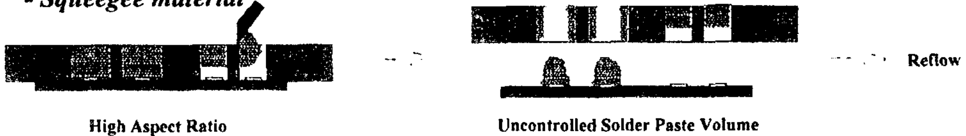




5. Hot issues in solder bump(1)
Large size wafer bumping & Fine pitch solder bumping

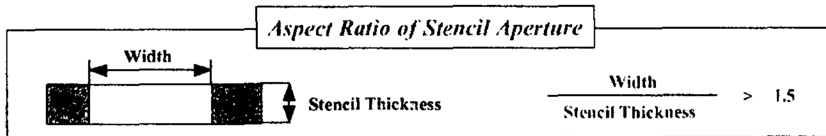
The factors which affect the bump uniformity in Screen printing solder bump

- ***Aspect ratio (Pitch and bump size)***
- ***Side wall roughness of via hole (Mask Fabrication methods)***
  Etching, Laser drilling, Electro-forming
- ***Hole size uniformity (Mask Fabrication methods)***
- ***Solder paste particle size***
- ***Squeegee material***



High Aspect Ratio

Uncontrolled Solder Paste Volume

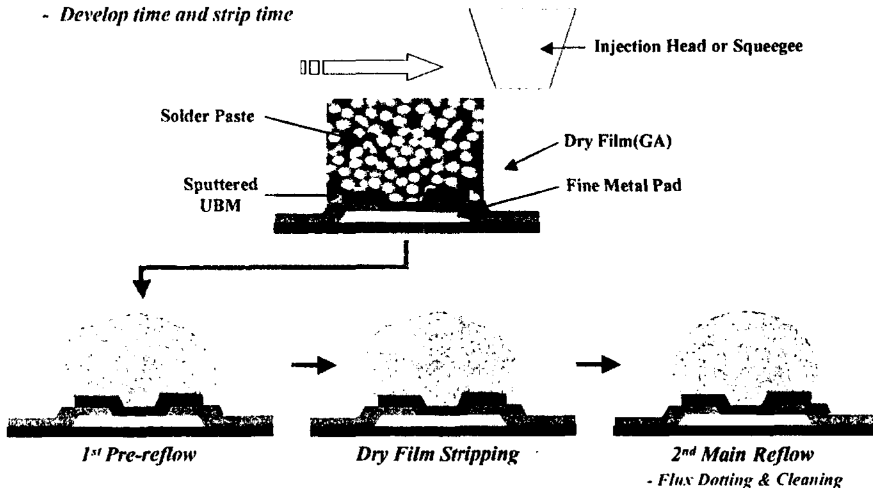


Source: Ekra Presentation

5. Hot issues in solder bump(2)
Fine pitch and large size wafer solder bumping – Dry Film

High Cost Wafer Bumping Method

- *Expensive dry film*
- *Develop time and strip time*



3. Hot issues in solder bump(3)
Lead free solder bump

Available lead free solder and their characteristics

Melting point (℃): 130 140 150 160 170 180 190 200 210 220 230 240 250 260

Alloy system	Low temp	Mid temp	Mid-high temp	high temp
Sn-Pb system		Sn/Pb37	Sn100	
Sn-Bi system	Sn/Bi58 Sn/Bi20/Ag2.0/Cu0.5 Sn/Bi20/In10	Sn/Bi7.5/Ag2.0/Cu0.5 Sn/Bi7.5/Ag2.0		
Sn-In system	Sn/In52			
Sn-Ag system			Sn/Ag3.5 Sn/Ag3.0/Cu0.5 Sn/Ag2.5/Cu0.5/Bi1.0 Sn/Ag3.5/Cu0.5/Bi0.2	
Sn-Cu system			Sn/Cu0.7/Ni0.1 Sn/Cu0.9/Sb0.3	
Sn-Zn system		Sn/Zn9 Sn/Zn9/In5 Sn/Zn9/Bi3		
Sn-Sb system			Sn/Sb1	Sn/Sb1/Cu

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3. Hot issues in solder bump(3)
Lead free solder bump

Comparison between Screen printing and Electroplating solder bump

Item	Screen printing	Electroplating
Minimum pitch	200~150 um	100 um
Available lead free solder	Most of the lead free solder bump materials	Binary system Sn-Bi Sn-Cu Sn-Ag
Composition control	Easy	Difficult
Bump size uniformity	Fair	Good
Cost	Low	High
Large size wafer	Fair	Good

Screen printing is more useful method for lead free solder bump. However, The electroplating solder bump techniques should be developed to satisfy the bump qualities of the high end devices (Uniformity, Fine pitch)

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3. Hot issues in solder bump(3)
Lead free solder bump

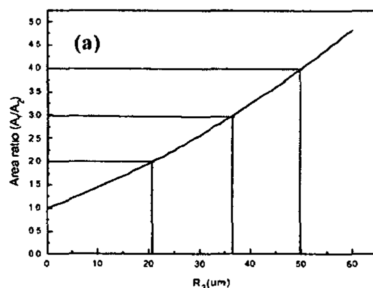
Comparison between electroplated lead free solder

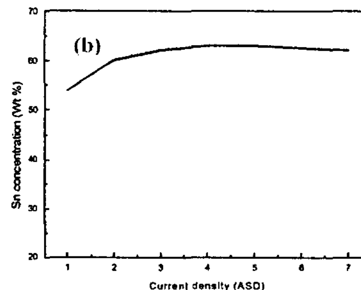
ITEM	Sn-Pb system	Sn-Bi system	Sn-Cu system	Sn-Ag system
Composition	90:10	95:5~98:2	95:5~99.3:0.7	96.5:3.5
Melting point	212 °C	210~229 °C	227~ °C	221 °C
Elongation	28~30%	20%	>30%	73%
Electrical Resistivity	14.99 uohmcm	34.48 uohmcm	11.67 uohmcm	12.31 uohmcm
Hardness(MHv)	5~10	15~25	15~30	13~20
Solderability	A	A	B	B
Shear strength	B	B	B	A
Bending Crack	A	B	A	A~B
Anode material	Sn-Pb	Sn	Sn or Sn-Cu	Sn
Whisker restriction	A	A	C	A~B
Running cost	A	B	A~B	C
Metal Cost	US$ 3.75/lb	US$ 5.85/lb	US$ 3.75/lb	US$ 8.40/lb
Solution stability	A	A	A~B	C

A: Good B: Fair C: Bad

3. Hot issues in solder bump(3)
Some problems in lead free solder bump by using electroplating method

Composition control : In lead free solder(Sn-X), X is small except the Sn-Bi system
Commercially available PR thickness is (30~60 um)
=> Muchroom shape => Plating area increases => Composition changes
=> Melting temp. rapidly increases





(a) ***Expected mushroom surface area to UBM surface area ratio as a function of R_2***
(R_2 = Mushroom radius – UBM radius)
(b) ***Sn concentration changes as a function of applied current density in commercially available eutectic solder solution.***

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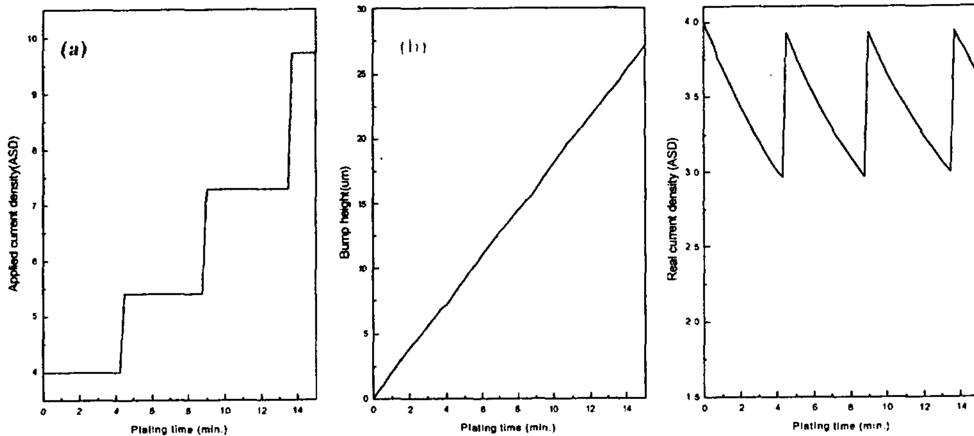
3. Hot issues in solder bump(3)
Some problems in lead free solder bump by using electroplating method

An example of plating recipe simulation to obtain uniform solder composition in eutectic solder



(a) ***Applied current density***
(b) ***Bump height variation as a function of plating time***
Real current density variation as a function of plating time.

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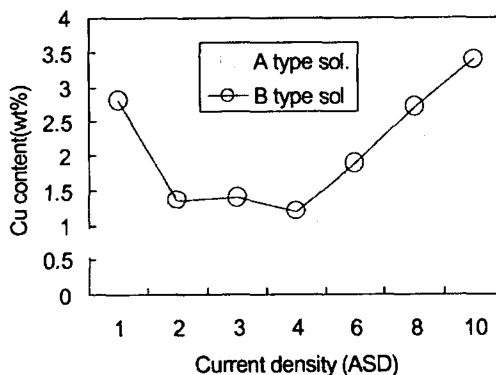
3. Hot issues in solder bump(3)
Some problems in lead free solder bump by using electroplating method



An example of lead free solder (Sn99.3/Cu0.7) bump composition as a function of applied current density

The methods to obtain uniform composition :
Increase the PR thickness : <100 um
Modifying the New lead free solder solution
=> increase the work current range

3. Hot issues in solder bump(3)
Some problems in lead free solder bump by using electroplating method

Grain size and surface morphologies of electroplated Sn-Cu:

(a) A type, 1 ASD

(b) A type, 6 ASD

(c) A type, 10 ASD

(d) B type, 1 ASD

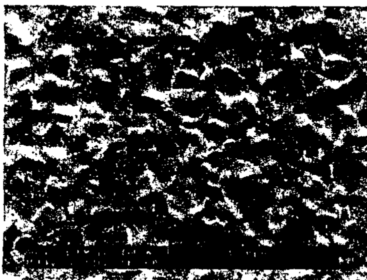
(e) B type, 6 ASD

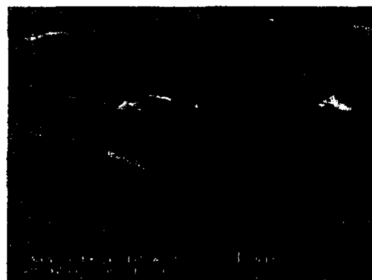
(f) B type, 10 ASD

At low current density, plating surface results is good but deposition rate is too low
At high current density, the packing density decreases => difficult to control the solder size

3. Hot issues in solder bump(3)
Some problems in lead free solder bump by using electroplating method

Grain size and surface morphologies of electroplated Sn-Cu:


(a) A type, 4 ASD, 10 um thick


(b) A type, 4 ASD, 100 um thick

As the thickness of Sn-Cu increases, the grain size increases => difficult to control the bump size

The methods for surface morphology and grain size
Modifying the New lead free solder solution
=> New types of additives are required (not yet solved)

V. Conclusions

- *Annual growth rate of flip chip package market is much high than the other package market*
- *Annual growth rates of Solder bump and Au bump is more than 30% and the growth rate of solder is higher than that of Au bump.*
- *In Au bump technology, large size wafer bumping, fine pitch bump and tip contamination during the EDS test are main issues, and these problems will be settle down sooner or late. However, cost issue will be remain.*
- *In solder bump technology, large size wafer bumping, fine pitch bump and lead free solder bumping are main issues. Particularly, in lead free solder, large size wafer bumping and fine pitch bumping technique are key factors for replacing eutectics solder.*

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