Electrodeposition Technology for Semiconductor and Semiconductor Packaging

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ASET

Introduction

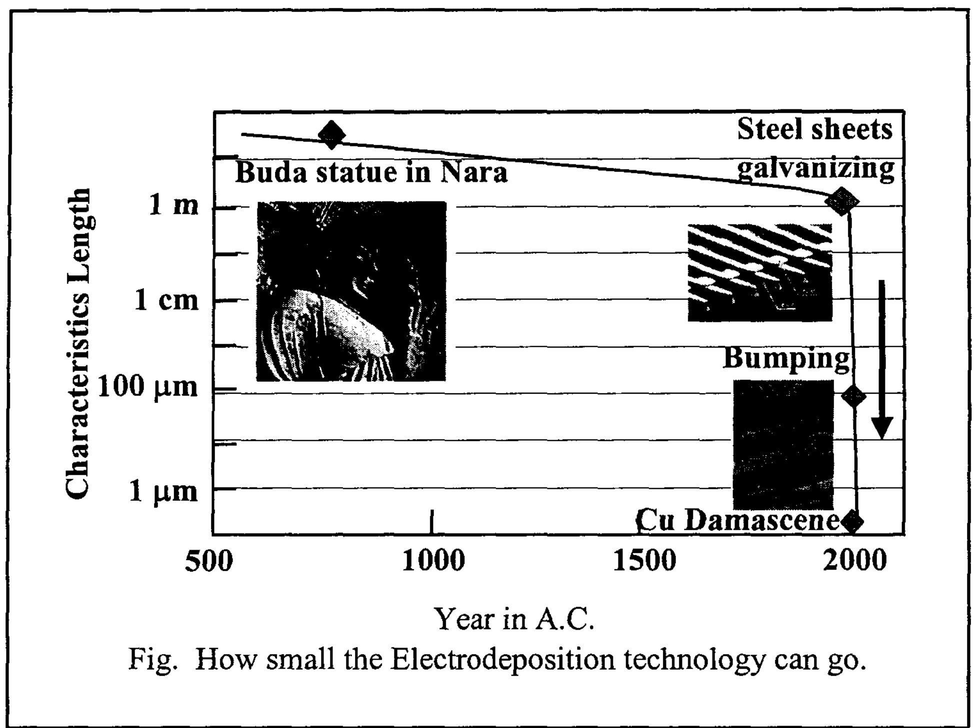


Fig. How small the Electrodeposition technology can go.

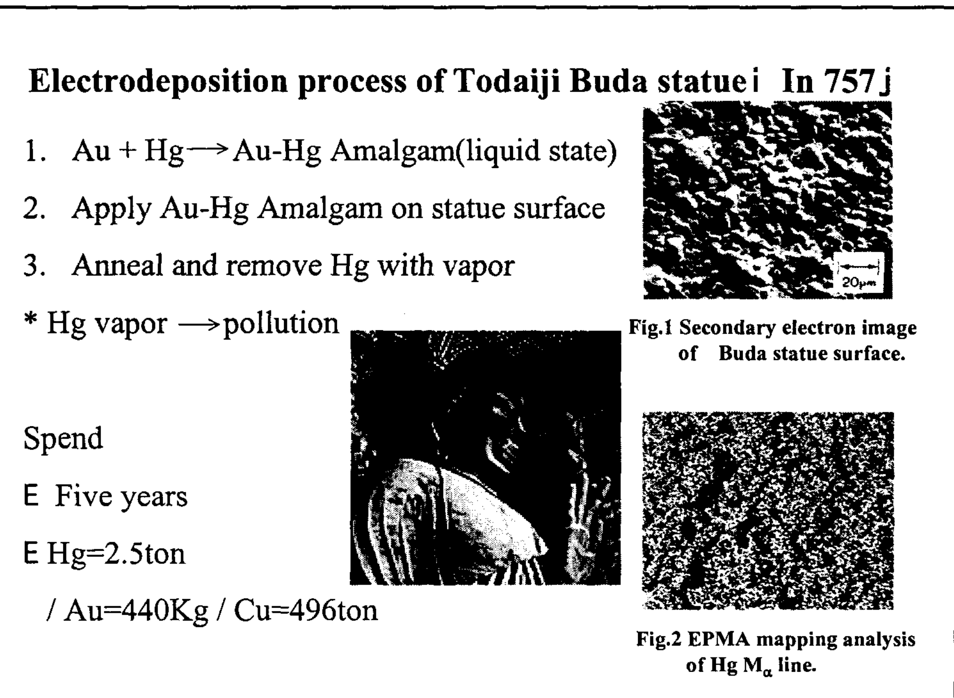
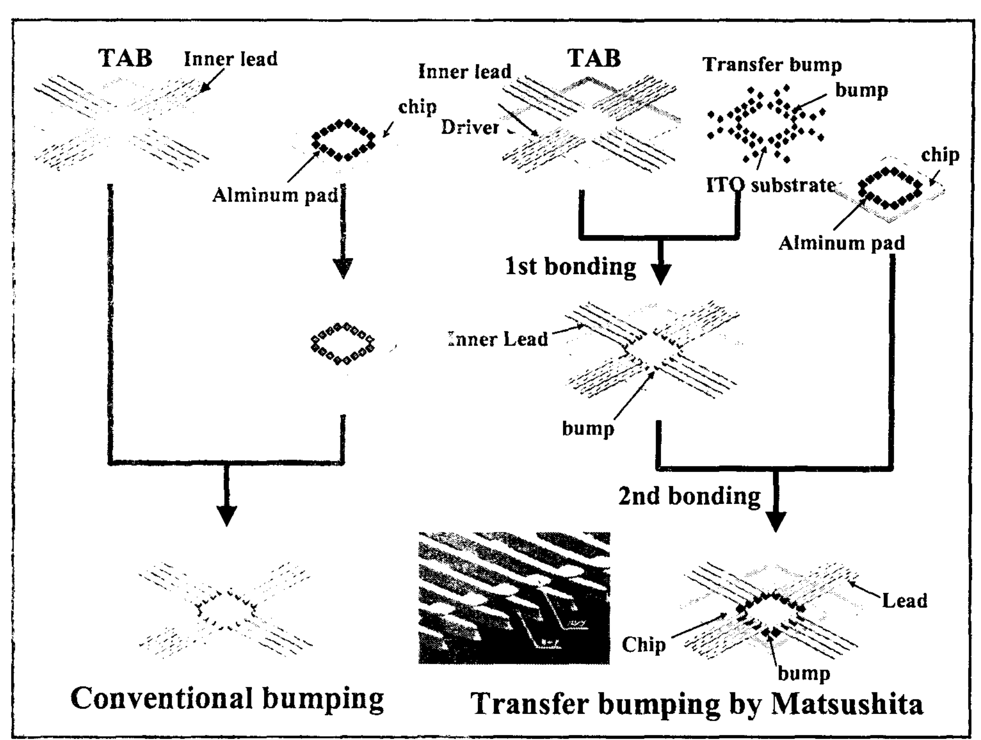
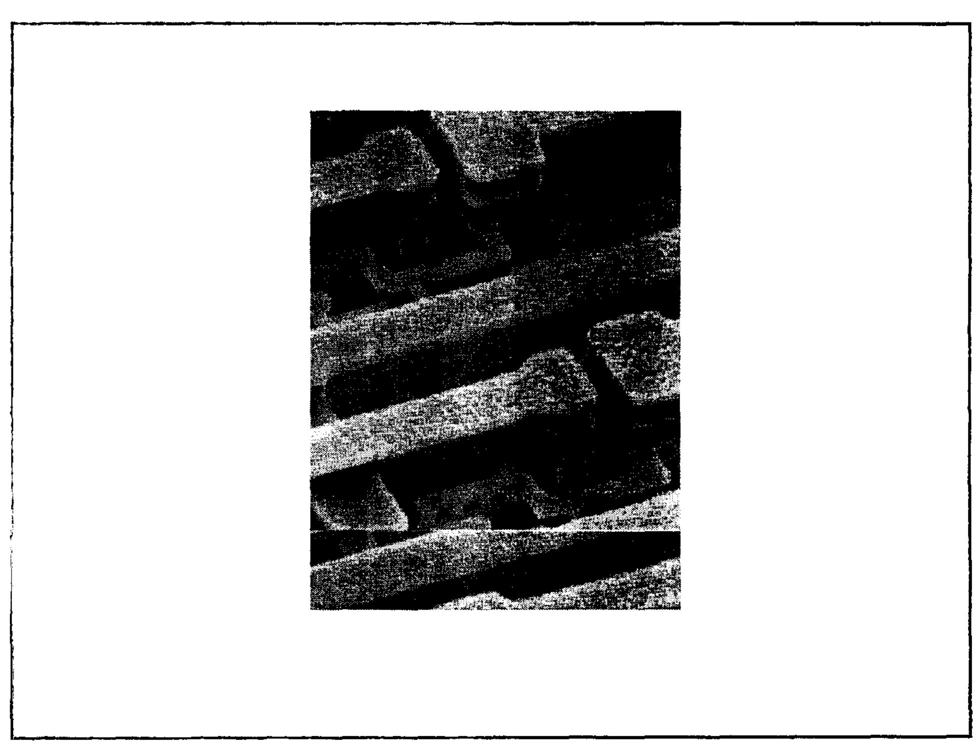


Fig.1 Secondary electron image of Buda statue surface.

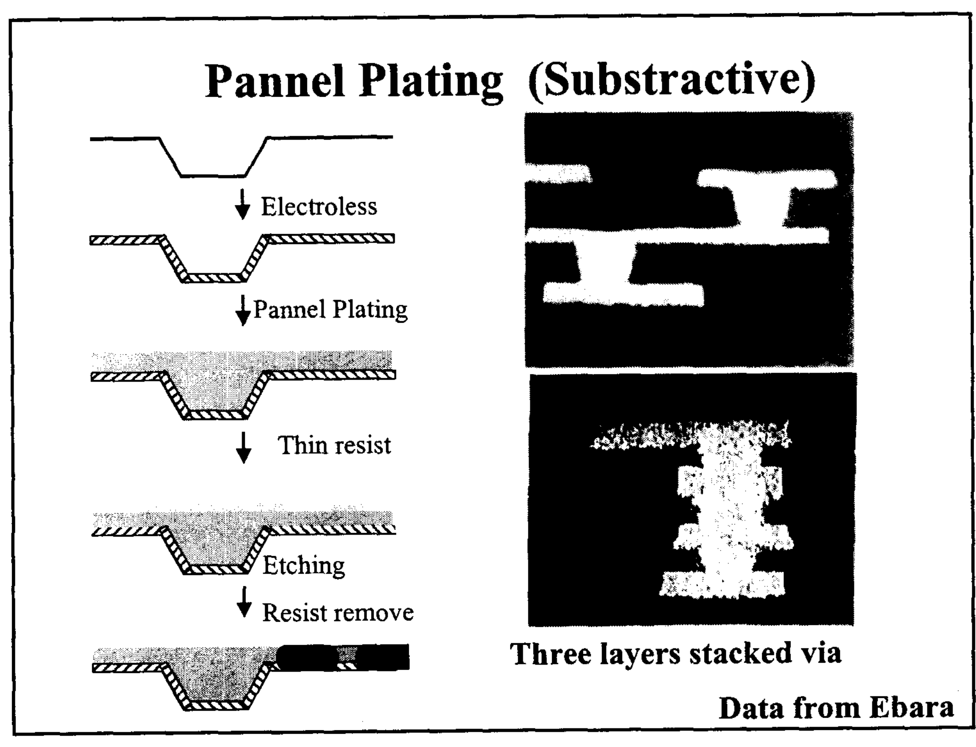
Fig.2 EPMA mapping analysis of Hg M_{α} line.


TAB
Inner lead
chip
Alminum pad
Inner lead
TAB
Driver
Transfer bump
bump
ITO substrate
chip
Alminum pad
1st bonding
Inner Lead
bump
2nd bonding
Lead
Chip
bump
Conventional bumping
Transfer bumping by Matsushita



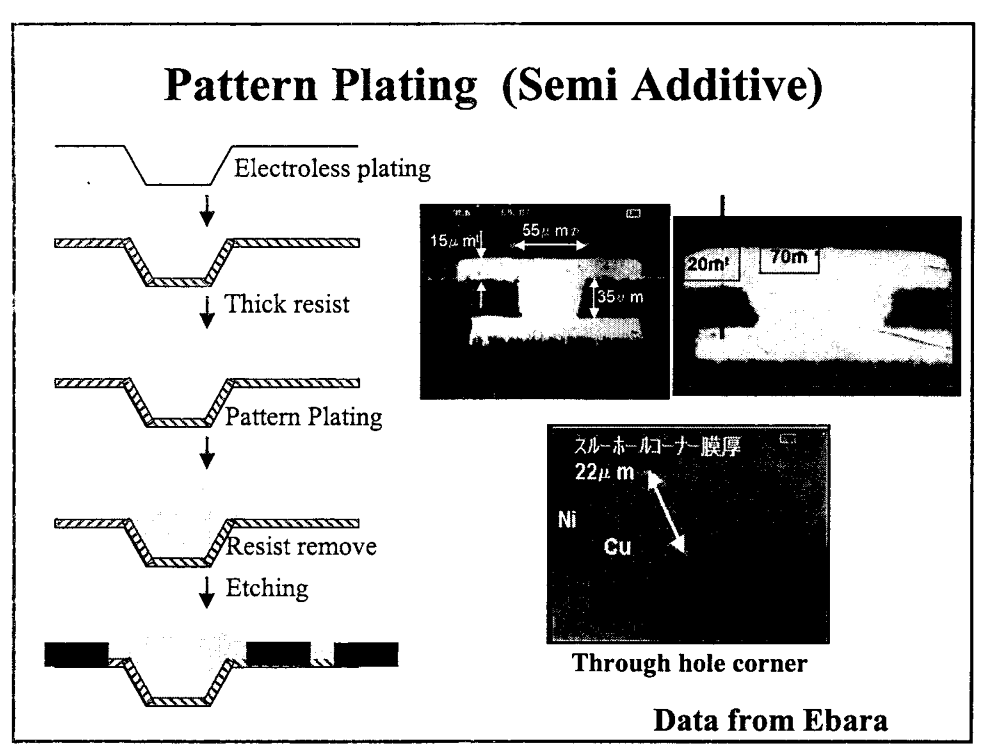
PCB Technologies

Pannel Plating (Substractive)

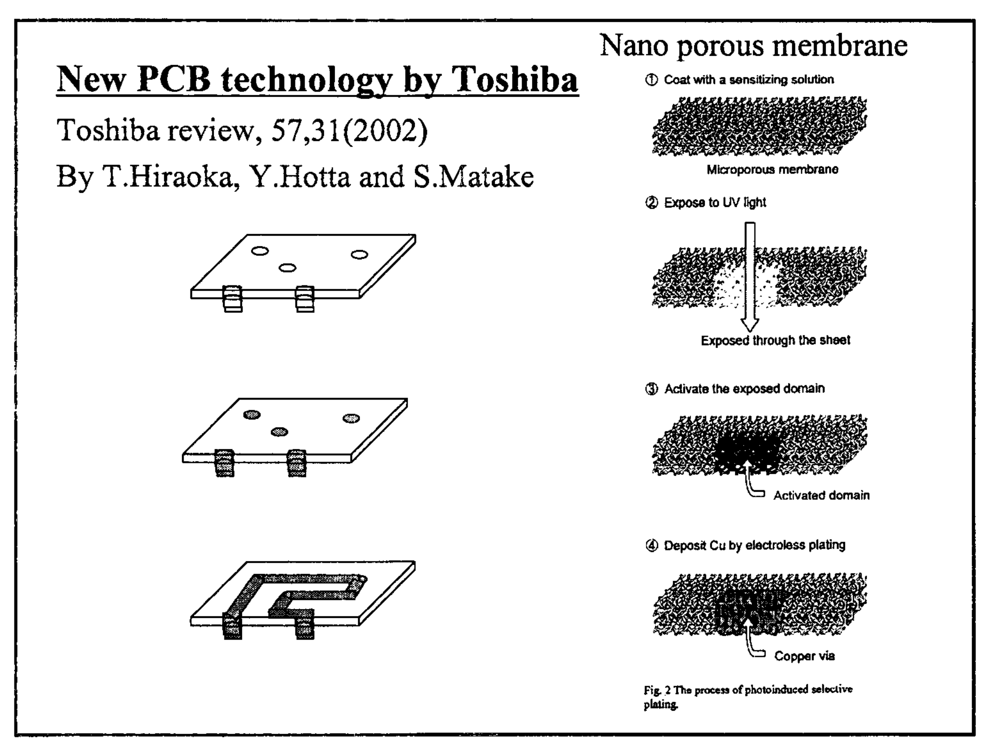


Three layers stacked via

Data from Ebara



Pattern Plating (Semi Additive)
Electroless plating
Thick resist
Pattern Plating
Resist remove
Etching
15μm
55μm
35μm
20m
70m
スルーホールコーナー膜厚
22μm
Ni
Cu
Through hole corner
Data from Ebara



New PCB technology by Toshiba
Toshiba review, 57,31(2002)
By T.Hiraoka, Y.Hotta and S.Matake
Nano porous membrane
① Coat with a sensitizing solution
Microporous membrane
② Expose to UV light
Exposed through the sheet
③ Activate the exposed domain
Activated domain
④ Deposit Cu by electroless plating
Copper via
Fig. 2 The process of photoinduced selective plating

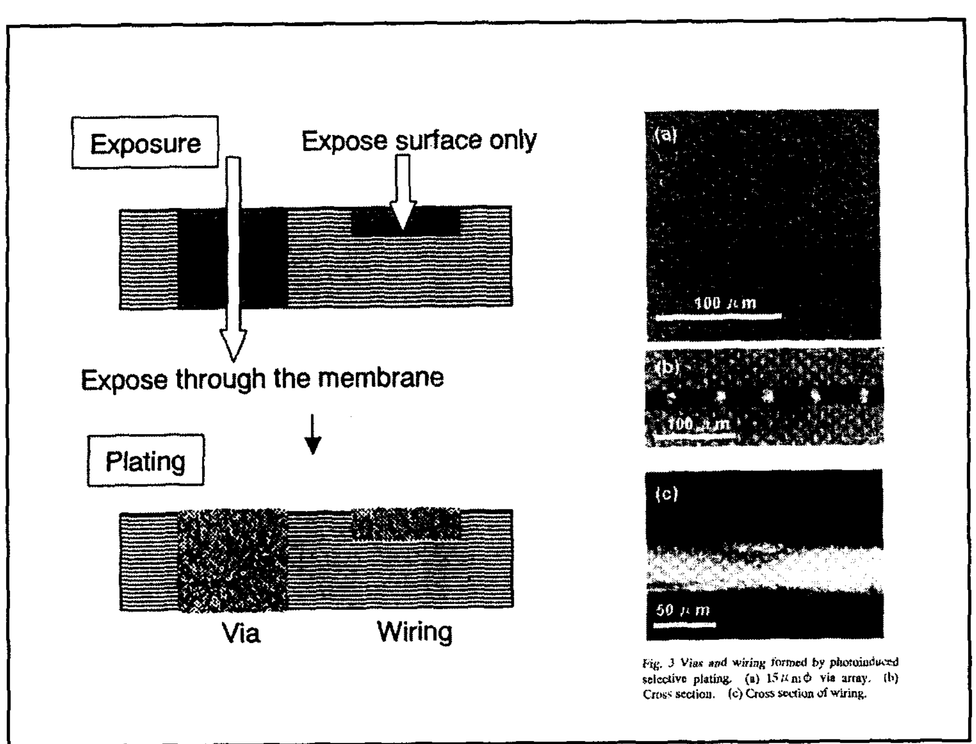
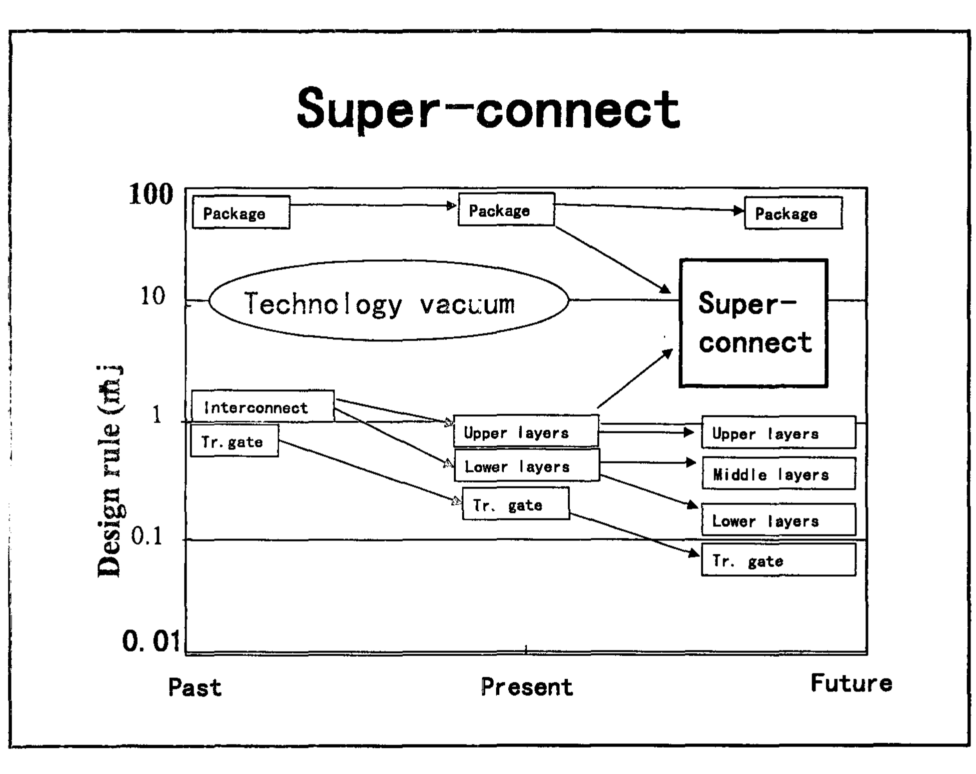
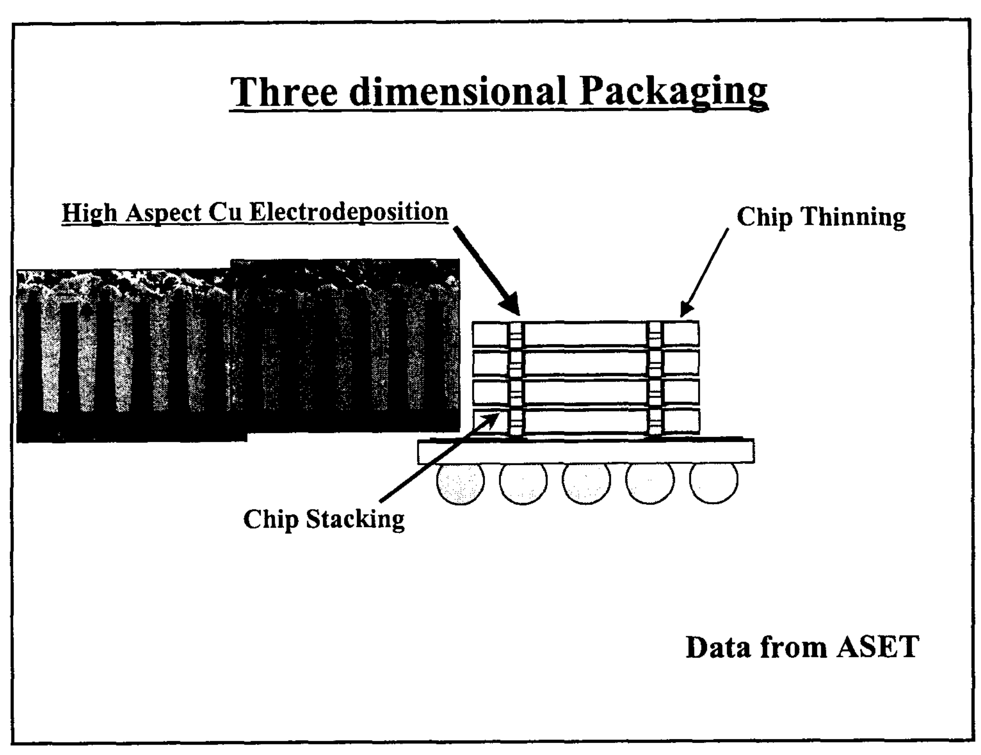
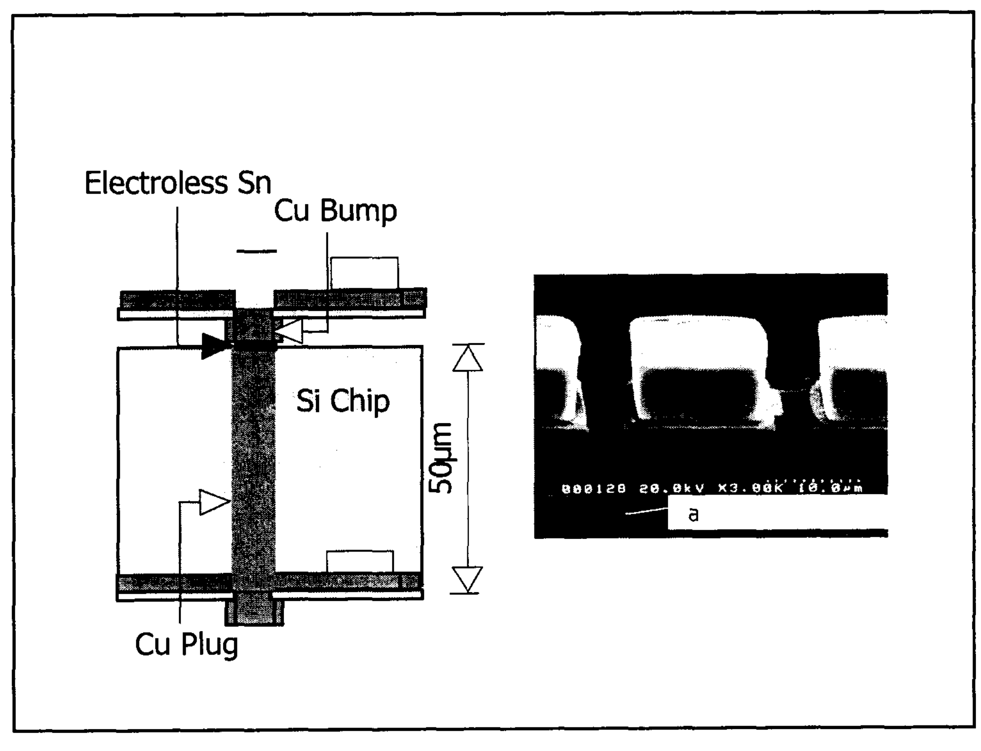


Fig. 3 Vias and wiring formed by photoinduced selective plating. (a) 15 μmΦ via array. (b) Cross section. (c) Cross section of wiring.

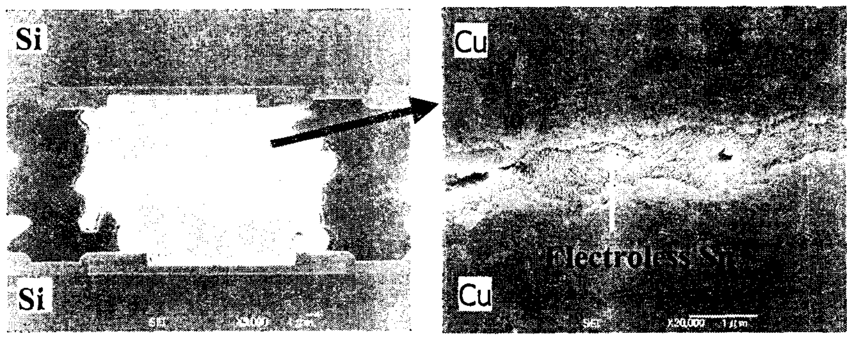
Super connect




Three dimensional Packaging
High Aspect Cu Electrodeposition
Chip Thinning
Chip Stacking
Data from ASET

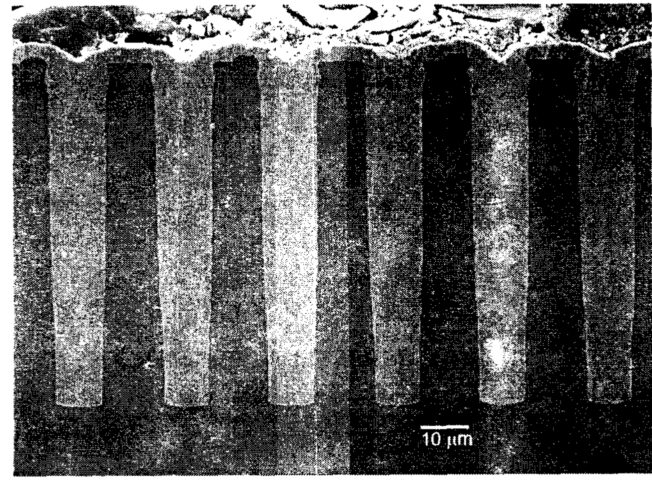

Electroless Sn
Cu Bump
Si Chip
50μm
Cu Plug
a

Cu bump interconnection by electroless Sn
(20 •m pitch 12 •m square)

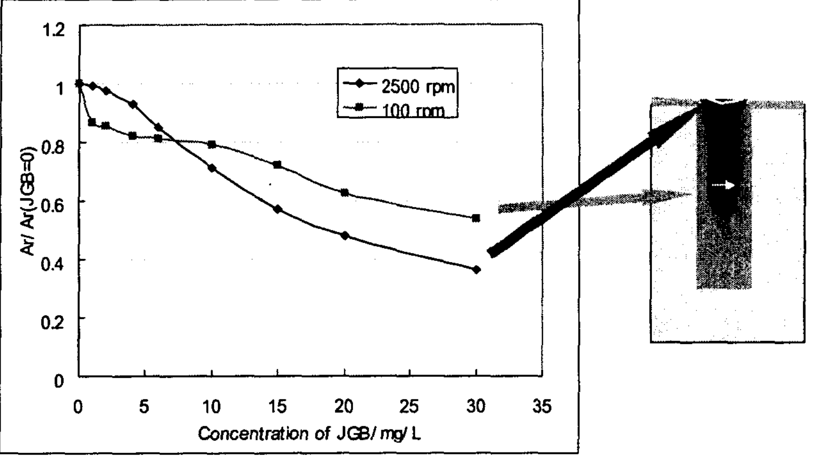


Increasing JGB Concentration

- Perfect Fill



Cycling Voltammetric Stripping (CVS) Method to Evaluate the Inhibition Effect of JGB

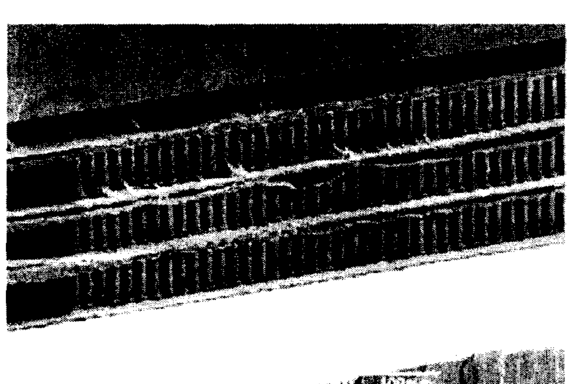


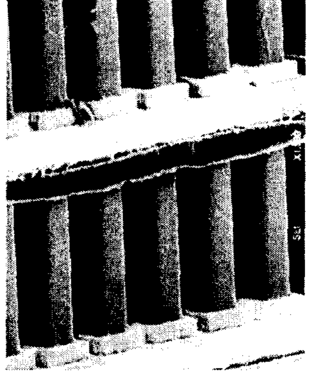
K. Kondo, et al., J. Japan Inst. Electro. Packaging, 3(7) 606 (2000)

ASET Three Dimensional Packaging become real

(Nikkei Micro Device, April(2002))

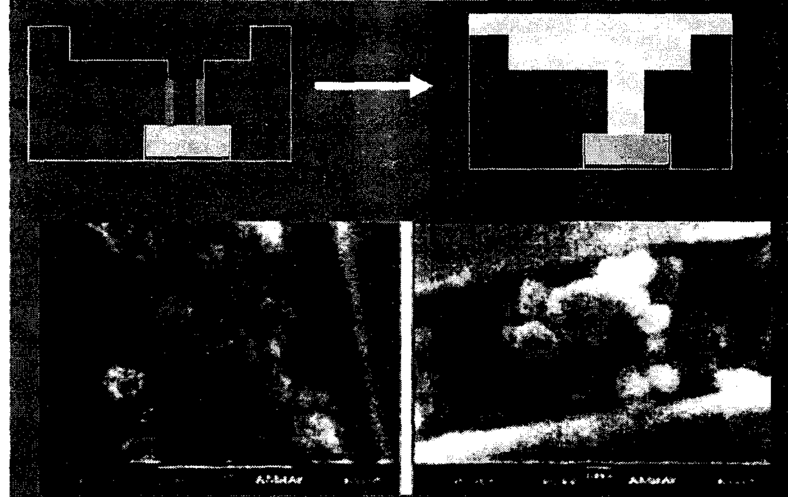
@





Copper Damascene

Direct barrier electrodeposition

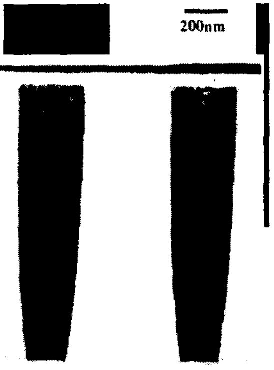


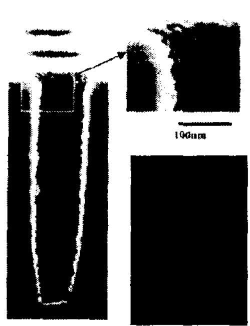
Direct electrodeposition on TaN barrier layer from fluoroborate solution.

ECS Abstract of 2002 spring, Philadelphia Abs.#525

Electroless copper via filling

S. Shingubara et al.
Proc. Advanced Metallization Conference 2000

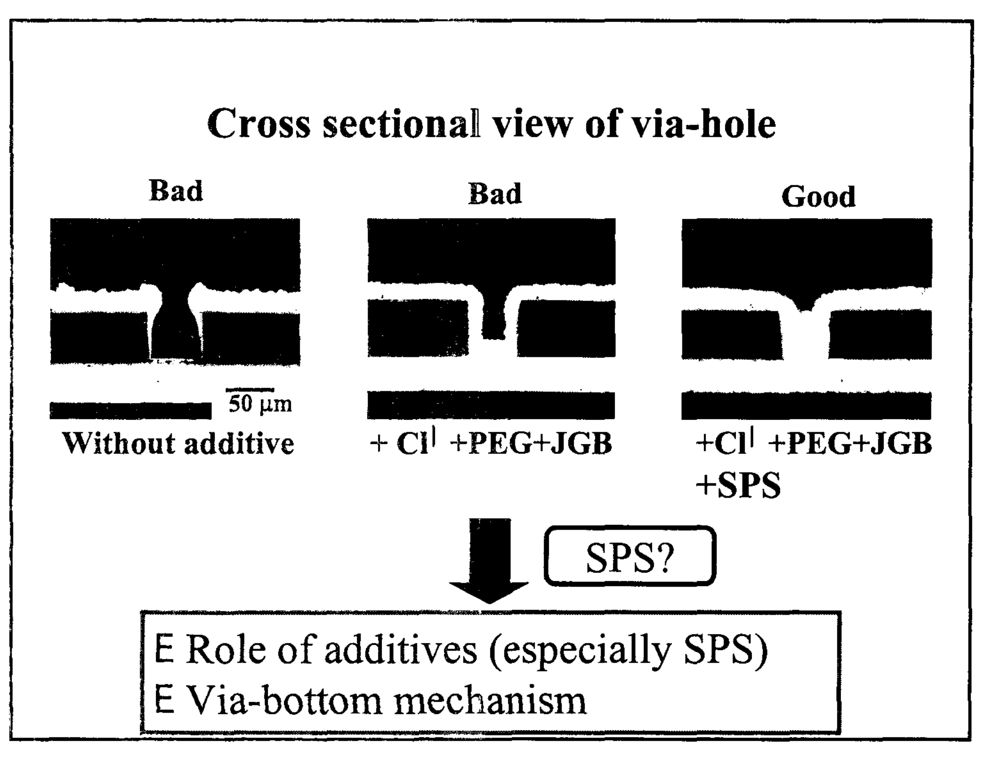


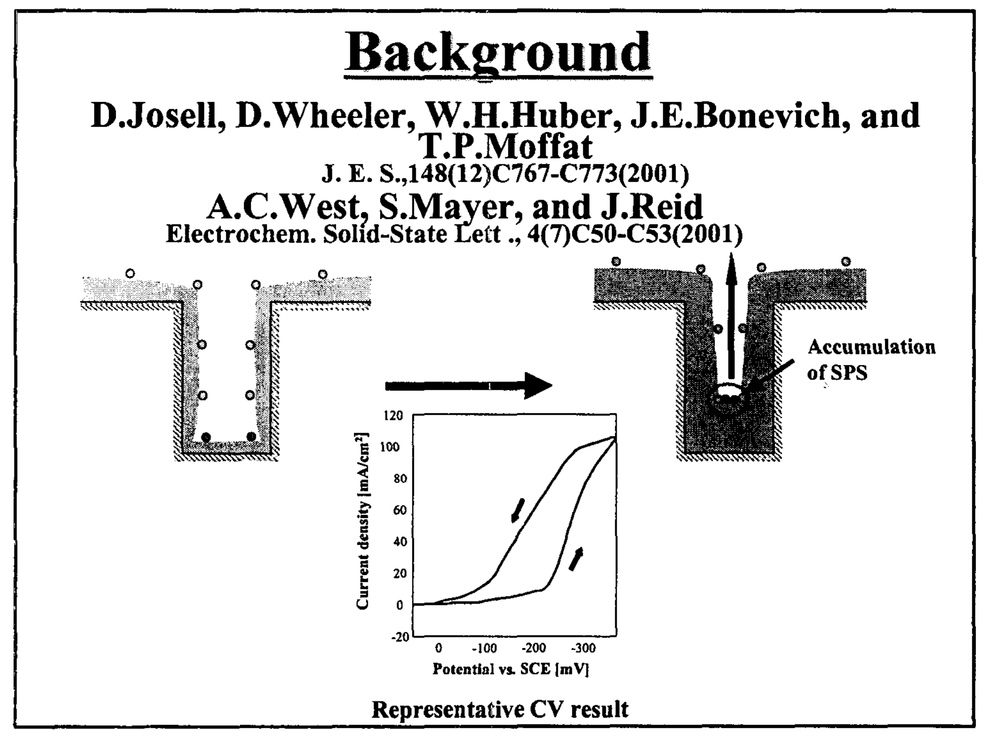


Cross sectional TEM micrograph of Cu electroless plating

SEM micrographs of the intial stage of electrolesscopper.

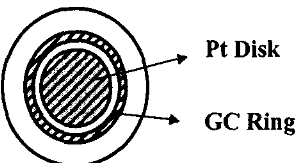
Additive mechanism


Cross sectional view of via-hole
Bad
Bad
Good
50 μm
Without additive
+ Cl⁻ +PEG+JGB
+Cl⁻ +PEG+JGB
+SPS
SPS?
Role of additives (especially SPS)
Via-bottom mechanism

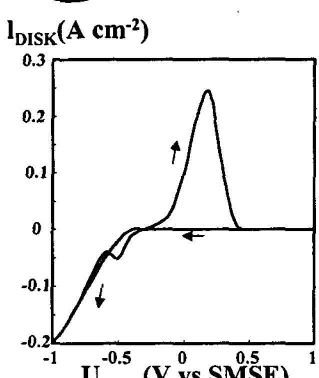

Background
D.Josell, D.Wheeler, W.H.Huber, J.E.Bonevich, and T.P.Moffat
J. E. S.,148(12)C767-C773(2001)
A.C.West, S.Mayer, and J.Reid
Electrochem. Solid-State Lett., 4(7)C50-C53(2001)
Accumulation of SPS
Current density [mA/cm²]
Potential vs. SCE [mV]
Representative CV result

Philippe M. Vereecken, H.Deligiani, K.T.Kwitniak, P.C.Andricacos,

201st Meeting of the ECS, Philadelphia ,Abstract No 517



$CuSO_4 \cdot 5H_2O$ + SPS + HCl + PEG in H_2SO_4



log $I_{RING,norm}$(A cm^{-2})

1, 0.8, 0.6, 0.4, 0.2, 0

-1, -0.5, 0, 0.5, 1

U_{DISK}(V vs SMSE)

Acceleration reaction of deposit growth (SPS)

Cathode model

flat cathode → **pattern cathode**

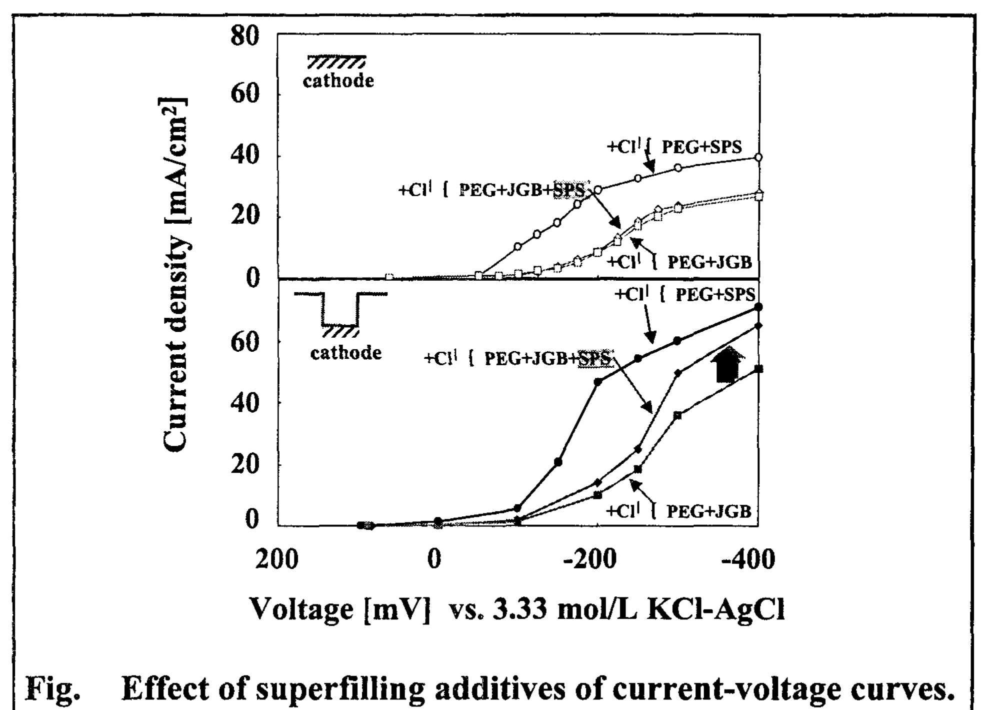
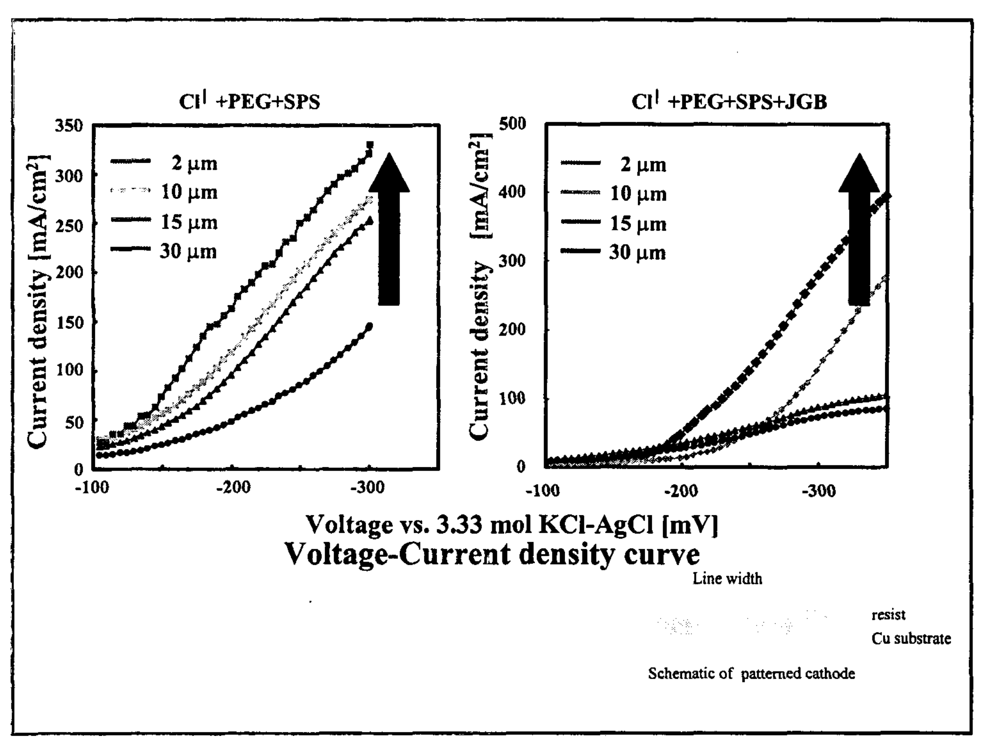
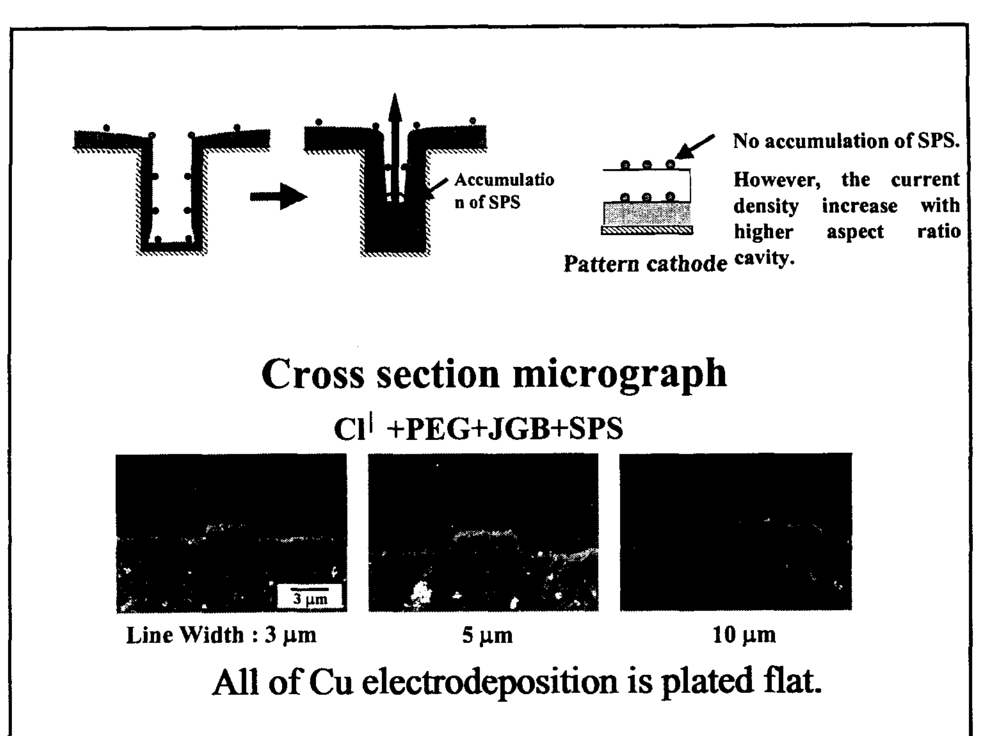
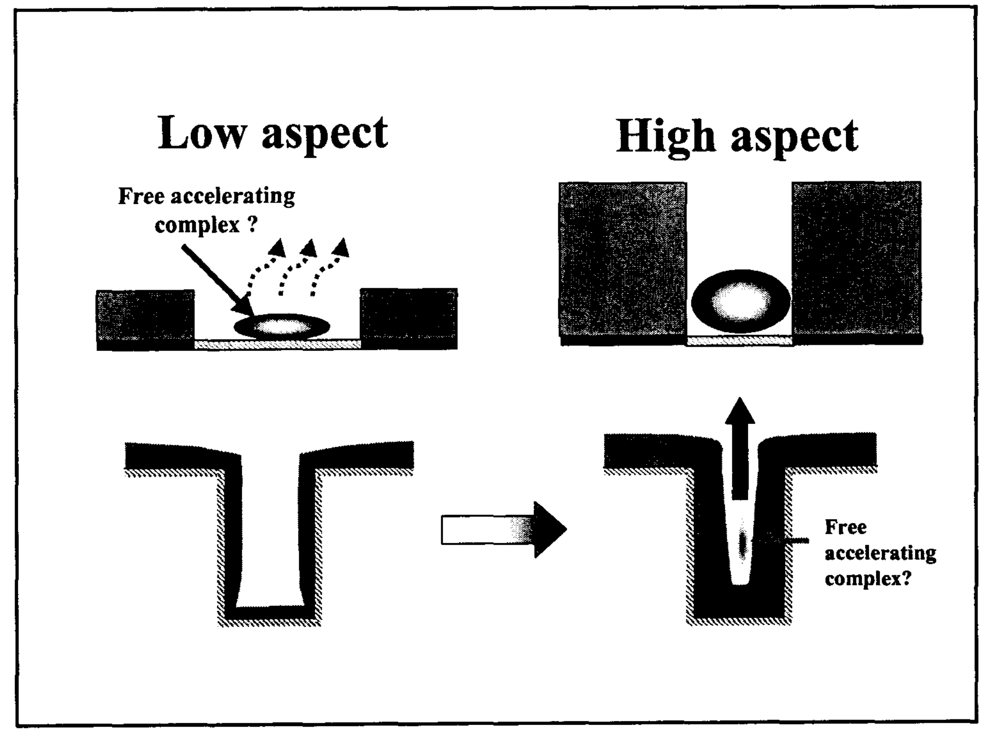


Fig. Effect of superfilling additives of current-voltage curves.



Voltage-Current density curve


Accumulation of SPS
No accumulation of SPS.
However, the current density increase with higher aspect ratio cavity.
Pattern cathode
Cross section micrograph
Cl⁻ +PEG+JGB+SPS
3 μm
Line Width : 3 μm
5 μm
10 μm
All of Cu electrodeposition is plated flat.


Low aspect
High aspect
Free accelerating complex ?
Free accelerating complex?

Future targets of electrodeposition technologies ?