# Prediction Methodology for Reliability of Semiconductor Package

**AMKOR**

**R&D**

**Design & Application**

**Jin-Young Kim**
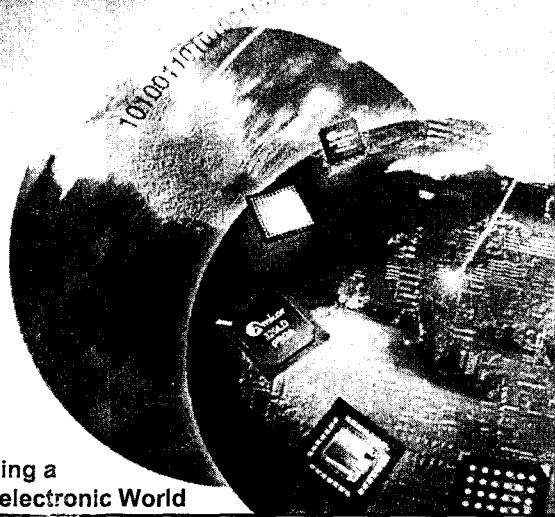
**Amkor Technology**

Enabling a
Microelectronic World

---

# Package Types

**2 Lyr PBGA**
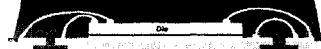
**4 Lyr PBGA**

**TEPBGA - 2**

**TSBGA**

**SBGA**

**etCSP**

**MCM PBGA**

**flexBGA**

**MLF**

Die

**ultraCSP**

ES

**Amkor Technology**

© 2002 Amkor Technology Korea, Inc.

Enabling a Microelectronic World

---

## Mechanical Failures in Package
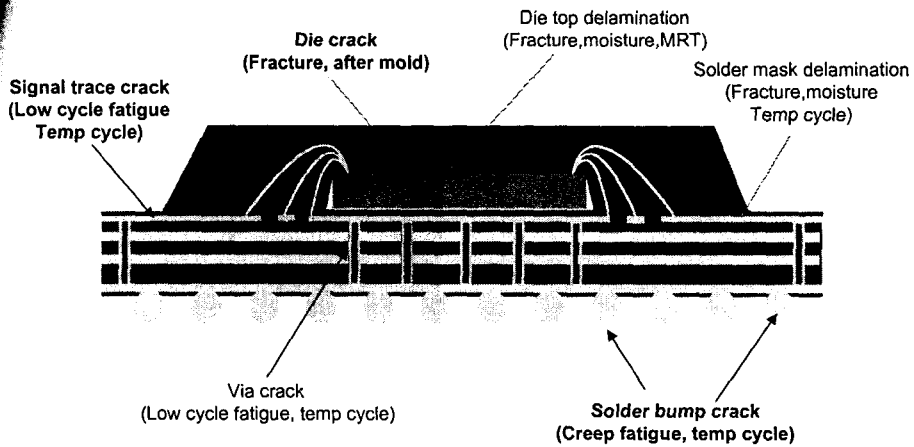
Die top delamination
(Fracture,moisture,MRT)

**Die crack**
**(Fracture, after mold)**

Solder mask delamination
(Fracture,moisture
Temp cycle)

**Signal trace crack**
**(Low cycle fatigue**
**Temp cycle)**

Via crack
(Low cycle fatigue, temp cycle)

**Solder bump crack**
**(Creep fatigue, temp cycle)**

ES

**Amkor**
Technology

© 2002 Amkor Technology Korea, Inc.

Enabling a Microelectronic World

---

# AGENDA

➡ 1. Die crack problem

2. Signal trace failure

3. Soder joint failure

ES

**Amkor**
Technology

© 2002 Amkor Technology Korea, Inc.

Enabling a Microelectronic World

# Mechanical Reliability of Semiconductor Packages
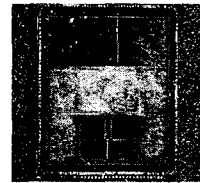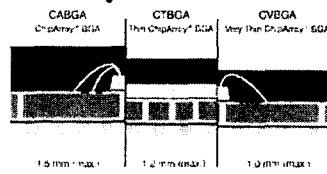## - Die crack problem -

**u Package type**
- CABGA, TABGA, µBGA, flexBGA, etc.
- Thin packages
- Thin substrates (2-layer laminate, Tape)

**◆ Root cause**
- Bending stress caused by molding pressure or external force
- Initial defect on a die surface
  ; micro crack induced by roughness of die

**u Prediction methodology**
- Elastic FEM analysis with temperature dependent material properties.
- Failure criteria based on the maximum stress



CABGA — ChipArray® BGA
CTBGA — Thin ChipArray® BGA
CVBGA — Very Thin ChipArray® BGA

flexBGA

ES

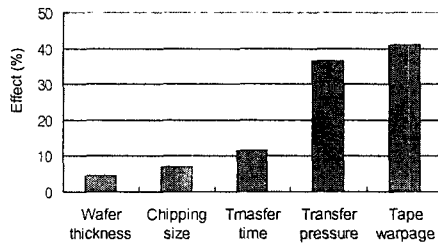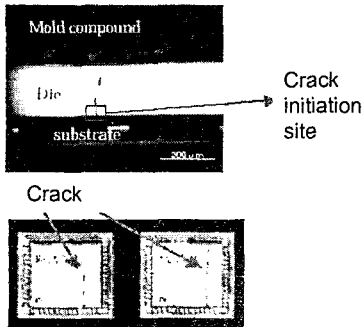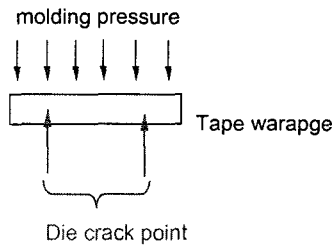Amkor Technology   © 2002 Amkor Technology Korea, Inc.   ...ng a Microelectronic World

---

# Mechanical Reliability of Semiconductor Packages
## - DOE ANALYSIS -

- Die crack propagates from the bottom surface of die
- Die cracks are the horizontal mode in most cases
- Tape/Substrate warpage and molding pressure are significant factors

molding pressure

Tape warapge

Die crack point

Mold compound

Die

substrate

Crack

Crack initiation site



| | Wafer thickness | Chipping size | Tmasfer time | Transfer pressure | Tape warpage |
|---|---|---|---|---|---|
| Effect (%) | | | | | |

ES

Amkor Technology   © 2002 Amkor Technology Korea, Inc.   ...ng a Microelectronic World

81

# Mechanical Reliability of Semiconductor Packages
## - Prediction methodology -

- Analysis of tape/substrate warpage using Finite element method
- Investigation of die flag, trace pattern, and Cu plugging effects
- Suggestion of optimal design to obtain the minimum warpage level
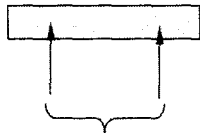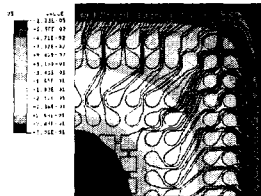- Stress analysis & failure prediction with a optimized design

"Tape warpage"

Warpage Contour

molding pressure

Tape warapge

Die crack point © Amkor Technology Korea, Inc.
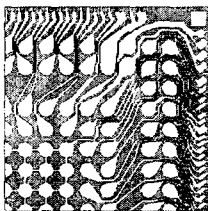
Amkor Technology

Enabling a Microelectronic World

---

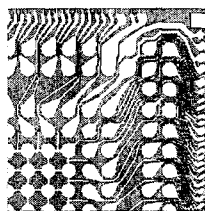# Mechanical Reliability of Semiconductor Packages
## - Optimal Design -

◆ Die flag design
  - Wider connection bar of die flag pattern
  - Larger Cu area of die flag pattern
◆ Dummy Cu pattern in signal trace area is not necessary
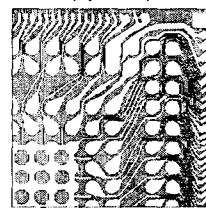◆ Cu plug gives small improvement in tape warpage performance
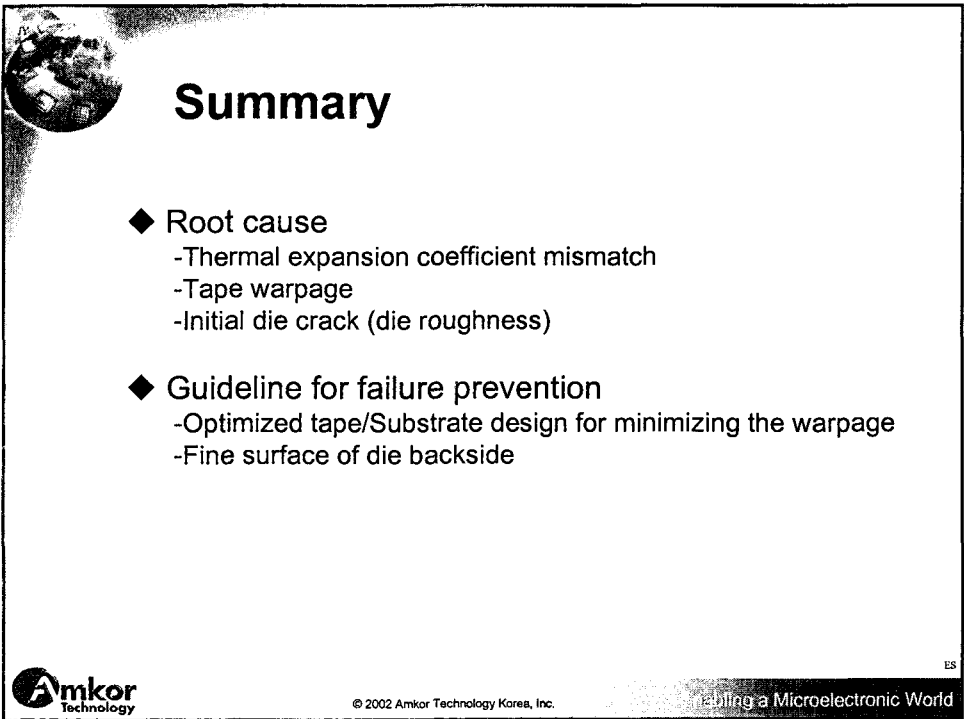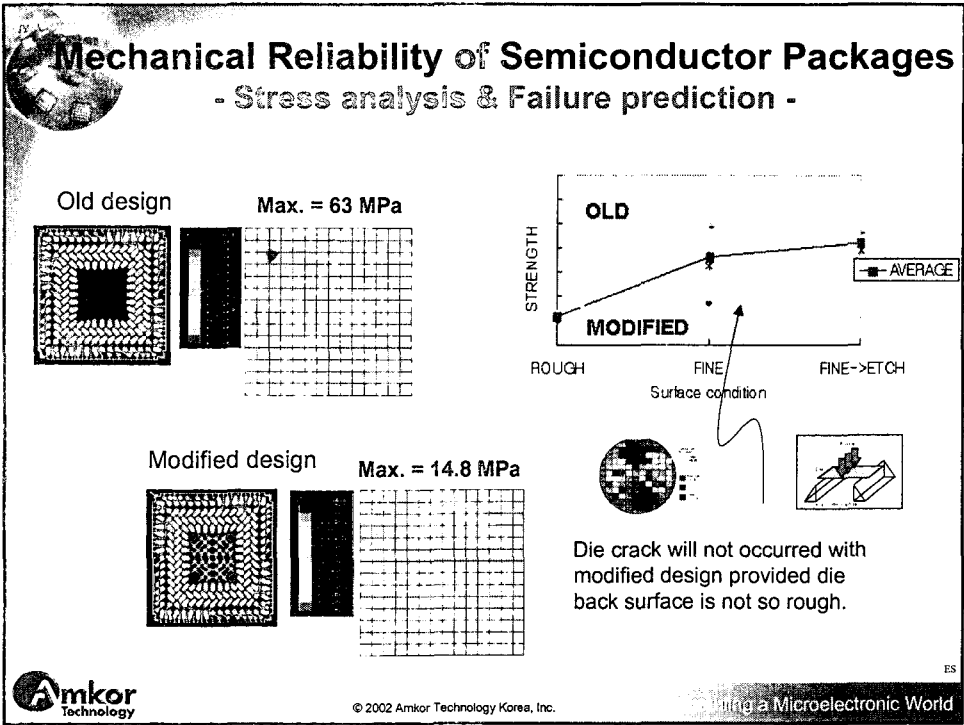
proposal 1

proposal 2

proposal 3 (optimal)

0.2715mm

0.2607mm

0.2073mm

Adding dummy line 4% improve ➡ Enhancement of Connection bar (x3 wider) 20.4% improve

ES

Amkor Technology

© 2002 Amkor Technology Korea, Inc.

Enabling a Microelectronic World

82

# Mechanical Reliability of Semiconductor Packages
## - Stress analysis & Failure prediction -

Old design    Max. = 63 MPa

OLD

STRENGTH

AVERAGE

MODIFIED

ROUGH          FINE          FINE->ETCH
            Surface condition

Modified design    Max. = 14.8 MPa

Die crack will not occurred with modified design provided die back surface is not so rough.

ES

Amkor
Technology

...ing a Microelectronic World

---

# Summary

◆ Root cause
   -Thermal expansion coefficient mismatch
   -Tape warpage
   -Initial die crack (die roughness)

◆ Guideline for failure prevention
   -Optimized tape/Substrate design for minimizing the warpage
   -Fine surface of die backside

ES

Amkor
Technology

...ing a Microelectronic World

# AGENDA

## 1. Die crack problem
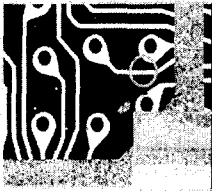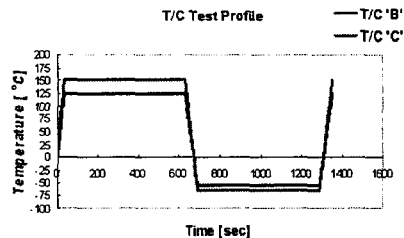➡ ## 2. Signal trace failure
## 3. Soder joint failure

---

# Mechanical Failures of Semiconductor Packages
## - Signal Trace Crack -

u **Package type**
- All kinds of laminate packages with fine pitch design

◆ **Root cause**
- Repetitive bending of a signal trace during temperature cycle
- Solder mask crack propagation
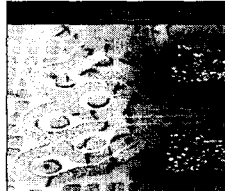
T/C Test Profile —T/C 'B' —T/C 'C'

Temperature [°C] vs Time [sec]

84

# Mechanical Reliability of Semiconductor Packages
## - Modeling Methodology -

- The pkg deformation during the T/C test is obtained using a Global model
- The plastic strain induced at the Cu trace under die is calculated using a Sub-model
- The fatigue life of Cu trace is predicted using low cycle fatigue equation

### Global model

- To obtain the pkg's macro behavior
- 3-dimensional quarter model
- Effective property used for PCB substrate
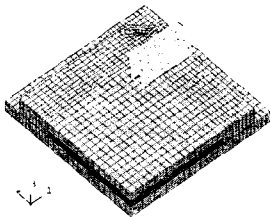
### Sub-model

- To obtain the plastic strain of Cu trace at the interested region
- Layer by layer real property used for PCB substrate
- Epoxy fillet feature considered
- Cu trace width modeling
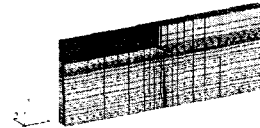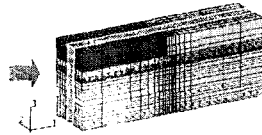
ES
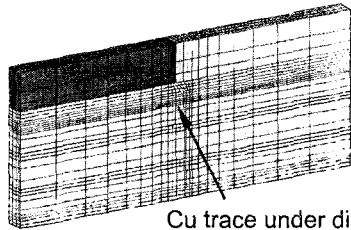
a Microelectronic World

---

# Mechanical Reliability of Semiconductor Packages
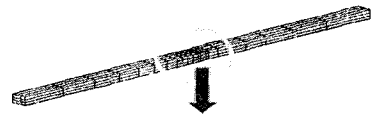## - Deformation of Cu Trace During T/C Test -

T/C 'C' condition

Side view of Cu trace in the Sub-model

Deformed Cu trace under die edge

Cu trace under die

Concentrated Plastic Strain

Deformation with x20 magnification factor

ES

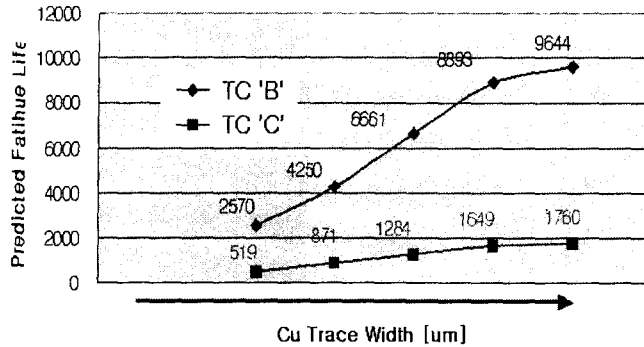a Microelectronic World

Life Prediction Rule

$$N_f^{-m} \times \varepsilon_f^n = PSR$$

Where,
PSR = Plastic Strain Range
$N_f$ = No of cycles-to-failure
$\varepsilon_f$ = Fatigue ductility coefficient (ductility)



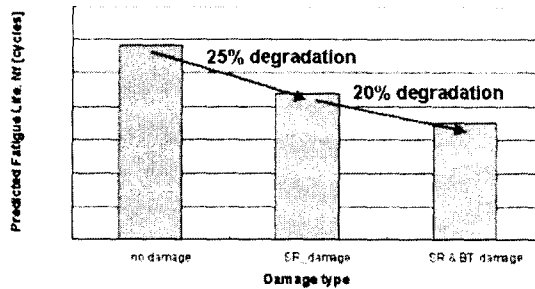Cu Trace Width [um]

---

**Mechanical Reliability of Semiconductor Packages**
**- SR damage effect-**

**Parameters : Initial damage around Cu trace**
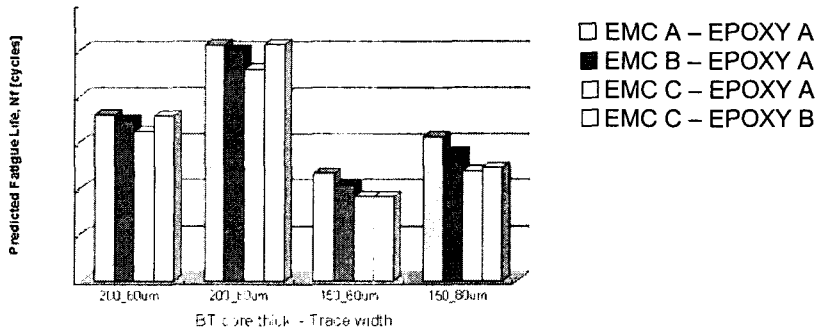


T/C 'C' condition
(-60 oC ~ 150 oC)

# Mechanical Reliability of Semiconductor Packages
## - Material set, BT core thickness effect-

**Parameters : Material set, BT core thick, Trace width**



☐ EMC A – EPOXY A
■ EMC B – EPOXY A
☐ EMC C – EPOXY A
☐ EMC C – EPOXY B

---

# Summary

◆ Root cause
  -Thermal expansion coefficient mismatch
  - Repetitive bending of a signal trace during TC cycle
  - Solder mask damage

◆ Guideline for failure prevention
  - Increase of trace width
  - Don't make signal trace passing the die edge
  - Proper material selection with thick substrate core

# AGENDA

## 1. Die crack problem
## 2. Signal trace failure
## ➡ 3. Soder joint failure

---

# chanical Failures of Semiconductor Packages
## - Creep-Fatigue Failure -

**u Creep-fatigue failure**

- T > 0.3 Tm (melting temperature) : eutectic solder(Tm=183 °C) : ~ 50 °C
- material degradation : micro crack (Pb rich/Sn rich phase), coarsening
- Time dependent failure : ramp rate, hold time
- Accumulated creep strain is the main concern of failure
- Material structure is important ; eutectic/lead free solder
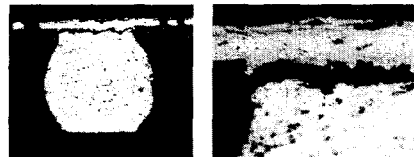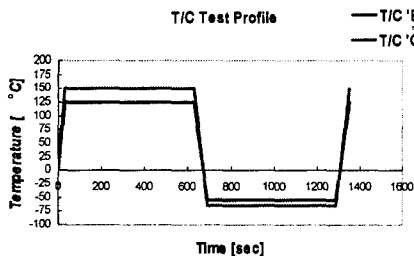


T/C Test Profile — T/C 'B' — T/C 'C'

Time [sec]

# Mechanical Failures of Semiconductor Packages
## - Solder joint reliability -

◆ Failure Mechanism
- Displacement due to mismatch of the CTE
- Thermally induced displacement results in a high peel and shear stress near the bonded edges of joint
- Fatigue crack initiates at the bonded edges
- Crack propagates along the interface leading to failure of the bump

CTE = $\alpha_2$

CTE = $\alpha_1$
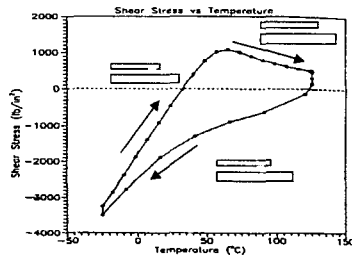


Shear Stress vs Temperature

Shear Stress (lb/in²) vs Temperature (°C) plot

ES

**A**mkor
Technology
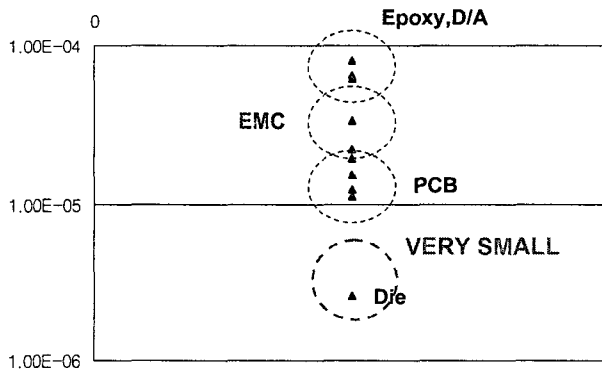
...ing a Microelectronic World

---

# Mechanical Failures of Semiconductor Packages
## - CTE mismatch -

◆ **CTE mismatch is the root cause of all kinds of the mechanical failure**
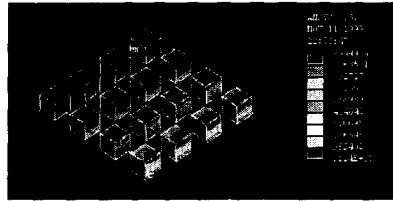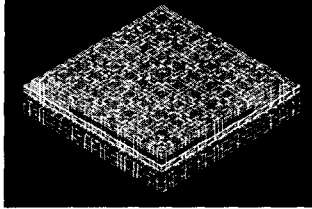- die crack/signal trace crack/solder joint crack



0

1.00E−04

Epoxy,D/A

EMC

PCB

1.00E−05

VERY SMALL

Die

1.00E−06

ES

**A**mkor
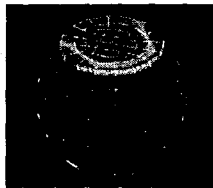Technology

...ing a Microelectronic World

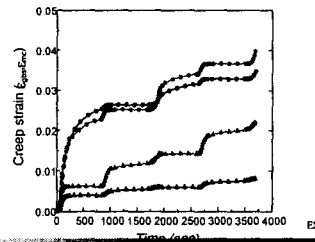# hanical Reliability of Semiconductor Packages
## - Modeling Methodology -

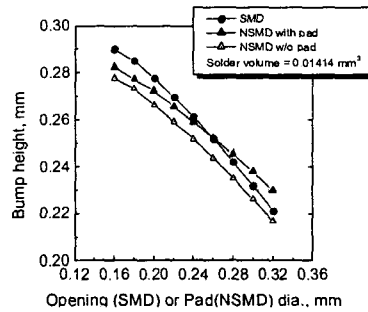- **Global Package Model**



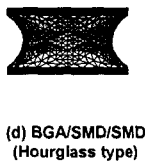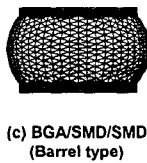- **Local Solder Joint Model**



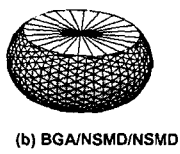Accumulation of creep strain



© 2002 Amkor Technology Korea, Inc.

Enabling a Microelectronic World

---

# hanical Reliability of Semiconductor Packages
## - Solder shape prediction -



(a) BGA/SMD/NSMD

(b) BGA/NSMD/NSMD

(c) BGA/SMD/SMD (Barrel type)

(d) BGA/SMD/SMD (Hourglass type)
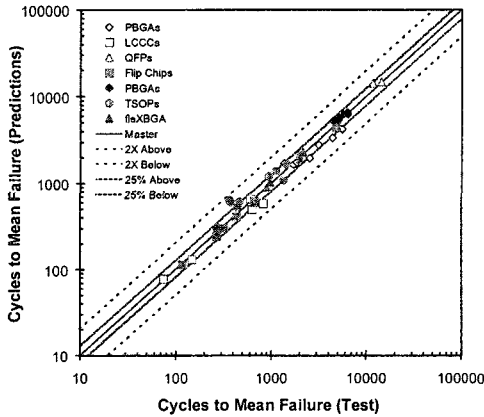


Opening (SMD) or Pad(NSMD) dia., mm

ES

© 2002 Amkor Technology Korea, Inc.

Enabling a Microelectronic World

90

# Mechanical Reliability of Semiconductor Packages
## - Life Prediction Model -



$$N_f = \left( \alpha \, \mathrm{E}_{GBS} + \beta \, \mathrm{E}_{MC} \right)^{-1}$$

*Where,*

$\varepsilon_{GBS}$ & $\varepsilon_{MC}$ = Accumulated Creep Strains
$N_f$ = Cycles to Mean Failure (N50)

First Failure is Estimated from
Mean Life as

Prediction Accuracy : ± 25%

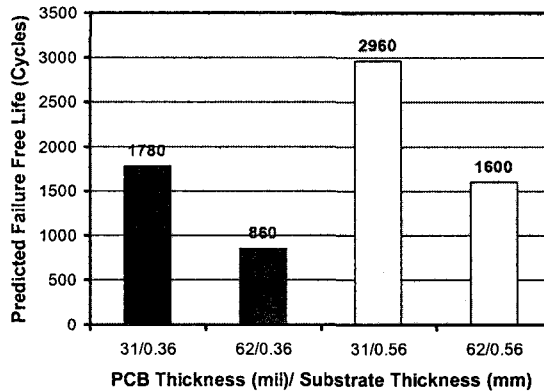$$0.6 N_f \leq First\ Failure \leq 0.7 N_f$$

ES

---

# Mechanical Reliability of Semiconductor Packages
## - PBGA, PCB/Substrate thickness effect -

- **256 PBGA, 17 x 17 mm, 1.0 mm Pitch**
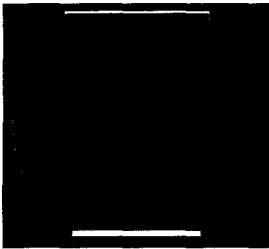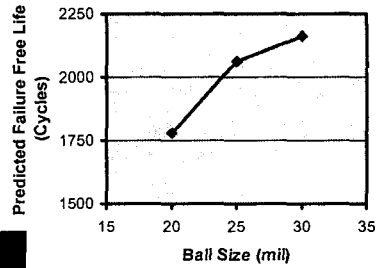  - Die Size = 11.5 mm
  - Solder Ball Size = 20 mils



ES

# hanical Reliability of Semiconductor Packages
## - PBGA, Solder ball size effect -

- **256 PBGA, 17 x 17 mm, 1.0 mm Pitch**
  - Die Size = 11.5 mm
  - Substrate : 0.36 mm Thick, 2 Layer
  - PCB : 31 Mils Thick

(graph: Predicted Failure Free Life (Cycles) vs Ball Size (mil), x-axis 15 to 35, y-axis 1500 to 2250)

30 Mils Ball
Diameter = 0.78 mm
Height = 0.70 mm

25 Mils Ball
Diameter = 0.66 mm
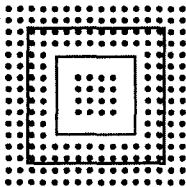Height = 0.56 mm

20 Mils Ball
Diameter = 0.56 mm
Height = 0.375

ES

**Amkor** Technology

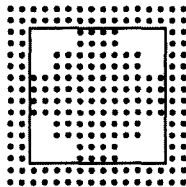© 2002 Amkor Technology Korea, Inc.

Enabling a Microelectronic World

---

# hanical Reliability of Semiconductor Packages
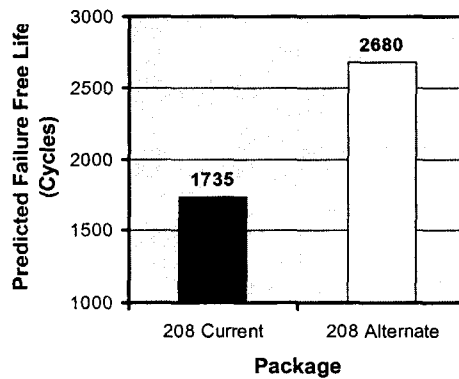## - PBGA, Ball array effect -

- **Die : 11.5 mm**
- **PCB : 31 Mil Thick**
- **Substrate : 0.36 mm**

For Die Size
< = 7 mm Sq.
Life > 2900 Cycles

For Die Size
> 7 mm Sq.

(bar chart: Predicted Failure Free Life (Cycles), 208 Current = 1735, 208 Alternate = 2680, y-axis 1000 to 3000, x-axis Package)
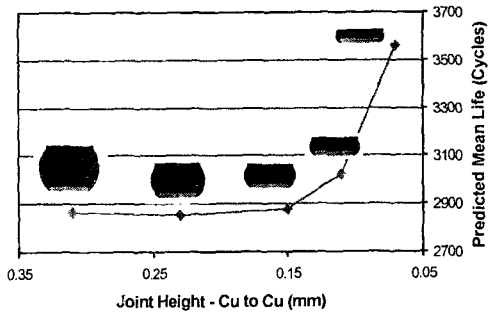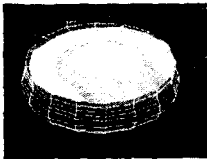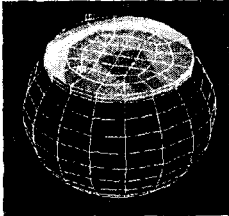
ES

**Amkor** Technology

© 2002 Amkor Technology Korea, Inc.

Enabling a Microelectronic World

92

# Mechanical Reliability of Semiconductor Packages
## - LGA & BGA -

- **Test Case: ChipArray BGA**
  - 8mm-64 Lead, 0.8mm Pitch, 3.2mm Die
  - -40 <=> 125°C, 2 cycles/hour, 0.8mm Board



*Depending on Assembly Stiffness (Thickness, Modulus, Sizes)*
*Tensile Load May Dominate Over Shear Load*

ES

 Amkor Technology    © 2002 Amkor Technology Korea, Inc.    ...ng a Microelectronic World

---

# Mechanical Reliability of Semiconductor Packages
## - SMD & NSMD -

- **SMD on Package Side**
- **NSMD on Package Side**



- 3560 Cycles
- 12,650 Cycles

- *> 3X Improvement in Life with NSMD Pad on Package Side*
  Solder Fillet on the Sides of Cu Pad Improves Reliability

ES

Amkor Technology    © 2002 Amkor Technology Korea, Inc.    ...ng a Microelectronic World

# Summary

◆ Root cause
- Thermal expansion coefficient mismatch
- Creep deformation of solder joint (shear/normal)
- Material degradation

◆ Guideline for failure prevention
- Increase of solder ball size
- Proper selection of the PCB/Substrate thickness
- Optimal design of the ball array
- Solder mask opening type : NSMD
- In some case, LGA type is better

ES

© 2002 Amkor Technology Korea, Inc.

Enabling a Microelectronic World

---

## Package characterization in Amkor

**Electrical analysis**
- R,L,C extraction
- Signal integrity
- RF design

**Mechanical analysis**
- Die cracking
- Warpage
- Interconnection failure
- Moisture induced failure
- Moldflow analysis

**Material DB**

**Thermal analysis**
- Thermal parameter
- Natural/Force convection
- Optimal design of thermal management

Methodology DB
Analysis procedure

Automation of FE Analysis

**Experimental analysis**
- 2nd Reliability test
- Thermal test
- Material Test

ES

© 2002 Amkor Technology Korea, Inc.

Enabling a Microelectronic World