GaAs PHEMT를 이용한 V-band CPW receiver chip set 설계 및 제작

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V-band CPW receiver chip set using GaAs PHEMT

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Abstract

We have designed and fabricated a low-cost, V-band CPW receiver chip set using GaAs PHEMT technology for the application of millimeter-wave wireless communication systems. Low noise amplifiers and down-converters were developed for this chip set. The fabricated low noise amplifier showed an S_{21} gain of 14.9 dB at 60 GHz and a noise figure of 4.1 dB at 52 GHz. The down-converter exhibited a high conversion gain of 2 dB at the low LO power of 0 dBm. This work demonstrates that the GaAs PHEMT technology is a viable low-cost solution for V-band applications.

Key words : Receiver, LNA, Mixer, CPW, PHEMT,

I. INTRODUCTION

Traditionally, the use of the millimeter-wave technology has been limited to military and space applications. In recent years, however, there has been an increasing interest in the commercial applications of millimeter-waves as the demand for high-speed, high-capacity wireless data transmission is growing at a great pace. 60 GHz, a V-band frequency, is gaining special importance as the choice for high speed, broadband indoor wireless LAN (Local Area Network) applications. To realize such wireless communication systems with a commercially competitive edge, the availability of compact and low-cost transceiver modules is essential, which requires MIMIC (monolithic millimeter-wave integrated circuit) technology. V-band MIMICs have been realized with InP technology, which is expensive [1-2].

In this paper, a low-cost, V-band receiver chip set has been developed using the GaAs PHEMT (Pseudomorphic High Electron Mobility Transistor) and the CPW (CoPlanar Waveguide) technology 60 GHz wireless LAN systems.

II. DESIGN OF V-BAND RECEIVER CHIP SET

GaAs PHEMTs with 0.1 ㎛ gate length have been developed to realize low noise amplifiers and down-converters. The epitaxial structure included double delta doping and AlGaAs/GaAs superlattice buffer. Fig 1 shows a cross sectional view of the device and the epi-structure of GaAs PHEMTs. The fabricated devices exhibited a transconductance of 500 mS/mm, f_{max} of 180 GHz, and f_T of 113 GHz. The PHEMT was modeled using an EEHEMT1 (EEsof scalable nonlinear HEMT Model) large signal model.

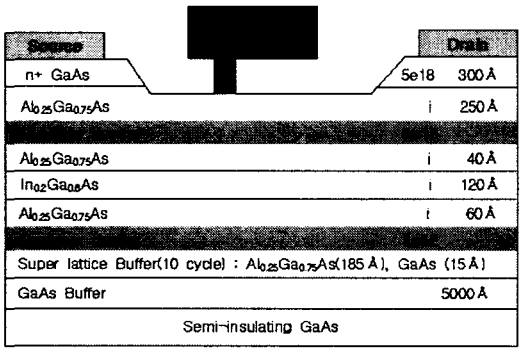

Fig 1. Device and epi-structure of GaAs PHEMT

The Low noise amplifier and down-converter were designed using the CPW technology. The CPW technology requires no backside manufacturing process during wafer fabrication, which provides easier process than the microstrip technology. Therefore, a higher fabrication yield and a lower chip cost can be expected. To construct the CPW library, we modeled discontinuity characteristics of transmission lines with various impedances including 35, 50, and 70 Ω. 600 Å NiCr resistors and 1000 Å Si_3N_4 MIM capacitors were fabricated and modeled to complete the passive library. Measured thin film resistors have 50.2-50.9 Ω/□ of resistance, and MIM capacitors have 0.485-0.538 fF/㎛^{2} of capacitance.

A. Low noise amplifier

The Low noise amplifier was designed with 50 Ω matching. A short stub was also included at the input port for the low frequency matching. Gate bias lines were designed with $\lambda/4$ short stubs, and thin film resistors were added to improve stability. Designed circuits were verified with full-wave simulation using Momentum™ for total patterns. The circuit schematic of the low noise amplifier is shown in Fig 2. Simulation result showed an S_{21} gain of 12.3 dB at 60 GHz.

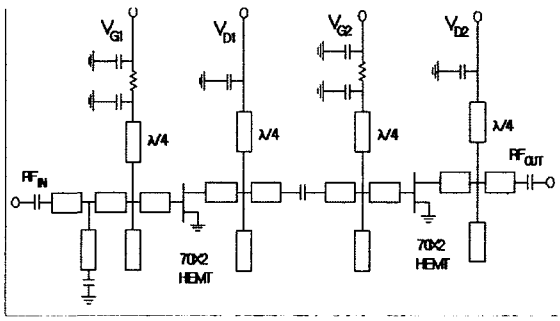

Fig 2. Circuit schematic of the low noise amplifier

B. Down-converter

The Down-converter was designed in a gate mixer structure for its high conversion gain and good RF-LO isolation characteristics. RF, LO and IF frequencies were designed to be 60.4 GHz, 58 GHz and 2.4 GHz, respectively. Matching circuits for the RF and LO ports were designed using CPW structure, while that of the IF port was designed using lumped elements such as inductors and capacitors because of its relatively low frequency. Also, we added a $\lambda/4$

open stub at the IF port to improve the LO-IF isolation characteristics by suppressing the LO power. Fig 3 shows the circuit schematic of the down-converter. Simulation result showed a conversion gain of 1.08 dB and P_{1dB} (1 dB compression point) of -6.9 dBm.

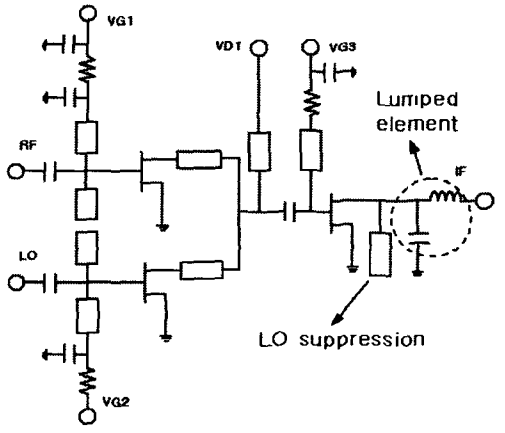

Fig 3. Circuit schematic of the down-converter

Ⅲ. FABRICATION AND MEASUREMENT

The V-band low noise amplifier and down-converter were fabricated using the standard MIMIC foundry developed at our research center, MINT (Millimeter-wave Innovation Technology research center). This foundry includes GaAs PHEMTs, CPW transmission lines, NiCr resistors and MIM capacitors [3].

A. Low noise Amplifier

Fig. 4 is a photograph of a fabricated low noise amplifier that integrated a PHEMT, resistors, capacitors, and CPW lines. The total chip area is 2.3 mm × 1.4 mm.

Fabricated low noise amplifier was first tested for gain using on-wafer small-signal S-parameter measurements. The small-signal gain and the return loss from 50 GHz to 70 GHz are presented in Fig. 5 with V_d = 1.8 V. A peak gain of 14.9 dB at 60 GHz was demonstrated. A noise parameter of 4.1 dB at 52 GHz was measured as shown in Fig. 6.

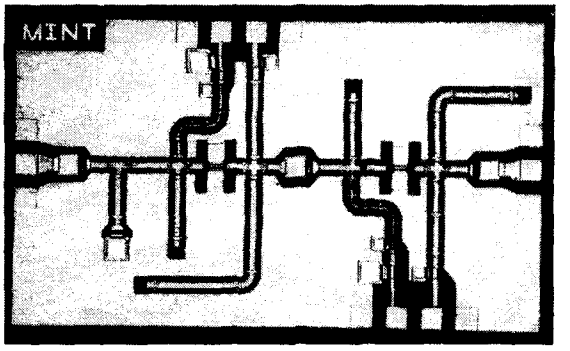

Fig 4. Photograph of the V-band low noise amplifier

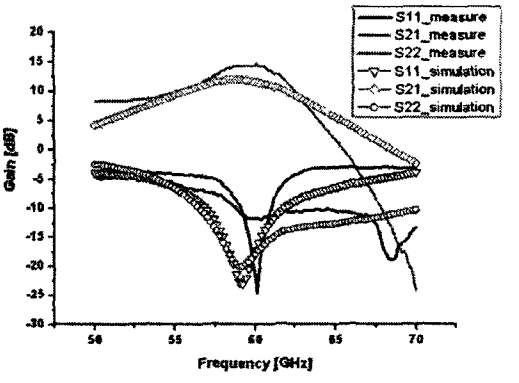

Fig 5. Gain and return loss of the low noise amplifier

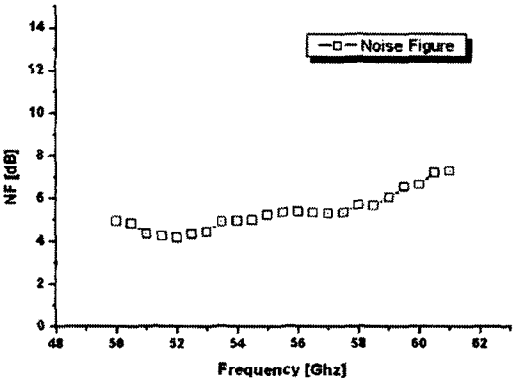

Fig 6. Noise figure of the low noise amplifier

B. Down-converter

Fig. 7 is a photograph of the fabricated down-converter. The total chip area is 1.8 mm × 1.7 mm.

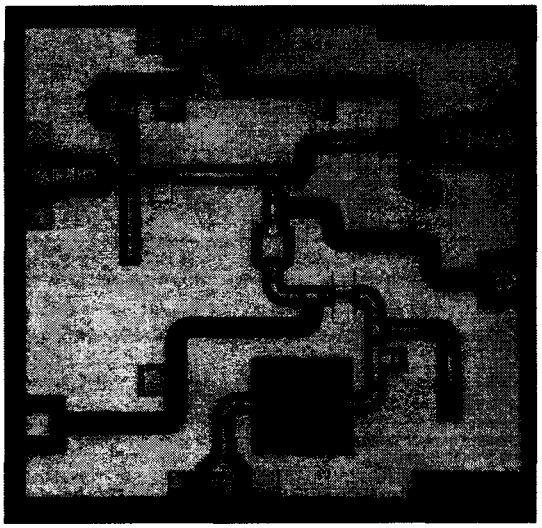

Fig 7. Photograph of the V-band down-converter

Fig. 8 to Fig. 10 shows the results of the large-signal down-converter measurement. Fig. 8 depicts conversion gain versus RF input power at 60.4 GHz for an LO power of 0 dBm at 58 GHz. Measured results demonstrated a high conversion gain of 2 dB at a low LO power of 0 dBm. Fig. 9 shows IF output power versus RF input power characteristics. The 1 dB compression point is -5.2 dBm for an RF input power of -6 dBm. Fig. 10 represents conversion gain versus RF frequency for an RF power of 12 dBm and an LO power of 0 dBm at 58 GHz. The conversion gain is 2 dB for an LO input power of 0 dBm and RF frequency within the 58.4 GHz-61.4 GHz band. The measured results of the fabricated down-converter show a good agreement with the simulation.

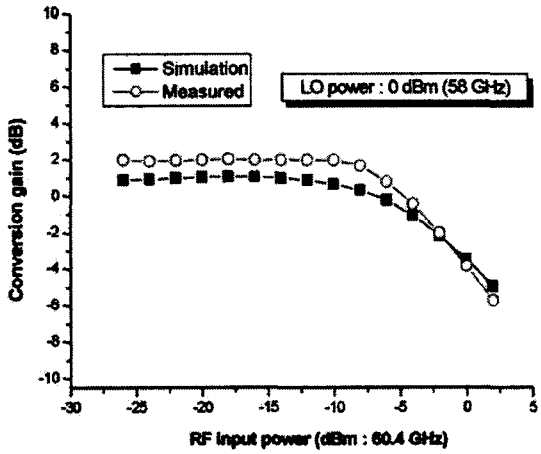

Fig 8. Conversion gain vs. RF power of the down-converter

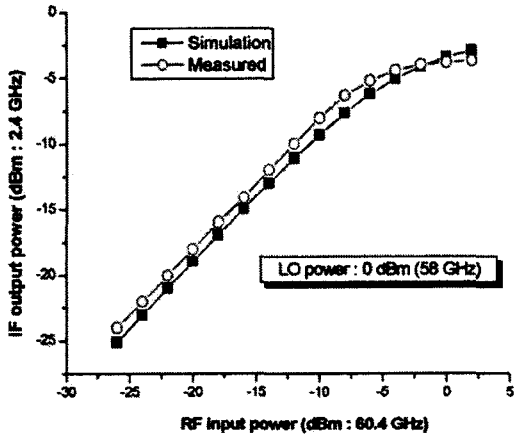

Fig 9. IF output vs. RF power of the down-converter

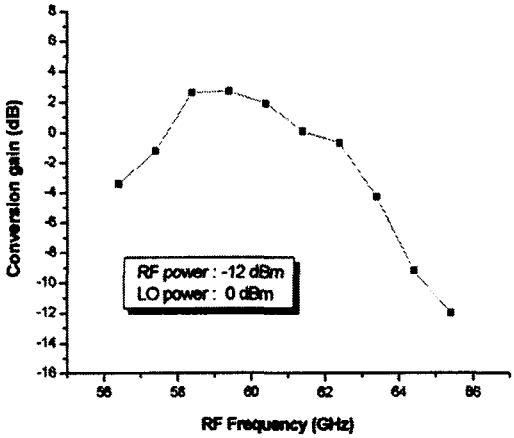

Fig 10. Conversion gain vs. RF frequency of the down-converter

IV. CONCLUSION

In this paper, we have designed and fabricated a V-band receiver chip set for the application of millimeter-wave wireless communication systems. Low noise amplifiers and down-converters were developed for the receiver chip set. For low cost, we used 0.1 ㎛ GaAs PHEMTs and CPW structures with no backside process, instead of InP devices and microstrip structures. The fabricated low noise amplifier has an S_{21} gain of 14.9 dB at 60 GHz and noise figure of 4.1 dB at 52 GHz. The fabricated down-converter demonstrated a high conversion gain of 2 dB at a low LO power of 0 dBm. This work demonstrates that the GaAs PHEMT technology is a viable low-cost solution for V-band applications.

ACKNOWLEDGEMENT

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