Design of a 2.4GHz 2 stage Low Noise Amplifier for RF Front-End In a 0.35um CMOS Technology

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Abstract

3 V, 2.46GHz Low Noise Amplifier (LNA) have been designed for standard 0.35 um CMOS process with one poly and four metal layers. This design includes on-chip biasing, matching network and multilayer spiral inductors. The single-ended amplifier provides a forward gain of 20.5dB with a noise figure 3.35dB, and an IIP3 of -6dBm while drawing 59mW total power consumption

Keywords — 2 stage LNA, CMOS, multilayer inductor.

1. Introduction

Rapid development of personal communication system has led to the development of low cost, better performing Low Noise Amplifiers. Low power consumption receivers are necessary to increase talk time of wireless communication products. The development of CMOS technology into deep submicron enables the use of such technology for implementation of GHz RF and microwave circuit [1].

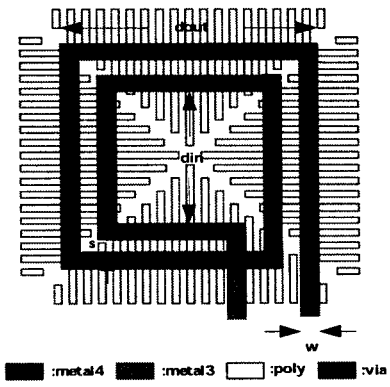
As we know, the first stage of a receiver is typically a Low Noise Amplifier (LNA), whose main function is to provide enough gain to overcome the noise of next stages. Aside from providing gain while adding as little noise as possible, an LNA should accommodate large signals without distortion, i.e. provide good linearity. The design problem is often compounded by the additional requirement that the amplifier exhibit a specified input impedance. Also, in heterodyne receivers the image rejection filter placed between the LNA and the mixer is usually realized as a passive, external component. This furthermore requires that the preceding stage, i.e., the LNA, drive 50Ω input impedance of the filter, inevitably leading to more severe trade-offs between the gain, noise figure, linearity, stability, and power dissipation in the amplifier [2].

And the monolithic spiral inductors have been used in RF ICs such as LNA, mixer, VCO, etc. The rising demand for the high quality monolithic inductors led to a significant progress in the silicon-based monolithic spiral inductor design techniques. Much of the effort has been given to the enhancement of the quality factors.

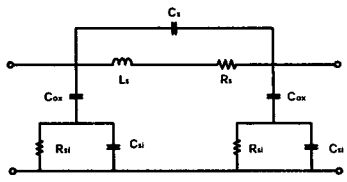
In spite of all the progress that have been made, the monolithic spiral inductors are rarely used for the consumer application RF ICs. This is because, in the consumer market, the issue of cost is the most dominating factor that determines the technologies to choose. The spiral inductors tend to be too expensive because of the amount of the die area needed. To reduce the chip area, dual layer inductors are used in 2 stage LNA structure, which results in good area efficiency and moderate quality factor [3].

2. Integrated Passive inductors.

The monolithic inductors exhibit losses at many level: i) Magnetic in the substrate (Eddy current), ii) capacitive to substrate, and iii) resistive. To reduce of these losses, this work used Pattern Ground Shield (Figure 1.a). Figure 1.b illustrates a commonly used physical model of inductor [4].



(a)



(b)

Figure 1.(a) Top view of a Shileded Inductor, (b) Physical model of an inductor

Figure 2 shows top view of a multilayer inductor. This structure is to replace the straight underpass by a second spiral coil to generate additional magnetic flux and arrives at a higher inductance value for the same inductor area and metal pitch

The contact uses an upper coil which spirals in to a center contact to lower coil which spirals out in the same sense. Magnetic flux is therefore generated at minimum wire length and thus minimum resistance but at the expense of a reduced self-resonance frequency. However, they have a higher quality factor than single layer inductors with the same inductance value [5].

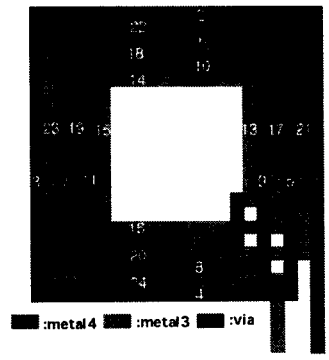


Figure 2. Multi layer inductor

In case of a single layer spiral inductor and dual layer spiral inductor Table.1 lists the

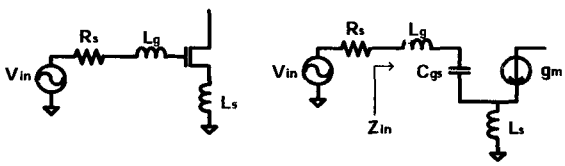
extracted component values for equivalent model shown in Figure 1.b. The multilayer inductor was provided a high inductance/area ratio. In comparison to inductors having only a single spiral coil, a multilayer inductance is achieved with a lower series resistance, but at the expense of a reduced self-resonance frequency (SFR). The application of multi layer inductances is limited to frequency, however, they have a higher quality factor than single layer inductors.

Table 1. Extracted values for inductor

	single	dual 1	dual 2
L_s (nH)	3.7	5.5	8.4
R_s (Ohm)	14	15	20
C_s (fF)	3.7	7.7	8
$C_{ox1,2}$ (fF)	150	178	130
$R_{sub1,2}$ (kOhm)	3.6	3.5	3.5
$C_{sub1,2}$ (fF)	34	97	120
area(umxum)	220x220	150x150	220x220
Quality factor (@2.46GHz)	4.5	4.5	4
SRF (GHz)	7	5.5	3.7

3. Design Approach for LNAs

Inductor degenerated common-source LNA topology allows one to simultaneously match the input impedance for both gain and noise. (Figure 3.)



(a) (b)

Figure3.Inductor-degenerated Commom source LNA : (a) topology and (b) small signal model.

Where the C_{gd} is neglected and R_s is the source impedance. The input impedance may now be expresses as

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} L_s \quad (1)$$ In

order to Z_{in} match the real-valu R_s, the conditions for this impedance matching are

$$R_s = \frac{g_m}{C_{gs}} L_s = \omega_T L_s; \quad (L_g + L_s) C_{gs} = \frac{1}{\omega_0^{\,2}} \quad (2)$$

The simplified relations were used to obtain an initial estimate of component values in the design. Assuming the device noise is dominated by the thermal noise produced by the MOSFET channel, the rms drain noise current is $\overline{i_d^{\,2}} = 4kT\gamma g_m \Delta f$, where γ=2/3 when based in the saturation region. The quality factor of the entire input network is

$$Q_{in} = \frac{1}{R_s} \frac{1}{\omega_0 C_{gs}} = \frac{1}{R_s} \omega_0 (L_g + L_s) \quad (3)$$

In the cascode LNA (Figure 5.), MOSFET M_2 has little effect on the noise figure. So, the input-referred noise figure (NF) under a matched condition can be expressed as (4)

$$NF = 1 + \gamma \frac{1}{R_s} \frac{1}{g_m} \frac{1}{Q_{in}^{\,2}} \quad (4)$$

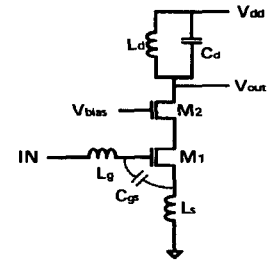


Figure 4. Cascode LNA topology.

Equation (4) shows that NF can be reduced by increasing Q_{in} . This now allows the LNA linearity to be trade-off with the noise figure for a given power consumption.

The complete circuit is shown in Figure 5. It was found that two stage amplifier is necessary to achieve the desired gain, and to provide good isolation between the input and output. The first stage is a casecode amplifier formed by MOSFET M_1, M_2. L_s and L_g are for the input matching. M_o, R_a, R_b are form of the bias circuit. L_d and C_d form a tank circuit to tune the LNA to 2.46GHz. The second stage is a common source amplifier formed of MOSFET M_3. L_{o1}, L_{o2} and C_o are for output matching. C_i is a DC blocking capacitor. R_S and R_L are 50Ω source and load resistors. All components are integrated on a single chip.

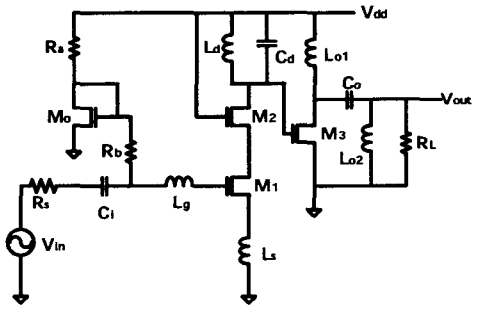


Figure 5. Completed LNA

4. Simulation and Result

Figure 6 shows voltage gain. The voltage gain is 20.5dB at 2.46GHz while the 3-dB band ranges from 2.33GHz to 2.67GHz. The Noise figure is shown in Figure 7. The simulated LNA achieves a noise figure 3.35dB at the 2.46GHz. The S-parameters of the LNA are illustrated in Figure 8. To improve the input matching, L_s should be slightly increased while L_g can be decreased to maintain the noise matching. Figure 9 shows the IIP3. The IIP3 is found to be around -6dBm by simulation. Power dissipation is about 59mW. Figure 10 shows the photograph of LNA.

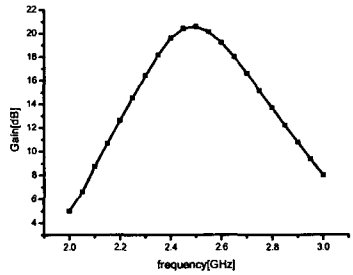


Figure 6. Voltage gain of LNA.

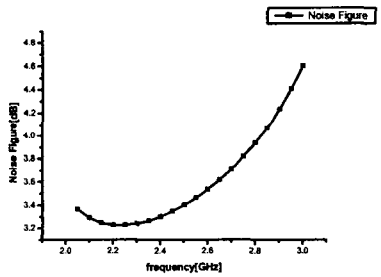


Figure 7. Noise figure of LNA.

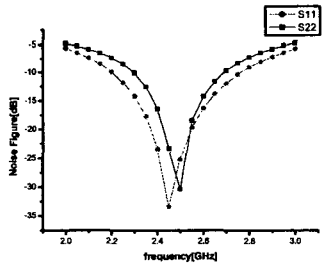


Figure 8. s-parameter of LNA.

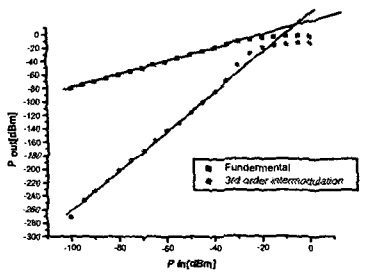


Figure 9. IIP3 of LNA.

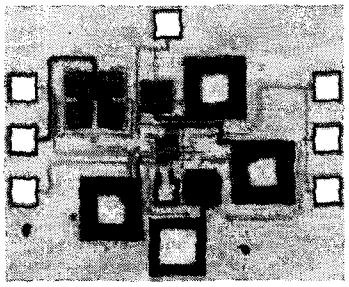


Figure 10. Photograph of LNA.

Table 2. Simulation results of LNA.

Frequency	2.46GHz
Noise Figure	3.35dB
Gain	20.5dB
IIP3	−6dBm
S11	−33dB
S22	−27dB
Supply voltage	3V
Power	59mW

5. Conclusion

A 2.46GHz LNA has been designed 0.35 um standard CMOS process. Compared with previous research result, this work shows good gain, isolation and linearity. We integrated all components in one chip. Noise figure and power consumption remains to be improved. To reduce power dissipation of LNA, we have to insert other bias circuit at second stage. The measurement is under process.

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