추아회로를 사용한 12-bit 파이프라인 A/D 변환기 설계

°김현호*, 우경환**, 이용희***, 이재영****, 이천희*****

The Design of 12-bit Pipeline A/D Converter using the Chua's Circuits

°Kim, Hyeon-ho*, Woo, Hyong-Hwan**, Lee, Yong-hui**, Yi, Jae-Young***, Yi, Cheon-hee****

Abstract

In this paper, the design of 12bit pipeline BiCMOS A/D converter presented. A BiCMOS operational amplifier and comparator suitable for use in the pipeline A/D converter. The main features is low distortion track-and-hold with 0-300MHz input bandwidth, and a proprietary 12bit multi-stage quantizer.

1. Introduction

There is an increasing interest in high-performance analog-to-digital converters for use in integrated analog and digital mixed processing systems. The realization of high-performance A/D converters typically has been limited to hybrid circuit technique.

This paper is concerned with the design of 12bit pipelined BiCMOS A/D converter using chua's circuit[1, 2, 3]. The pipeline architecture offers the potential of high throughput rate at moderate circuit complexity and cost[4].

In this paper, the design of pipeline BiCMOS A/D converter using the Chua's circuit is presented. Chua's circuit uses a current source to force a current offset in the piecewise characteristics of a Chua diode. The Chua diode consists of a negative resistance converter, two ideal diodes, and a current source. A BiCMOS operational amplifier and comparator suitable for use in the pipeline A/D converter[5]. Simulation results of the circuit blocks and the converter system are presented. The features differential analog inputs, a low distortion sample-and-hold with 0-300MHz input bandwidth, and a proprietary 12bit multi-stage quantizer. And Fabricated on 0.8um BiCMOS process.

2. Circuit description

2.1 Block diagram

The pipelining operation in the ADCs is very similar to the pipelining in digital applications. Figure 1 shows the pipelined BiCMOS block diagram used in this paper. The first stage of the ADC receives an input

* 도립충북과학대학
** 우송공업대학
*** 신성대학
**** Technical Univ. of Budapest
***** 청주대학교

signal, processes it, and feeds the analog residue to the next stage. At the same time the digital output of the comparators are sent to a register block. Then the first stage accepts another input while the next stage starts processing this residue and so on. Although shown separately, the digital to analog converter, adder and the sample hold amplifier in the stage are designed as one amplifier block.

2.2 Chua's circuit

Chua's circuit is a simple electronic network which exhibits a variety of bifurcation phenomena and attractors. The circuit consists of two capacitors, an inductor, a linear resistor, and a nonlinear resistor(called chua diode). The state equation for the circuit are as follows:

$$C1(dv_{c1}/dt) = G(v_{c2}-v_{c1}) - g(v_{c1}) \quad -----(1)$$

$$C2(dv_{c2}/dt) = G(v_{c1}-v_{c2}) + i_L \quad --------(2)$$

$$L(di_L/dt) = -v_{c2} \quad ----------(3)$$

Where G=1/R and g is a picewise-linear function defined by $g(v_R) = m_o v_R + \frac{1}{2}(m_1-m_o)[|v_R+Bp| - |v_R-Bp|]$

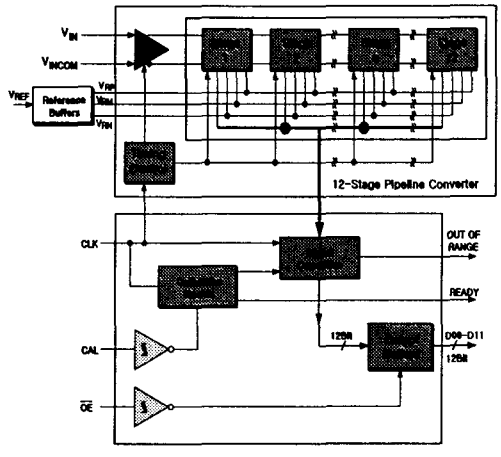
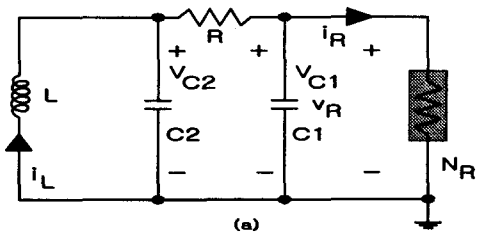


Figure 1. Pipelined BiCMOS ADC block diagram

This relation is shown in graphically in Figure 2. the slopes in the inner and outer region are m_o and m_1 respectively; $\pm Bp$ denote breakpoints. The nonlinear resistor N_R is termed voltage-controlled because the current in the element is a function of the voltage across its terminals.

The *i-v* characteristic of a voltage-controlled nonlinear resistor may be offset along the i-axis by adding a current source in parallel with the element (Figure 2(a), (b)). Realization of Chua's circuit using a current-offset Chua diode is shown in Figure 2(c). The desired nonlinear resistor characteristic is obtained by connecting in parallel a negative impedance converter N_{R1}, two ideal diodes(N_{R2} and N_{R3}), and a current source(N_{R4}) resistance. A negative resistance converter N_{R1}(A_1,R_1,R_2, and R_3)is used to produce the underlying negative resistance. Connected in parallel with the negative impedance converter are two ideal diodes(A_2,R_4,D_1) and (A_3,R_8 ,D_2) with dc offsets set by V+, R_5, and R_6, and V-, R_9, and R_{10}. Respectively. These connect a positive resistance R_7 in parallel with the negative resistor N_{R1} whenever the voltage V_R exceeds the breakpoints BP- and BP+ in magnitude. N_{R4} supplies the desired dc offset current I_{os}. This architecture allow one to control independently the slopes, breakpoints, and current offset of the Chua diode's *i-v* characteristic.



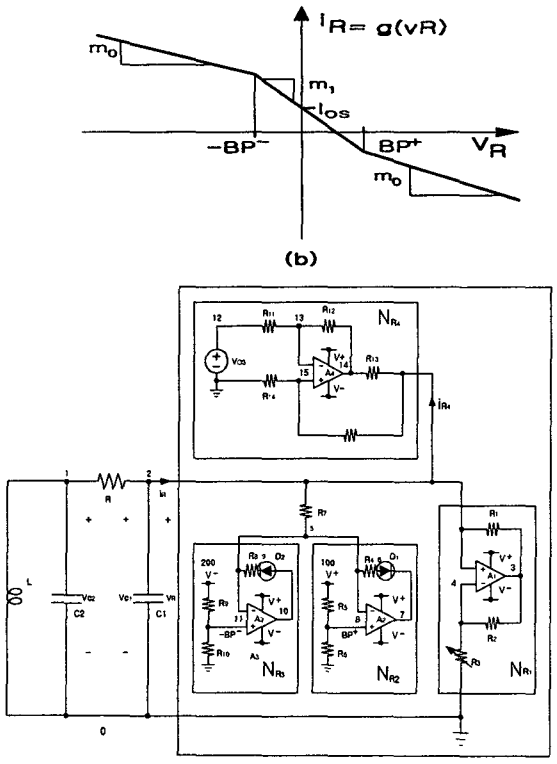


Figure 2. (a)A current source Ios in parallel with the nonlinear resistor, (b)A current offset in the i-v characteristic, (c) Realization of Chua's circuit.(c)

3. Simulation Results

Simulation results are first presented for the individual circuit blocks used to synthesize the pipeline A/D converter. Basic circuit simulations were performed with HSPICE in SUN system.

3.1 BiCMOS Pipeline A/D Converter

The entire switched-capacitor BiCMOS pipelined A/D converter presents a formidable simulation task from a circuit level. The accuracy of the pipeline converter is determined primarily by the first few stages. As a result, placing focus on the first two stages provides most of the information that is sought from the simulation.

This section presents the simulation results of the first two stages in the pipeline A/D converter. The first stage employs a sample-and-hold switched-capacitor amplifier, an offset cancelled pre-amplifier system and a latch. The second stage employs a multiply-by-two switched-capacitor amplifier, an offset cancelled pre-amplifier system and a latch.

The simulation presented in this section uses a large differential input signal, namely 5 V. Mismatches in the circuit blocks are not included in this case. In Figure 3, the analog output of the sample-and-hold is shown. Notice that the output alternately settles from 5 V and then to 0 V when reset. Figure 4 shows the analog output for the multiply-by-two. Since the pipeline input is 5 V, the sample-and-hold out is 5 V. Figures. 5 and Figure 6 show the digital outputs of the sample-and-hold and multiply-by-two stages, respectively. Detailed examination of the analog outputs reveals that this pipeline operates with 12-bit accuracy for a 10 V full scale. The clocks for the sample-and-hold analog system are shown in Figure 7. These clocks correctly sequence the switched-capacitor sample-and-hold function. the sample-and-hold digital system clocks are shown in Figure 8.

These clocks correctly sequence the latch function in this stage. The period of the clocks is 190ns. Thus, the throughput of this pipeline is about 5.2 MHz. The clock timing allocates 50 ns for op-amp and pre-amp

settling. A substantial amount of time is needed for the clock waveforms to slew. Additional time is allocated to assure non-overlapping clocks. Thus, the total overhead amounts to 90ns. Less conservative clock timing for 6.25 MHz throughput rate was successful in maintaining more than 12 bit of accuracy.

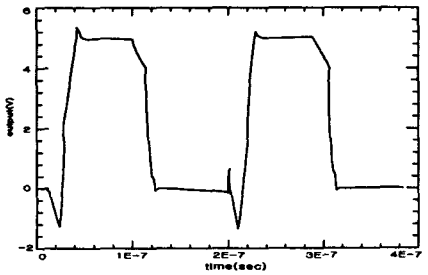


Figure 3. Sample-and-hold analog output

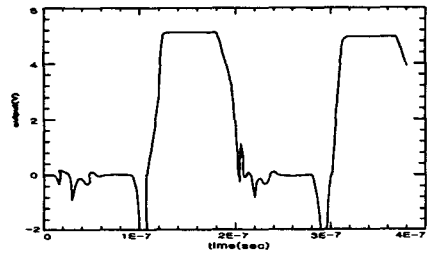


Figure 4. Multiply-by-two analog output

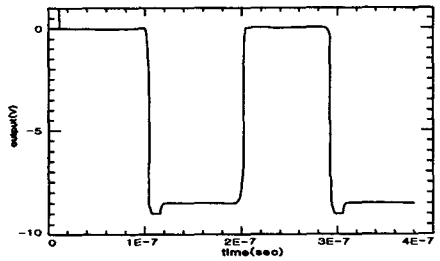


Figure 5. Sample-and-hold digital output

And Figure 9, 10, 11 show the DC characteristics of DNL, ILL and SNR. DNL (Differential Non- Linearity) is measure of the maximum deviation from the ideal step size of 1 LSB. Measured DNL is ±0.30LSB (SPEC:± 0.65LSB). INL(Integral-Non-Linearity) is a

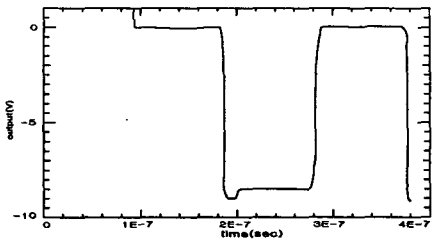


Figure 6. Multiply-by-two digital output

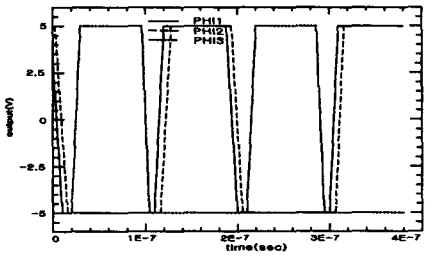


Figure 7. Sample-and-hold analog system clocks

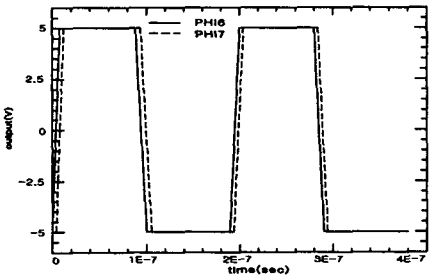


Figure 8. Sample-and-hold digital system clocks

measure of the deviation of each individual code from a line drawn from negative full scale(1/2 LSB below the first code transition) through positive full scale. The deviation of any given code from this straight line is measured from the center of that code value. Measured INL is ±0.52LSB(SPEC:±1.15LSB).

Finally, SNR(Signal to Noise Ratio) is the ratio of the rms value of the input signal to the rms value of the other spectral components below one-half the sampling frequency. Measured SNR is 66dBFS at Fin= 24.5MHz, and SFDR is 74dBc at Fin=24.5 MHz. And fabricated final chip top view is represented as shown in Figure 12.

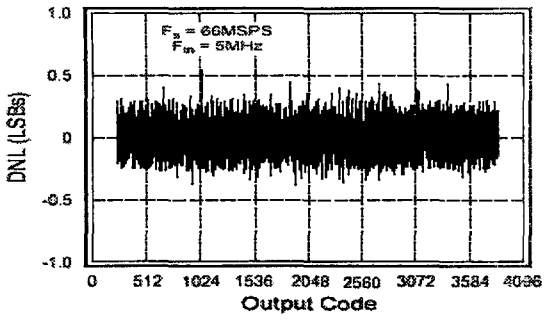


Figure 11. Differential Non-linearity

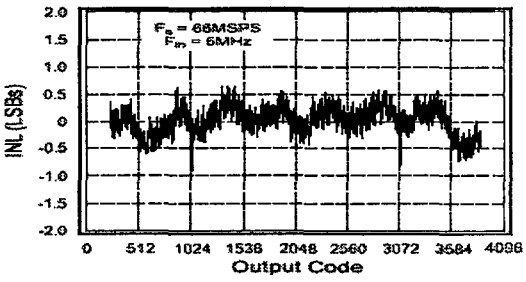


Figure 12. Integral Non-linearity

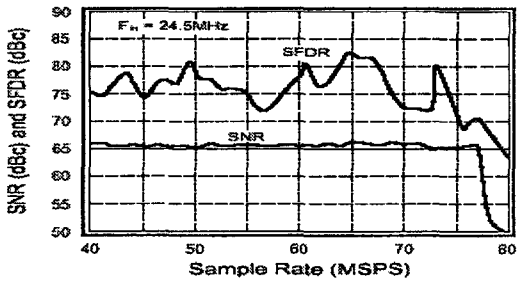


Figure 13. SNR and SFDR vs sample rate

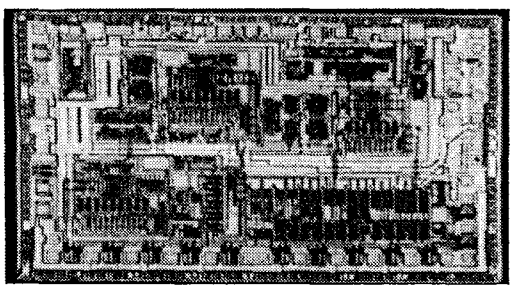


Figure 14. Fabricated final chip top view

4. Conclusion

In this paper, the design of 12-bit pipeline BiCMOS A/D converter is presented. The operational amplifier design has emphasized dynamic response as this circuit primarily determines the throughput of the pipeline A/D converter. A novel comparator pre-amplifier design used in an open loop offset cancelled comparator has been presented. Simulations have indicated a pipeline throughput of greater than 5 MHz for a 10 V full scale. A high frequency, fully differential BiCMOS operational amplifier has been designed, fabricated and tested. Measured DNL = ± 0.30LSB, INL=±0.52LSB, SNR=66dBFS at Fin =24.5MHz, and SFDR=74dBc at Fin=24.5MHz. The performance measures indicate that this BiCMOS op-amp is suitable for high-performance applications.

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