An IC Chip of a Cell-Network Type Circuit Constructed with 1-Dimensional Chaos Circuits

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Abstract: In this paper, an IC chip of a cell-network type circuit constructed with 1-dimensional chaos circuits is reported. The circuit is designed by using switched-current (SI) techniques. In the proposed circuit, by controlling connections of cells, an S-dimensional circuit ($S = 1, 2, 3, \dots$) and a synchronization system can be constructed easily. Furthermore, in spite of faults of a few cells, the circuit can reconstruct above-mentioned systems only to change connections of cells. This feature will open up new vista for engineering applications which are used in a distance place such as space, deep sea, etc. since it is difficult to repair faults of these application systems. To investigate the characteristics of the circuit, SPICE simulations are performed. The VLSI chip is fabricated from the layout design using a CAD tool, MAGIC. The proposed circuit is integrable by a standard 1.2 μm CMOS technology.

1. Introduction

A chaos circuit is one of the most efficient tools for the experimental observation of chaos. Among others, high-dimensional chaos circuits are useful as an experimental tool since they can demonstrate more various bifurcation modes than 1-dimensional chaos circuits. For this reason, several high-dimensional chaos circuits have already been proposed [1]-[4]. For example, Delgado-Restituto et al. realized Chua's chaos circuit by using CMOS technologies [1] and Saito et al. realized hysteresis chaos generator [2]. Most of these chaos circuits are analog chaos circuits generating 2 or 3-dimensional chaotic signals. Although high-dimensional chaotic signals can be generated by these continuous-time chaos circuits, we design a high-dimensional chaos circuit by using arrayed discrete-time chaos circuits. Different from continuous-time chaos circuits, the discrete-time chaos circuit which is a portion of the proposed circuit can be realized in a 1-dimensional form. Compared with the continuous-time chaos circuits, the chaotic behavior of the 1-dimensional chaos circuits is simple. Therefore, not only the proposed circuit can achieve a simple structure, but the chaotic behavior of the 1-dimensional chaos circuits can be analyzed easily. These features help us to detect the fault of the building blocks.

In this paper, an IC chip of a cell-network type circuit constructed with 1-dimensional chaos circuits is reported. The circuit is designed by using switched-current (SI) techniques. In the proposed circuit, by controlling connections of cells, an S-dimensional circuit ($S = 1, 2, 3, \dots$) and a synchronization system [5] can be constructed easily. Furthermore, in spite of faults of a few cells, the circuit can reconstruct above-mentioned systems only to change connections of cells. This feature will open up new vista for engineering applications which are used in a distance place such as space, deep sea, etc. since it is difficult to repair faults of these application systems. To investigate the characteristics of the circuit, SPICE simulations are performed. From the layout design using a CAD tool, MAGIC, the VLSI chip is fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo with the collaboration by On-Semiconductor.

2. Circuit Structure

Figure 1 shows an architecture of the proposed circuit. The circuit consists of M ($M \geq 2$) chaos circuits called cell circuits. When the connections to other cells are closed, the dynamics of p-th cell circuit is expressed by

$$\mathrm{F}({}^p\mathrm{X}(t)) = 1 - A|{}^p\mathrm{X}(t)|. \quad (1)$$

In Eq.(1), A is a non-negative parameter. Figure 2 shows a cell circuit designed by using switched-current (SI) techniques. A current-mode technique is suitable for integration of cell networks since it can easily realize summation and multiplication by a wired-sum connection and a loop connection, respectively. In Fig.2, the parameter A in Eq.(1) is realized by the copying-ratios of current mirrors. The unit delay in Eq.(1) is realized by an SI track & hold circuit shown in Fig.2. Since the

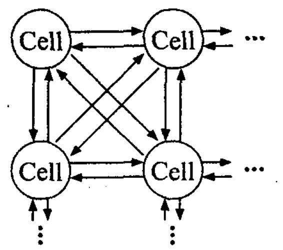


Fig.1 Architecture of the proposed circuit.

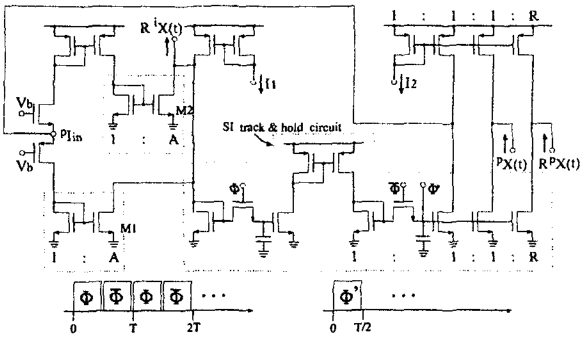


Fig.2 Cell circuit designed by SI techniques.

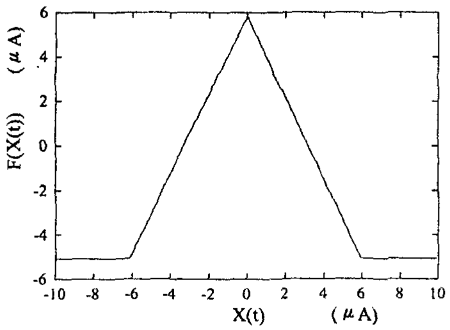


Fig.3 Nonlinear function of the cell circuit when $A = 1.625$.

SI track & hold circuit cannot achieve 2-quadrant operation, the unity constant in Eq.(1) is realized by $I_1 - I_2$.

By connecting S cell circuits, an S-dimensional chaos circuit can be constructed. The dynamics of S-dimensional chaos circuit is given by

$$\begin{aligned} {}^{p}X(t+1) &= F({}^{p}X(t)) - \sum_{\{i|\ i \neq p\}} R\ {}^{i}X(t), \\ &= 1 - A|{}^{p}X(t)| \\ &\quad - \sum_{\{i|\ i \neq p\}} R\ {}^{i}X(t), \end{aligned} \tag{2}$$

where $F(\cdot)$ is an output of the p-th cell circuit and R is a damping factor which satisfies $0 \leq R < 1$. In the high-dimensional case, the current source I_1 is set to satisfy

$$F({}^{p}X(t)) - \sum_{\{i|\ i \neq p\}} R\ {}^{i}X(t) \geq 0.$$

The long-working life is achieved by closing the connection to fault cell circuits. The connection to other cells can be closed by setting $I_2 = 0$ and $\overline{\phi} = 0$.

3. Simulation

To confirm the validity of circuit design, SPICE simulations were performed. The SPICE simulations were performed under the conditions that $V_{dd} = 5V$, $V_b = 2.5V$, $I_1 = 10\mu A$, $I_2 = 5\mu A$, and $R = 0.5$.

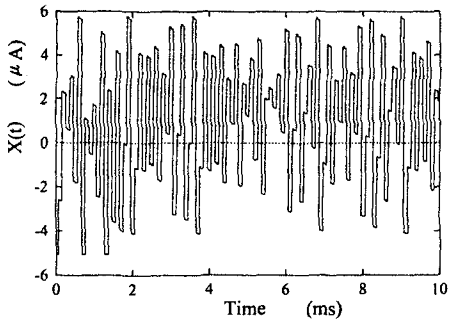


Fig.4 Chaotic signal of the cell circuit when $A = 1.625$

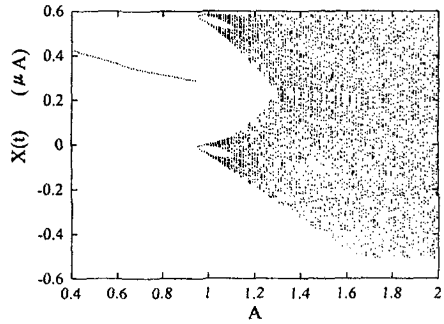


Fig.5 Bifurcation diagram of the cell circuit.

Figure 3 shows a nonlinear function of the cell circuit. In Fig.3, the region which satisfy $F'(X(t)) \neq 0$ is determined by the current sources I_1 and I_2. Figure 4 shows an example of chaotic signals of the cell circuit when A=1.625. The parameter A is determined by controlling the size of MOSFET's, M1 and M2 (see in Fig.2). Figure 5 shows the bifurcation diagram of cell circuit. The period-n orbits ($n = 1, 2, \ldots$) in Fig.5 are stable fixed-points. The fixed points denoted by $X_{qj}(t)$ ($j = 1, 2, \ldots, s$) can be obtained by the following equations:

$$\begin{aligned} X_{q1}(t) &= F^{(n)}(X_{q1}(t)), \\ X_{q2}(t) &= F^{(n)}(X_{q2}(t)), \\ &\cdots \\ X_{qs}(t) &= F^{(n)}(X_{qs}(t)), \end{aligned} \tag{3}$$

where $F^{(n)}(\cdot)$ is the nonlinear function which is defined by

$$F^{(n)}(X(t)) \triangleq \overbrace{F(F(\cdots F(X(t))\cdots))}^{n}. \tag{4}$$

Among those, the fixed points which satisfy the following condition are the period-n orbits.

$$\left|\frac{dF^{(n)}(X_{qj}(t))}{dX(t)}\right| < 1. \tag{5}$$

For example, the period-1 orbit in *ideal* bifurcation diagram of the cell circuit is expressed by

$$X_{q1}(t) = \frac{I_1 - I_2}{1 + A} \qquad (0 < A < 1). \tag{6}$$

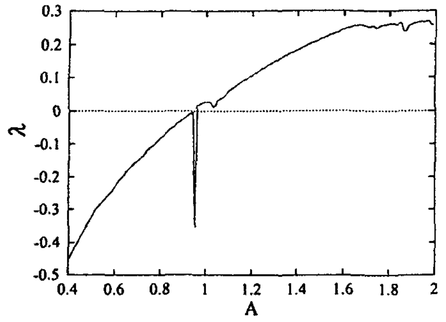


Fig.6 Lyapunov exponent for the bifurcation diagram of Fig.5.

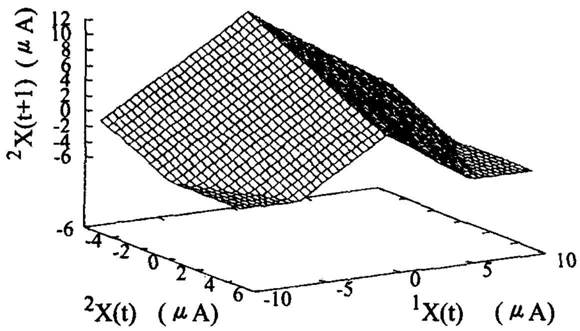


Fig.7 Nonlinear function of the 2-dimensional chaos circuit.

In the bifurcation diagram, the upper edge of the chaotic region for X(t), X$_u(t)$, is given by the top of tent-type map F$(\cdot)$. On the other hand, the lower edge of the chaotic region, X$_l(t)$, is determined by X$_u(t)$. The X$_l(t)$ is given by

$$\mathrm{X}_l(t) = \mathrm{F}(\mathrm{X}_u(t)). \quad (7)$$

From Eqs.(1) and (7), X$_u(t)$ and X$_l(t)$ of *ideal* bifurcation diagram are given by

$$\mathrm{X}_u(t) = \mathrm{I}_1 - \mathrm{I}_2 \quad (8)$$

and

$$\mathrm{X}_l(t) = \mathrm{I}_1 - \mathrm{I}_2 - A, \quad (9)$$

respectively.

Figure 6 shows the Lyapunov exponent for the bifurcation diagram of Fig.5. The Lyapunov exponent is defined by

$$\lambda = \frac{1}{M}\sum_{t=0}^{M-1} \log|\mathrm{F}'({}^p\mathrm{X}(t))|, \quad (10)$$

where

$$\mathrm{F}'({}^p\mathrm{X}(t)) \triangleq d\mathrm{F}({}^p\mathrm{X}(t))/d\,\mathrm{X}(t).$$

In Eq.(10), the parameter M was set to 100,000.

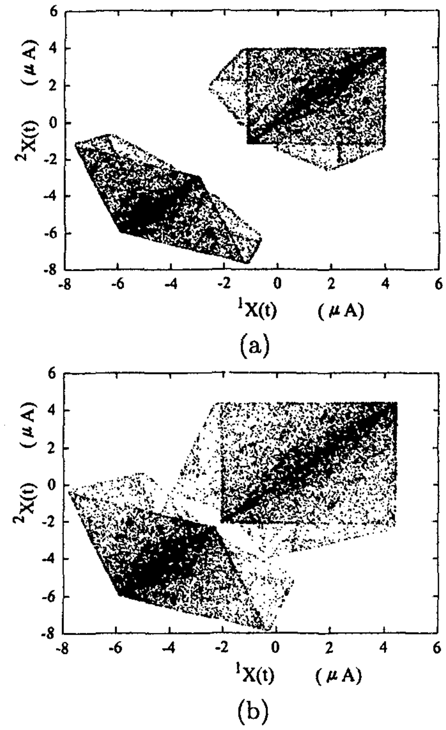


Fig.8 Strange attractors generated from 2-dimensional chaos circuit. (a) A =1.1875. (b) A =1.25.

As an example of high-dimensional circuits, 2-dimensional chaos circuit was constructed by connecting the terminal R ^{p}X(t) to the terminal R ^{i}X(t) of the other circuit. The dynamics of 2-dimensional chaos circuit is given by

$$\begin{aligned} {}^1\mathrm{X}(t+1) &= 1 - {}^1A|{}^1\mathrm{X}(t)| - \mathrm{R}\,{}^2\mathrm{X}(t), \\ {}^2\mathrm{X}(t+1) &= 1 - {}^2A|{}^2\mathrm{X}(t)| - \mathrm{R}\,{}^1\mathrm{X}(t). \end{aligned} \quad (11)$$

Figure 7 shows a nonlinear functions of the coupled cell circuits. Figure 8 shows strange attractors when A=1.1875 and A=1.25. As Fig.8 shows, the proposed circuit can demonstrate various bifurcation modes by controlling the parameter A.

By connecting the terminal R ^{p}X(t) to the terminal ^{p}I$_{\mathrm{in}}$ of the other circuit, chaos synchronization phenomena can be observed. The dynamics of mutually-coupled cell circuit is given by

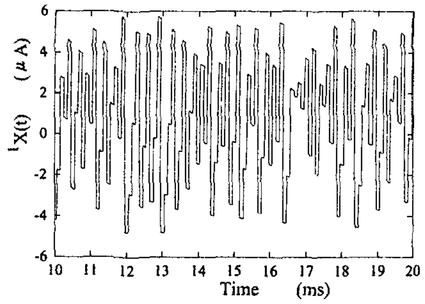
$$\begin{aligned} {}^1\mathrm{X}(t+1) &= 1 - {}^1A|{}^1\mathrm{X}(t) + \mathrm{R}\,{}^2\mathrm{X}(t)|, \\ {}^2\mathrm{X}(t+1) &= 1 - {}^2A|{}^2\mathrm{X}(t) + \mathrm{R}\,{}^1\mathrm{X}(t)|. \end{aligned} \quad (12)$$

The condition for chaos synchronization can be derived from

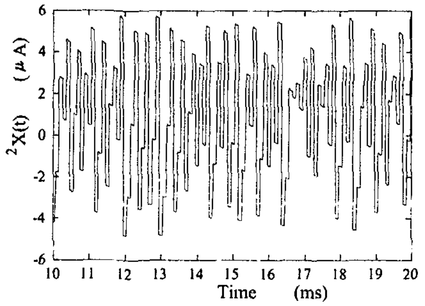
$$\left|\frac{d\mathrm{Y}(t+1)}{d\mathrm{Y}(t)}\right| < 1, \quad (13)$$

where Y$(t) = {}^1$X$(t) - {}^2$X(t). From Eq.(13), the condition for chaos synchronization is given by

$$\frac{A-1}{A} < \mathrm{R}. \quad (14)$$



(a)



(b)

Fig.9 Chaotic signals of mutually-coupled cell circuits. (a) ${}^1X(t)$. (b) ${}^2X(t)$.

Figure 9 shows chaotic signals of the cell circuits. As Fig.9 shows, the mutually-coupled cell circuits are synchronized with each other.

4. IC Implementation

To fabricate the VLSI chip, the layout of the proposed circuit was performed by using an analog CAD tool, MAGIC. Figure 10 shows the photograph of the fabricated IC. The VLSI chip shown in Fig.10 was fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo with the collaboration by On-Semiconductor. The size of the fabricated IC designed by a 1.2 μm CMOS process is $2.3mm \times 2.3mm$. The VLSI chip shown in Fig.10 includes 17 cell circuits. The size of a cell circuit is $520\mu m \times 355\mu m$.

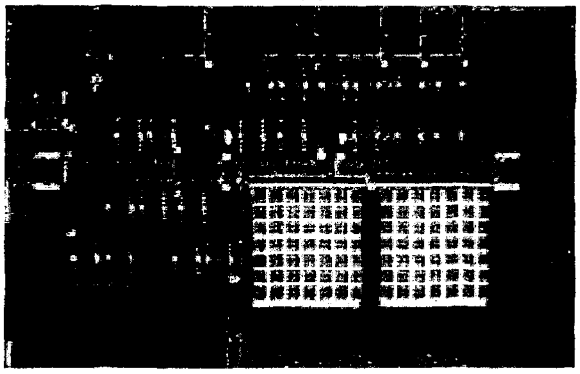
5. Conclusion

An IC chip of a cell-network type circuit constructed with 1-dimensional chaos circuits has been proposed in this paper.

The SPICE simulations showed the following results: 1. Not only S-dimensional chaotic signals, but chaos synchronization phenomena can be observed by changing the connections of cell circuits. 2. The proposed circuit is implementable by a standard CMOS technology.

The theoretical analysis for high-dimensional chaos circuits is left to the future study.

(a)



(b)

Fig.10 Photograph of the fabricated IC. (a) Total view. (b) Cell circuit.

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