Testability of Current Testing for Open Faults Undetected by Functional Testing in TTL Combinational Circuits

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Abstract: A new test approach based on a supply current test method is proposed for testing open faults in bipolar logic circuits. In the approach, only the open faults are detected by the supply current test method, which are difficult to be detected by functional test methods. The effectiveness of the approach is examined experimentally on open fault detection in TTL combinational circuits. The results shows that higher fault coverage can be established by applying a small number of test input vectors of the supply current test method after test vectors of functional test methods based on stuck-at models.

1. Introduction

It has been shown that quiescent supply current tests of logic circuits are indispensable for realizing high reliable logic systems[1,2,3]. Especially, IDDQ testing is very effective in CMOS logic IC tests. Also, test input generation algorithms for the IDDQ testing have been proposed. In a fault-free CMOS IC, very small quiescent supply current will be generated in operation. If large quiescent supply current is generated, the circuit can be determined as faulty. The IDDQ testing can detect physical defects, which can not be modeled as logical faults and is effective for realizing high reliable systems.

Besides CMOS ICs, bipolar circuits, like TTL and ECL circuits, are often used now for implementing logical systems. Especially, they are used in the electronic equipments which require a high speed operation, and are used as a core in logic system. If they do not work, the generated damage will be extremely large. Thus, very high reliability is requested for bipolar circuits.

Quiescent supply current of unfaulty bipolar gates depends on the output logic values[3]. Thus, even if any defects do not occur in a bipolar circuit, quiescent supply current flows from the VCC terminal to the GND terminal. It means that IDDQ test technique is not applicable to fault detection problems of bipolar circuits.

In order to detect faults in bipolar circuits with their quiescent supply currents, a new fault detection method should be developed. Thus, in the past, we proposed a supply current test method for bipolar circuits[3]. The method is to detect faults by measuring the quiescent supply current of a circuit under test and comparing it with the unfaulty circuit. Also, we proposed a fast random test input generation method for the supply current tests and an algorithmic one in [4] and [5], respectively.

There are some variations in the quiescent supply current of each gate in implemented logic circuits. Thus, we proposed a test method which is applicable even if there are some variations among gates[6]. Practical fault coverage of the supply current test method is examined for open faults in TTL combinational circuits[8], since open faults often occur in logic circuits fabricated with the state-of-art technology. The results show that more open faults can be detected by the supply current test method than functional ones based on stack-at fault models. It stems that functional test methods require to propagate the faulty effect generated by fault excitation to some primary output terminals but the supply current test method does not need to do.

On the other hand, it takes large time for quiescent supply current to appear. It means that it takes long time to detect all of the open faults in a circuit only by the supply current test method. Thus, we think from the practical point of view that our test method should be used for detecting only the open faults which are difficult to be detected by functional tests.

In this paper, the testability of the faults undetected by functional tests based on stuck-at fault models is examined in an ISCAS-85 benchmark circuit. Our supply current test method is described in section 2. After that, executed experiments and the obtained results are described in section 3.

2. Supply Current Test for TTL Circuits

The Quiescent supply current $I_{CCN}(Tj)$ of an unfaulty TTL circuit made of Ns gates which flows when the j-th test input vector is applied to the circuit, can be defined by Eq.(1).

$$I_{CCQN}(T_j) = \sum_{i=1}^{Ns} I_{CCQNi}(T_j) \quad (1)$$

where $I_{CCQNi}(T_j)$ is the quiescent supply current of the i-th TTL gate generated when T_j is provided to the unfaulty circuit. Also, quiescent supply current $I_{CCQC}(T_j)$ of a circut under test(CUT) can be defined by Eq.(2).

$$I_{CCQC}(T_j) = \sum_{i=1}^{Ns} I_{CCQCi}(T_j) \quad (2)$$

where $I_{CCQCi}(T_j)$ is the quiescent supply current of the i-th TTL gate in the CUT generated by the T_j application.

If Eq.(3) *is satisfied, the CUT is determined as faulty.*

$$\Delta I_{CCQ}(T_j) \geq I_{th} \quad (3)$$

where $\Delta I_{DDQ}(T_j)$ is defined by Eq.(4) and I_{th} is the threshold value to determine whether the CUT is faulty or not.

$$\Delta I_{CCQ}(T_j) = | I_{DDQC}(T_j) - I_{DDQN}(T_j) | \quad (4)$$

Quiescent supply current of unfaulty TTL gates depends on the output logic values[3]. In this paper, it is assumed that quiescnet supply currents I_{iL} and I_{iH} flow in the i-th TTL gate when the output logic value is L and when it is H, respectively.

When an open fault is excited by the test input vector Tj, any large quiescent supply current change will not be generated in the gate having the open fault at the output signal line. Thus, $\Delta I_{DDQ}(T_j)$ is defined by the supply current changes of gates whose output logic values are changed by the fault propagation. A set of the gates is called *Sg* in this paper. $\Delta I_{DDQ}(T_j)$ can be obtained by Eq.(5).

$$\Delta I_{CCQ}(T_j) = \sum_{i \in Sg} \Delta I_i(T_j) \quad (5)$$

where $\Delta I_i(T_j)$ is quiescent supply current change of the i-th gate which is generated when T_j is provided to the circuit and is defined by Eq.(6).

$$\Delta I_i(T_j) = \begin{cases} I_{iL} - I_{iH}, & \text{the output of the i-th gate is changed from H to L} \\ I_{iH} - I_{iL}, & \text{the output of the i-th gate is changed from L to H} \end{cases} \quad (6)$$

There are some variations in quiescent supply current among ICs. The generation process is modeled as a Gaussian distribution process $N(\mu_{Ni}(T_j), \sigma(T_j)^2)$, where $\mu_{Ni}(T_j)$ and $\sigma(T_j)^2$ are the mean value and the variance of quiescent supply current in the i-th gate which flows when a test input vector (T_j) is provided to the CUT.

Supply current of logic circuits made of TTL gates can be modeled as a Gaussian distribution. From the current and the specified variation, a Gaussian distribution can be derived. Examples of the distributions for an unfaulty circuit and the fault one are shown in Figure 1. By the variation generated in IC productions, $I_{CCQN}(T_j)$ and $I_{CCQC}(T_j)$ will not be defined as values and faults can not be detected by using Eq.(3). The supply currents can be defined by means of distribution functions.

If the distributions of $I_{DDQN}(T_j)$ and $I_{DDQC}(T_j)$ are separated each other, the faults can be detected. Otherwise, they are not detected. However, if they are overlapped with small probability, in our test method, it is determined that the fault can be detected. Thus, the statistical analysis method with level of significance(α) is used in our test method. That is, fault is detected with α, which is used for judging whether any two distributions are separated each other like in [6]. Test input vectors of our test method can be generated so that the distribution of quiescent supply current of the faulty circuit can be separated to the unfaulty one as shown in Figure 1[6].

This test method is based on quiescent supply current. Whenever a test input vector is provided to a CUT, dynamic supply current will appear. After the dynamic supply current disappear, quiescent supply current will appear. Thus, test speed of the supply current test method is slower than functional test methods based on stuck-at fault models, since output logic values can appear before quiescent supply current appears. However, there are many faults which are easier to be detected by the supply current test method than the functional ones, since faulty effects generated by excitation need not always to be propagated to any primary output terminals. Therefore, we propose to use the supply current test methods for detecting open faults which can not be detected by the functional test methods, as shown in Figure 2.

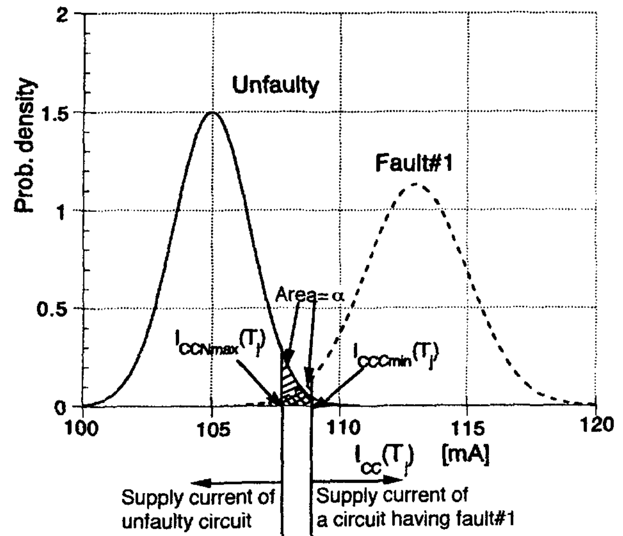


Figure 1. Fault detection with level of significance

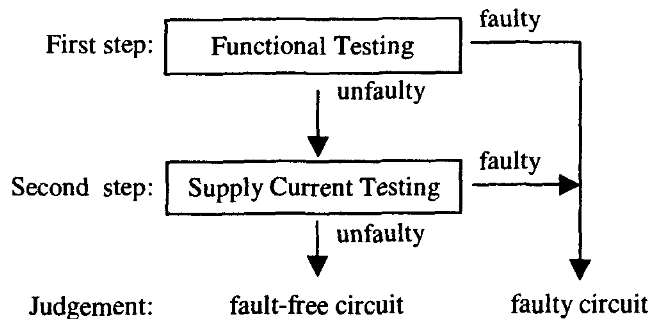


Figure 2. Our test method.

3. Experimental Evaluation

In order to evaluate testablity of the test method in Figure 2, we evaluated fault coverage of open faults in TTL circuits by generating test input vectors for an ISCAS-85 benchmark circuit made of TTL-LS SSIs with α =0.1.

In our experiments, test input vectors for the functional test method are derived by a random test input generation method which is almost the same as in [4]. If any open faults can not be detected by the last 50 vectors generated by random numbers, the test input generation process is terminated. After that, test input vectors for the supply current test method are generated to detect open faults which are not be detected by functional test methods. In the

past, we proposed a random test generation algorithm and a deterministic one for the supply current test method. In our experiments, the deterministic algorithm is used which is modified so that the criterion for judging whether T_j can be selected as a test input vector can be based on the variance of supply current of each SSI.

Test input generation process using the algorithm is as follows. Output logic value of each gate is determined by the determisitic algorithm in [5]. From the output logic value of each gate, the supply current of the circuit is calculated by the method in [7]. From the current and specified variation(σ), a Gaussian distribution is derived, whose example is shown in Figure 1. As shown in Figure 1, if the distribution of quiescent supply current of a faulty circuit can be separated to the unfaulty one by specifying α, the vector is employed as a test input vector for detecting the fault.

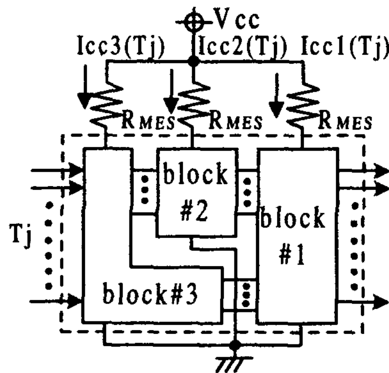


Figure 3. Supply current measurement methods.

Table 1. Circuit under test, C432.

Primary inputs	36
Primary outputs	7
Signal lines	488
SSIs	60
Circuit blocks	2

C432 is used as a CUT. Before testing, technology mapping is performed, that is, it is determined which gate in SSIs is used for each gate in the CUT[8]. The results are shown in Table 1. As shown in Table 1, the number of SSIs in the CUT is *60*. Usually, circuits having such a large number of SSIs will not be fabricated on printed boards. However, since it can be used for evaluating the applicability of the supply current testing to TTL circuits, the CUT is used in our experiments.

Supply current of the CUT is measured at the supply voltage terminal. Usually, the current is measured as voltage by means of an I-V transformer, which can be modeled as a resistor. In our experiments, the resistance is assumed as 1Ω.

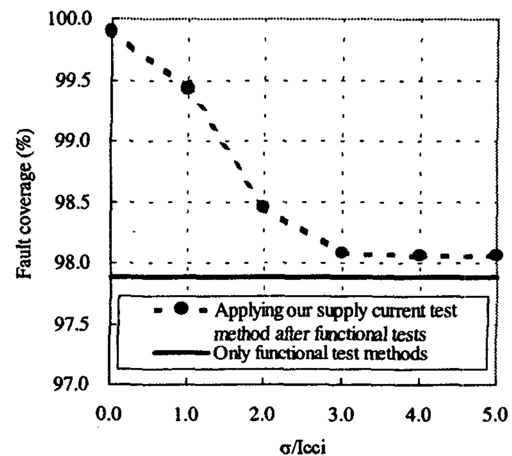
In TTL LS-type ICs, the recommended supply voltage range is from 4.75V to 5.25V. In order to satisfy the specification, the CUT is divided into circuit blocks so that the implemented circuit can work within the recommended voltage range. As the result, it is divided into two blocks and supply current of each block is measured as I_{DDQC} in Eq.(1) like in [6].

The results obtained by functional test method are shown in Table 2. Since experimental results depend on generated random numbers, 10 experiments per the varience of supply current of SSIs have been performed and the average values are denoted in Table 2. As showin in Table 2, fault coverage of 97.89% is obtained. The average number of undetected faults is 10.3.

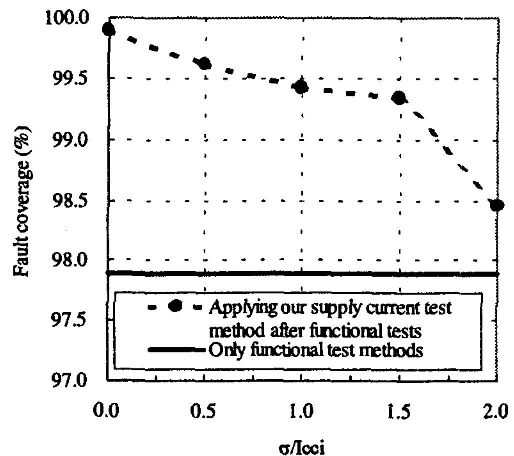
Test input vectors of the supply current test method are generated to detect undetected faults. In the generation, it is assumed that distribution of supply current, I_{CCi}, of an SSI will be almost same as the others and σ/ I_{CCi} is changed from 0% to 5%. The results are shown in Figure 4. As shown in Figure 4, larger fault coverage can be obtained by applying our supply current test method to detect them. Especially, fault coverage of more than 99 % can be obtained, when varience of each supply current of SSIs is smaller than 1.5%.

Table 2. The results obtained by functional tests.

The total numbers of targeted faults	488
The number of detected faults	477.7
The number of undetected faults	10.3
Faults coverage (%)	97.89
The number of test vectors	73.5



(a)Fault coverage for σ/Icci from 0 to 5%



(b)Fault coverage for σ/Icci from 0 to 2%

Figure 4. Obtained fault coverages.

The test generation results are summaried in Table 3. As shown in Table 3, by applying our supply current test method to detect open faults undetected by functional test methods, some of them can be detected with a small number of test input vectors of our supply current test method. It means that more open faults can be detected without long test time added by applying our supply current test method after functional tests than only by functional test methods.

Table 3. Experimental results obtained by applying our supply current test method after functional tests.

σ/Icci	The number of faults detected by supply current test method	The number of addition al test vectors	The Increase of faults coverage (%)	The rate of increase of the test vectors (%)	CPU time (sec)
0.0	9.8	6.3	2.01	8.57	0.31
0.5	8.4	6.6	1.72	8.98	0.60
1.0	7.5	5.9	1.54	8.03	0.88
1.5	7.1	5.9	1.45	8.03	1.56
2.0	2.7	2.5	0.56	3.40	2.18
3.0	0.9	0.8	0.19	1.08	-
4.0	0.8	0.8	0.16	1.08	-
5.0	0.5	0.8	0.16	1.08	-

The number of faults undetected by functional test method = 10.3
CPU time is not measured for σ/Icci=3.0,4.0,5.0.
Used machine: Sun ULTRA 10.

In this paper, only tests for open faults are discussed. Most of the faults in the circuits fabricated with the state-of-art technologies are open faults and bridging ones. It is shown that most of bridging faults can be detected by supply current testing easily[1,2,3]. Thus, most of the bridging faults which can not be detected by a functional test method can be detected by applying the supply current test method. Therefore, if bridging faults are added to targeted faults, more effectiveness of our test approach will be obtained.

4. Conclusion

In this paper, a new test approach is proposed, which is based on a supply current test method. In this approach, the supply current test method is used for detecting only the open faults which are difficult to be detected by functional tests. In order to evaluate the testability, fault coverage of the open faults undetected by functional tests based on stuck-at fault models is examined in an ISCAS-85 benchmark circuit made of TTL LS-type SSIs. The result shows that open faults undetected by a functional test can be detected with a small number of test input vectors of the supply current test method applied after the functional test.

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