A Modified Scheme of OFDM Transceiver for Reduction of Its Natural Delay

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Abstract: In this paper, we analyze the natural processing delay of OFDM systems and proposed two modified functional blocks to decrease about 25% of the total delay. We evaluate BER performance of the proposed scheme to be compared with that of classical one to confirm same performance between them.

1. Introduction

The OFDM (Orthogonal Frequency Division Multiplexing) techniques are extensively applied to the high-data rate communication systems [1]; in the early stage the point-to-point communication such as ADSL (Asymmetric Digital Subscriber Line) or the broadcasting systems such as DAB (Digital Audio Broadcasting) and DVB-T (Digital Video Broadcasting – Terrestrial) and BWA (Broadband Wireless Access) [2]-[7].

This paper focuses on the packet-type multiple access, in which only one transmitter occupies the channel for a setting time. For increase of its throughput, it is necessary to minimize the length of the preamble in the packet and the interval between packets. The length of the preamble, which is used for the initialization of the receiver, has been optimized 1 to 4 of the OFDM symbols typically. And the other issue, the interval of the packet is selected to consider the signal processing delay time at the physical layer and MAC layer both. The OFDM systems, which are included in the physical layer, process a unit symbol (that is made up of multiple values) so that its natural processing delay is one of the major factor.

In Section 2, we analyze the delays of each functional block in the OFDM transceiver based on [5] and the modified schemes for two blocks among them to remove their delay are proposed in Section 3. In Section 4, we compare the performance with that of the classical schemes under multipath fading channels.

2. Delays of OFDM system

In [8], Grass analyzed the processing delays of each block in the OFDM transceiver. This result is based on the C model (high-level) so that the real results of the low-level differ from them in the view of the time. We may expect the ratio of each delay to the total delay of the transceiver by evaluating the number of the required clock for each block.

2.1 Delays of each functional block

The delay of the block is defined as the time interval or the required processing delay from the input time to the output time. Differently contrary to the single-carrier modulation system, OFDM systems are processing the values by symbol unit so that it is necessary to define the number of required bit to generate one OFDM symbol. This section focuses on IEEE 802.11a [5].

1) **Scrambling and De-scrambling:** Scrambling block in the transmitter outputs the result of XOR operation between the input data bits and the PN sequence to randomize the characteristic of the data so its operating delay is 0~1 clocks. De-scrambling block in the receiver has the same delay.

2) **Channel encoding and De-coding:** Channel encoding in the transmitter is convolutional encoding, of which the generator polynomials are $g_0=133_8$ and $g_1=171_8$, the constraint length (K) is 7 and its coding rate (R) is 1/2. The delay is 0~1 clock because the coded bits are outputted for every input uncoded bit. For channel decoding in the receiver, Viterbi decoding is very popular. The delay is dependent on the depth, which is more than five times of constrain length in general. Let define depth as D, first decoded data bit is outputted after D clocks when the number of input path is two.

3) **Interleaving and De-interleaving:** Interleaving can be considered with the typical three types; inter-symbol interleaving, inter-subcarrier interleaving and intra-subcarrier interleaving. IEEE802.11a standard uses a block interleaving scheme with block size corresponding to the number of bits in a single OFDM symbol which is made up of 2nd and 3rd ones. Intra-subcarrier one interleaves M bits corresponding to each subcarrier, so the delay becomes M clocks and inter-subcarrier one does K subcarrier in each symbol so the delay becomes K*M clocks. But if the number of the input path is two, the delay becomes down to a half. De-interleaving is the inverse process of Interleaving block so that the delay becomes K×M clocks. The number of bits for one symbol is shown in Table 1.

Table 1. The number of bits for one OFDM symbol.

Constellation	Bits per subcarrier: M	Number of used subcarrier per symbol: K	Bits per symbol: M×K
BPSK	1	48	48
QPSK	2	48	96
16QAM	4	48	192
64QAM	6	48	288

4) **Mapping and De-mapping:** Mapping and De-mapping use BPSK, QPSK, 16QAM and 64QAM, dependent on

the transmit rate requested to convert the input bit sequence into complex number train representing each constellation point. If the number of the input(output) data path is 6, the delay of Mapping(De-mapping) block becomes 0~1 clock.

5) **Formatting and De-formatting:** There are three kinds of subcarriers in the OFDM symbols; data transmit subcarriers, pilot subcarriers and virtual subcarriers. Formatting block arranges input data in corresponding subcarrier index and add pilots and virtual carriers to complete preparation for generation of a OFDM symbol. Thus when inputted data, Formatting block outputs data in order, so the delay is 0~1 clocks. The delay of De-formatting is same case.

6) **Subcarrier reposition:** Subcarrier reposition block changes the output order of the first half (N/2 values) and the second one (N/2 values) for the sequential N input values. In the typical scheme, the outputs of Formatting block are corresponded to from negative subcarrier index to positive index in order and by passing Subcarrier reposition block, the values corresponding to positive subcarrier index are inputted into IFFT block before the others as shown in Figure 1 [9]. In the Figure 1, the gloomy quadrangle means the output part earlier than white solid one and Eq.(1) can be expressed. Thus the delay is N/2 clocks.

$$f = o - \frac{N}{2} = k \qquad (1)$$

where f, o and k are IFFT block input index, Formatting block output index and subcarrier index respectively. Subcarrier reposition block in the receiver is same case.

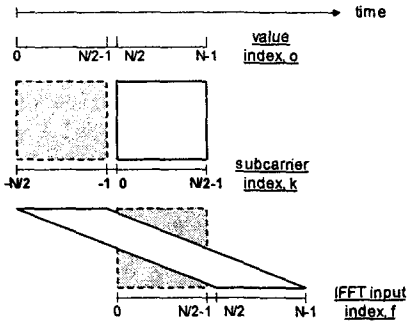


Figure 1. Subcarrier reposition block.

7) **IFFT and FFT:** There are Radix-2, 4 and 4/2 for the general architecture and the transceiver can share FFT/IFFT block due to the duality characteristic of FFT. Its delay is dependent on the FFT size and the operating clock frequency and architecture. If one value is inputted into it in every clock, the delay of N-point FFT/IFFT is more than 2N clocks.

8) **GI(Guard Interval) inserting and removing:** GI is inserted in every OFDM symbol as a countermeasure against the severe delay spread by copying the real G values among N input values and outputting the copied values before N input values as shown in Figure 2. The output order becomes (N-1-G),(N-G),...,(N-2),(N-1),0,1,...,(N-2),(N-1). Until (N-1-G)th value is outputted from IFFT block, the foremost values are stored in this block, so its delay becomes N-G clocks.GI removing in the receiver is simply passing only rear N values among N+G values and discarding the foremost G values, so the delay is G [sample duration].

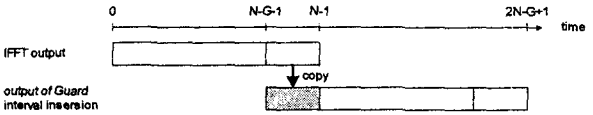


Figure 2. GI inserting block.

9) **LPF(Low Pass Filtering):** All transceiver uses LPF, typically squared-root-raised-cosine filter, to meet the spectrum mask defined in the standard. The filter length is longer than 16 [OFDM sample duration] so that its delay has longer than 8 [OFDM sample duration]

10) **Sync:** Sync block is made up of three functions as follows,
- carrier frequency sync,
- symbol timing sync,
- sampling frequency sync.

Because it carries out estimating and correcting of the sync errors through the preamble of the packet, its total delay can be defined as the required time from receiving the preamble completely to correcting the estimated sync errors. Thus it depends on the estimate algorithms and their cooperation scenario, in general the delay may be about 1/8 through 2 [OFDM symbol duration].

11) **Channel estimation and equalization:** Channel estimation carries out Eq.(2) in the frequency domain by using Fast Fourier transformed preamble to detects the distortion characteristics of each subcarrier occurred through channel.

$$C(k) = \frac{1}{H(k,p)} = \frac{X(k,p)}{Y(k,p)} = \frac{X(k,p)\cdot Y^*(k,p)}{|Y(k,p)|^2} \qquad (2)$$

where C, H, X and Y are the equalizer coefficient, the channel characteristic, the transmitted value and the received value for k^{th} subcarrier. p and * mean the preamble and the conjugate complex operation. During the estimation for each subcarrier, one division function is required, so which is needed 2~5 clocks.

Equalization block corrects the data value of each subcarrier following the preamble as multiply the distorted data values by the estimated equalizer coefficients according to Eq.(3). Thus its delay is 1~2 clocks.

$$\tilde{X}(k,d) = Y(k,d)\cdot C(k) \qquad (3)$$

where d and ~ mean the data symbol and the corrected data value.

2.2 Total delay

We have to use two kinds of unit to analyze the delays of each functional block because there are two kinds of blocks, which are dependent on the operating clock frequency or not. For the former, the number of clock is used to express its delay, while for the latter, the number of the nominal sampling duration is used. Table 2 and Figure 3 show the total delay of the transceiver according to the following parameters,

- convolutional coding rate : 1/2
- constellation : 64QAM
- Viterbi decoding depth : 60

In the view of the transmitter, the total delay is about 9.5 and 5 [usec] for the operating clock frequency of 40 and 80MHz respectively. The total delay of the receiver is increased to 14.6 and 9.9 [usec] respectively due to using Sync block and Viterbi decoding block. From these results, in the transmitter in the order of Interleaving, IFFT, GI inserting, Subcarrier reposition, LPF block, their delays are dominant. And the delay of Sync, De-interleaving, FFT, Viterbi decoding, GI removing, Subcarrier reposition block are dominant in the receiver.

Long processing delay of Modem in the multiple access environments means that it needs long time to generate the transmit signal and recover the received signal and this fact results to decrease of the throughput.

Table 2. Processing delay.

(a) Transmitter

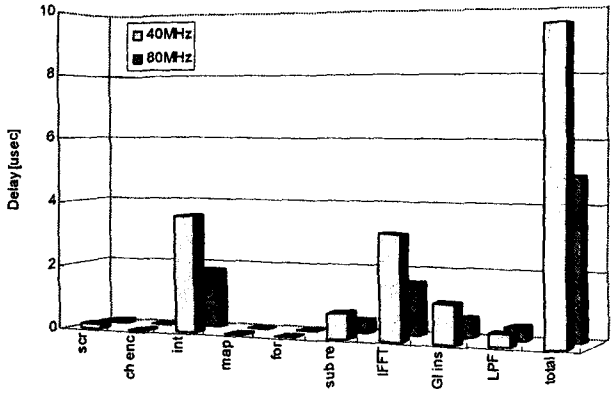
Tx	Delay	40MHz		80MHz	
		[usec]	[%]	[usec]	[%]
scr	6 clocks	0.15	1.6%	0.075	1.5%
ch enc	1 clocks	0.025	0.3%	0.0125	0.3%
int	144 clocks	3.6	38.2%	1.8	36.6%
map	1 clocks	0.025	0.3%	0.0125	0.3%
for	1 clocks	0.025	0.3%	0.0125	0.3%
sub re	32 clocks	0.8	8.5%	0.4	8.1%
IFFT	128 clocks	3.2	34.0%	1.6	32.6%
GI ins	48 clocks	1.2	12.7%	0.6	12.2%
LPF	8 samples	0.4	4.2%	0.4	8.1%
total		9.425	100.0%	4.9125	100.0%

(b) Receiver

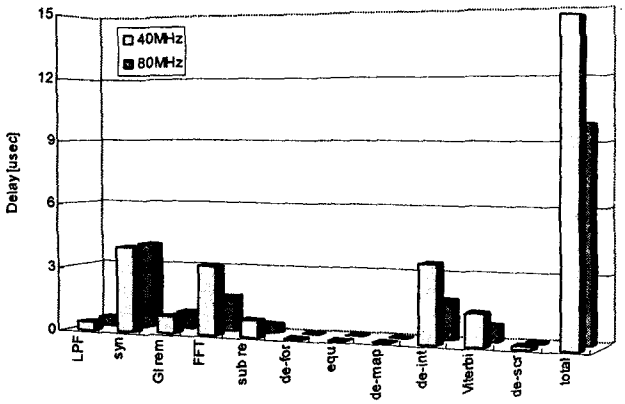
Rx	Delay	40MHz		80MHz	
		[usec]	[%]	[usec]	[%]
LPF	8 samples	0.4	2.7%	0.4	4.1%
syn	1 symbol	4	27.5%	4	40.5%
GI rem	16 samples	0.8	5.5%	0.8	8.1%
FFT	128 clocks	3.2	22.0%	1.6	16.2%
sub re	32 clocks	0.8	5.5%	0.4	4.1%
de-for	1 clocks	0.025	0.2%	0.0125	0.1%
equ	2 clocks	0.05	0.3%	0.025	0.3%
de-map	1 clocks	0.025	0.2%	0.0125	0.1%
de-int	144 clocks	3.6	24.7%	1.8	18.2%
Viterbi	60 clocks	1.5	10.3%	0.75	7.6%
de-scr	6 clocks	0.15	1.0%	0.075	0.8%
total		14.55	100.0%	9.875	100.0%

3. Proposed Two Schemes

In this paper we propose the modified schemes of Subcarrier reposition block and GI inserting block to get rid of its processing delay. From Table 2, the delay of Subcarrier reposition block occupies about 8% in the transmitter and about 4% in the receiver and that of GI inserting is about 12% of total transmitter delay.



(a) Transmitter



(b) Receiver

Figure 3. Processing delay.

3.1 Subcarrier reposition

In Figure 4, the outputs of Formatting block (index: o) are the input IFFT block (index: f) without change of the order. This means that 0,1,...,(N-2),(N-1) of Formatting block output index o are corresponding to 0,1,...,(N/2-2),(N/2-1),-N/2,(-N/2+1),...,-2,-1 of subcarrier index f as Eq.(4), therefore the delay of Subcarrier reposition block becomes 0. Another one in the receiver is the reverse process of the transmitter so that its delay is 0.

$$f = o, \begin{cases} k = o, \ when \ 0 \le o \le \dfrac{N}{2} - 1 \\ k = o - N, \ when \ \dfrac{N}{2} \le o \le N - 1 \end{cases} \quad (4)$$

3.2 GI Inserting

N output values from IFFT block are passed to the next block and then first G values again, as like Figure 5. By copying first G values its delay becomes 0.

In the receiver, if N values except first G values among N+G values input into FFT block, this is equivalent to occurring the symbol timing error of G [sample duration]

and this effects the phase rotation of subcarrier. But it can be simply corrected at Channel estimation block and Equalization block.

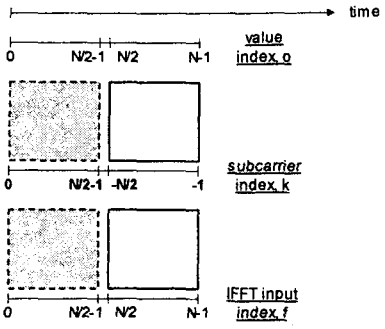


Figure 4. Proposed subcarrier reposition block.

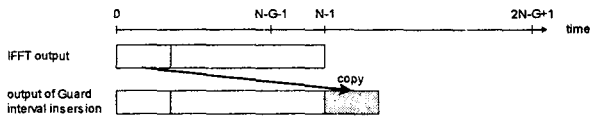


Figure 5. Proposed GI insertion block.

4. Simulation Results

4.1 System and channel model

In this paper, we use the OFDM system based on IEEE 802.11a. Figure 6 shows the channel model, which the length of the delay spread is 7 [sample duration]. The length of guard interval, G and useful data interval, N are 16 and 64 samples respectively. The length of the channel delay spread is shorter than that of guard interval.

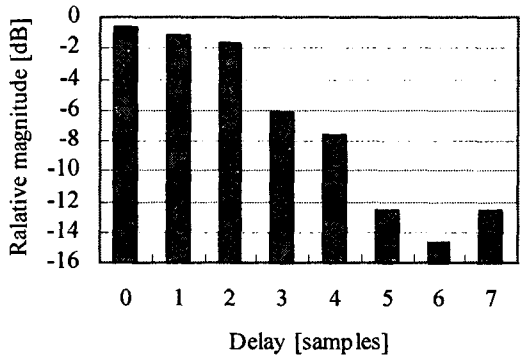


Figure 6. Channel delay and attenuation

4.2 BER performance

We carry out the performance evaluation of the proposed schemes under multipath fading channel with AWGN noise. Figure 7 shows BER comparison for classical scheme (line curves in the Figure) and the proposed one (symbols curves in the Figure). The proposed one includes both the modified Subcarrier reposition block and the modified GI inserting block. There is no difference between both schemes.

5. Conclusions

It is known that OFDM systems are suitable for the high-data rate transmission but its relative long processing delay results in the decrease of throughput. In this paper, we analyzed the natural processing delay of OFDM systems and proposed two modified functional block to decrease the total delay. We evaluated that the proposed blocks decrease about 21% of the transmitter delay and about 4% of the receiver delay and compared BER performance of the proposed scheme with that of classical one to confirm same performance between them.

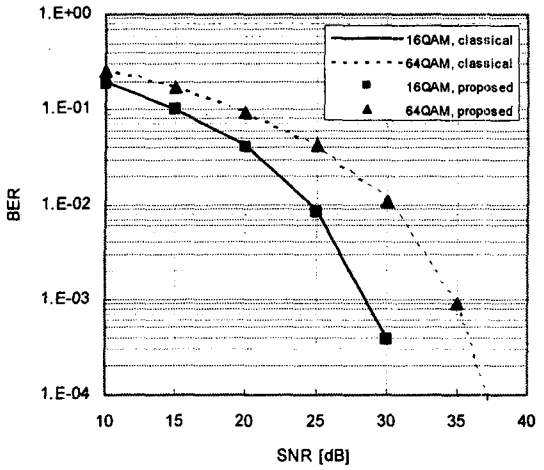


Figure 7. BER comparison: classical scheme vs. proposed scheme includes Subcarrier reposition and GI inserting.

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