

The far-end crosstalk voltage for CMOS-IC load

Nobuyuki Miyao, Yasuaki Noguchi and Fujihiko Matsumoto

Department of Applied Physics, National Defense Academy
1-10-20 Hashirimizu Yokosuka, Kanagawa, 239-8686 Japan
Tel: +81-468-41-3810 ext.3624, Fax: +81-468-44-5912 (Dept. of Applied Physics)
E-mail: matsugen@nda.ac.jp

Abstract: The capacitance of nonlinear component such as a CMOS inverter varies largely around the threshold voltage. We measured the far-end crosstalk of two parallel microstrip lines with the CMOS inverter load near the threshold voltage of the CMOS inverter. The negative voltage of the crosstalk agrees with that for a 4pF capacitor load. The positive voltage of the crosstalk hardly changes of the amplitude of the input step voltage.

1. Introduction

Semiconductor device technology and high-speed digital signal processing techniques contribute much to high speed, low voltage operation and downsizing of electronic equipments. It becomes more difficult and more important to prevent the inducing faulty behavior in integrated circuits. Crosstalk noise is one of causes of faulty behavior. Crosstalk noise is induced by inductive coupling and capacitive coupling from the pulse activated line to other lines. Far-end crosstalk waveform is indicated on a V-t plane. The crosstalk voltage depends on some parameters of microstrip lines, such as line interval, coupling length, thickness of dielectric, dielectric constant and terminated load impedance [1]. In case where the pulse activated line is terminated by a rated load impedance element, the crosstalk voltage can be calculated exactly. However, in most actual circuits, transmission lines are terminated by nonlinear impedance elements, such as CMOS-IC. It is difficult to calculate the crosstalk voltage for microstrip lines with a nonlinear impedance element because of its complexity [2]. Although we can analyze the crosstalk waveform using a simulator, such as SPICE, we require a highly efficient hardware.

The purpose of this research is to study behavior of crosstalk for the CMOS inverter load. The equivalent capacitance of the CMOS inverter varies largely around the threshold voltage. The change of the capacitance is regarded as nonlinear impedance. Therefore, we took notice of the variation of the crosstalk voltage, if the input step voltage is near the threshold voltage of the CMOS inverter. Firstly, The measurement system of far-end crosstalk and the simulation method with 4-port network are presented. Secondly, the calculation of far-end crosstalk constant and the measurement of

far-end crosstalk for capacitor load are described. Finally, the experimental results of the far-end crosstalk for the CMOS inverter load is shown.

2. Experiment method

2.1 measurement

Measurement system of far-end crosstalk and principal parameters of the microstrip lines are shown in Fig. 1 and 2 respectively.

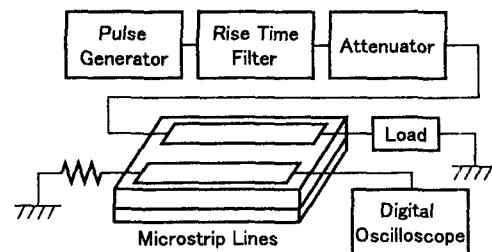


Figure 1. Measurement system of far-end crosstalk

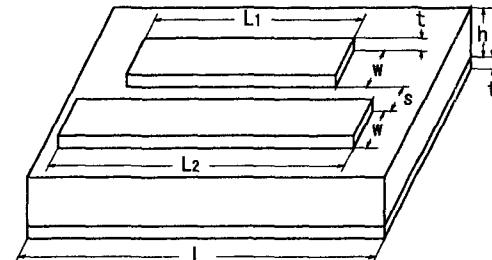


Figure 2. Parameters of microstrip lines

L_1	coupling length	200mm
h	thickness of dielectric material	0.3mm
s	line interval	1.0mm
t	thickness of line	0.018mm
w	width of line	0.58mm
ϵ	Dielectric constant	4.8

The coupling length of the microstrip lines is 200mm. The line interval is set at 1.0mm, for which far-end crosstalk constant obtained from pre-experiment is the closest to that from Ref. [3] (See Subsection 3.1). The dielectric material is fiberglass epoxy, the relative permittivity of which is 4.8. The thickness of the dielectric

plate is 0.3mm. The microstrip lines are designed so that the characteristic impedance of a single line may be 50Ω.

For impedance matching, the near-end terminal of the driven line is terminated with a 50Ω resistor. Three kinds of loads are connected with the far-end terminal of the driving line. One is a 50Ω resistor, and the others are a 4pF monolithic ceramic capacitor and a CMOS inverter (TC74HC04A). The 50Ω resistor is used in order to confirm the impedance matching of microstrip lines and to obtain the far-end crosstalk constant. The reason why the 4pF capacitor load is selected is that the input capacitance of CMOS-IC is about 4pF [4]. The CMOS inverter IC has six inverter logic gates. Only one gate is connected with the far-end terminal of the driving line, the others are grounded. The output pin (No.2) is grounded too. The input step voltage is set to 4.2, 3.7, 3.3, 2.9, 2.6, 2.3, 2.1, 1.9 and 1.5V by the attenuator.

2.2 simulation

The simulation model is shown in Fig. 3. This model is called a 4-port network.

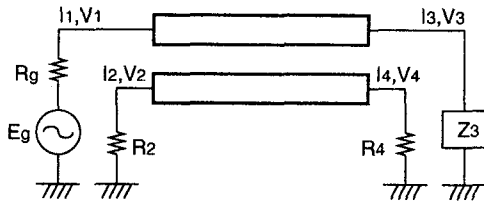


Figure 3. 4-port network simulation model

The basic equations of this model are telegraphy equations composed of common and differential mode [5]. These equations can be solved with matrices. We obtained numerical data of crosstalk waveform by MATLAB® simulator. For example, V_4 (Far-end crosstalk voltage) is expressed as follows.

$$V_4 = -\frac{E_g(\ell, t)}{\Delta} \{(c_{21} + G_3 d_{21}) + G_2(a_{21} + G_3 b_{21})\} \quad (1)$$

$E_g(\ell, t)$: input step voltage function (driving line)

$G_3 = \frac{1}{Z_3}$: admittance of far-end load on driving line

$G_2 = \frac{1}{R_2}$: admittance of near-end load on driven line

Δ : coefficient determinant for crosstalk equation

$$c_{21} = \frac{1}{4W_c} \sinh \theta_c - \frac{1}{W_d} \sinh \theta_d \quad (2)$$

$$b_{21} = W_c \sinh \theta_c - \frac{W_d}{4} \sinh \theta_d \quad (3)$$

$$a_{21} = d_{21} = \frac{1}{2} (\cosh \theta_c - \cosh \theta_d) \quad (4)$$

W_c : characteristic impedance for common mode

W_d : characteristic impedance for differential mode

θ_c : phase velocity for common mode

θ_d : phase velocity for differential mode

3. Result of measurement and simulation

3.1 matching resistor load

In order to confirm accuracy of our measurement, a far-end crosstalk with a matching resistor is measured. The crosstalk waveform for the matching resistor load is shown in Fig. 4. The simulated waveform agrees with the experimental result.

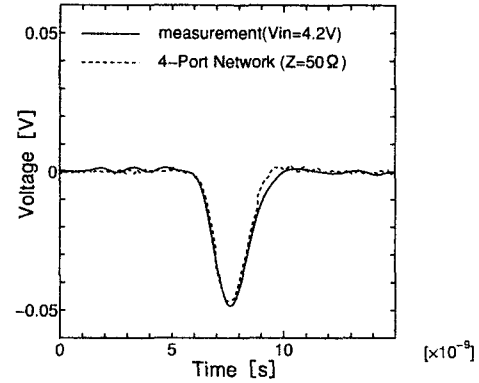


Figure 4. Far-end crosstalk for matching resistor load

We can calculate the far-end crosstalk constant from these results. According to Ref. [3], far-end (forward) crosstalk constant is defined as follows,

$$K_F = \frac{1}{2} \left(Z_0 C_m - \frac{L_m}{Z_0} \right) \quad (5)$$

$$= \frac{V(\ell, t) T_r}{V_k \ell} = \frac{V(\ell, t)}{\ell \frac{d}{dt} [V_{in}(t)]_{max}} \quad (6)$$

K_F : far-end crosstalk constant

Z_0 : characteristic impedance of each line in the presence of the other

C_m : mutual capacitance per unit length between the two lines.

L_m : mutual inductance per unit length between the two lines.

$V(\ell, t)$: Voltage of driven line at $x = \ell$ (far-end), time t

T_r : risetime of input step pulse

V_k : magnitude of input step voltage

ℓ : coupling length

$\frac{d}{dt} [V_{in}(t)]_{max}$: maximum derivative of the input step voltage

The variables in Eq. (6), $V(\ell, t)$, V_k , ℓ , and $\frac{d}{dt} [V_{in}(t)]_{max}$ are measurable. We measured these parameters for the intervals of 2.0, 1.5, 1.0, 0.50, and 0.25mm. The comparison between the far-end crosstalk constant in Ref. [3] and the experimental values obtained from our measurement is shown in Fig. 5, where h is the thickness of the dielectric. The values of our results are a little lower than that shown in Ref. [3]. In case where the line interval is 1.0mm, the measured value is the nearest to that of Ref. [3].

Thus, the results from our measurement agree with the values of 4-port network simulation and the values in Ref. [3].

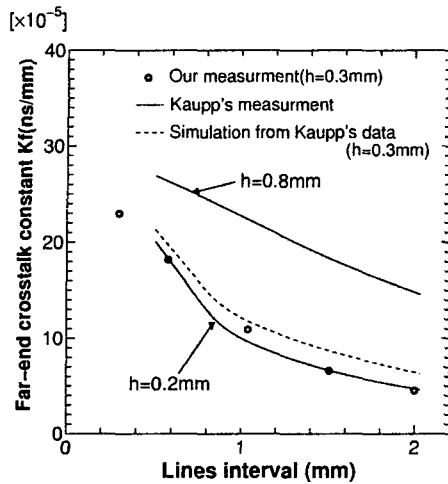


Figure 5. Far-end crosstalk constant comparison

3.2 capacitor load (mismatching)

The far-end crosstalk waveform for rated capacitance load is shown in Fig. 6.

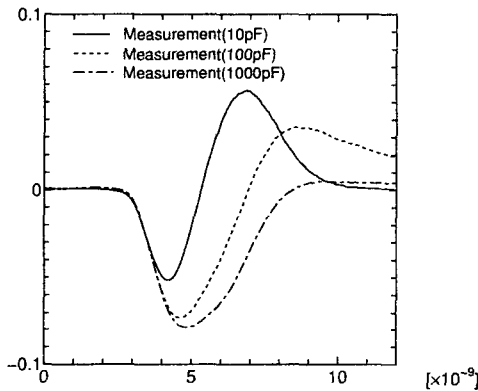


Figure 6. the crosstalk waveform for 10-1000pF capacitor loads

In case where a positive input pulse propagates through the driving line which is terminated by the matching resistor load, a negative crosstalk is induced at the far-end of the driven line. However, for a capacitor load is terminated at far-end of driving line, the terminal impedance are varied by input voltage. Thus, the positive crosstalk is caused by mismatching refractive effect. It is difficult to solve the crosstalk equations. Therefore we usually make use of computer to solve the equations. Figure 7 shows the maximum and the minimum voltages of the crosstalk for capacitance of the load. The simulated values obtained from 4-port network simulation agree with measured value of maximum and the minimum voltages of the crosstalk, roughly. As the capacitance of the load increases above 15pF, the

positive crosstalk voltage is smaller than the magnitude of the negative one and approaches to zero gradually. Conversely, when the capacitance of the load is smaller than 15pF, the positive crosstalk voltage is larger than magnitude of the negative one. This means that mismatching refractive effect appears when the capacitance of the load is smaller.

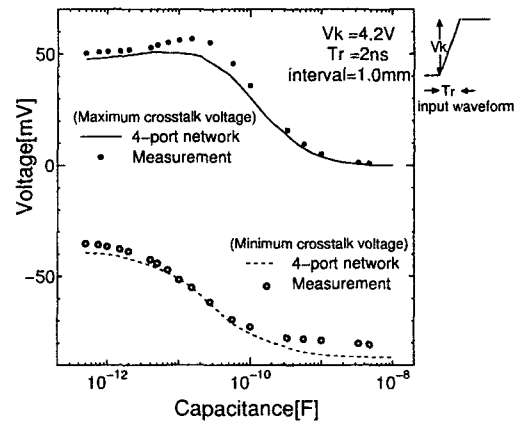


Figure 7. Maximum and Minimum crosstalk voltage for any capacitor loads

3.3 CMOS inverter load

Figures 8 and 9 show the crosstalk waveforms with respect to 4.2V and 2.6V input step voltages, respectively. For both, the negative voltage of the crosstalk similar to the negative crosstalk part for the 4pF capacitance load. However the positive voltage of the crosstalk never correspond with the positive crosstalk for the 4pF capacitance load. Further, It is found from Fig. 10 that the crosstalk waveform for the CMOS inverter load agrees with that for the 4pF capacitance load, when the magnitude of the input step voltage is 1.5V.

Figure 11 shows the relation between the input voltage and the crosstalk voltage. The measured results for the CMOS inverter and the 4pF capacitor are denoted by closed circles and open circles, respectively. The calculated crosstalk voltage through 4-port network for the 4pF capacitance load is drawn by the solid line. The lower part in Fig. 11 shows the minimum negative crosstalk voltage. It is apparent that the experimental result for the inverter accords with that for the capacitance load and the simulation result. The upper part in Fig. 11 shows the maximum positive crosstalk voltage. It should be noted that the crosstalk voltage for the inverter changes little even though the input step voltage increases in the range higher than 2.3V, while the crosstalk voltage for the capacitance is proportional to the step voltage. Therefore, The waveform of 4-port network simulation hardly agrees with the experimental result.

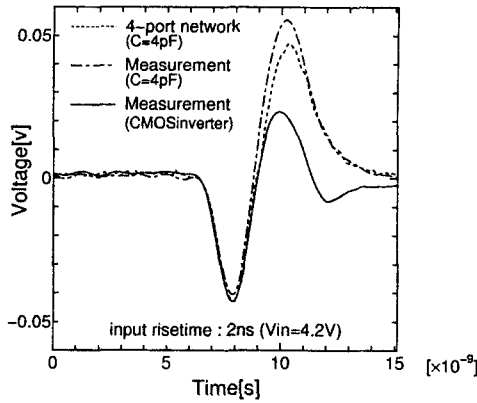


Figure 8. Far-end crosstalk (CMOS load $V_k=4.2V$)

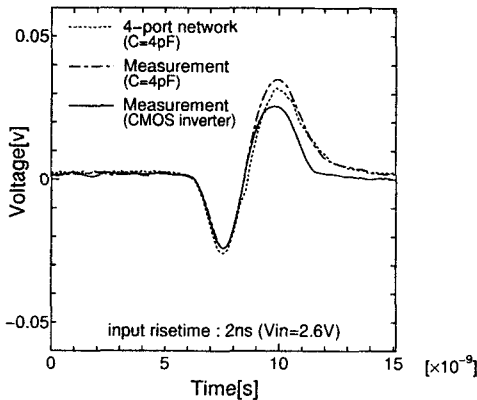


Figure 9. Far-end crosstalk (CMOS load $V_k=2.6V$)

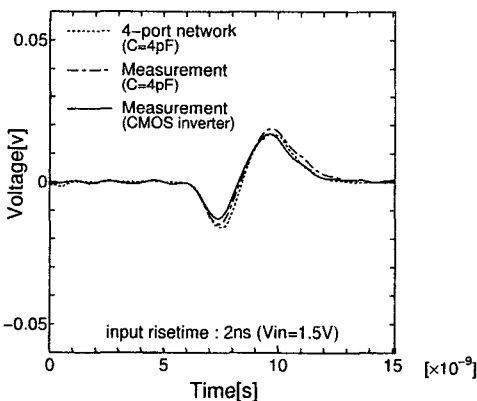


Figure 10. Far-end crosstalk (CMOS load $V_k=1.5V$)

4. Conclusion

We have obtained the following interesting results about the crosstalk voltage for a CMOS inverter load:

- The negative crosstalk voltage agrees with that for a 4pF capacitance load.
- The positive crosstalk voltage is nearly constant, in case where the input step voltage is larger than 2.3V, while the voltage for the capacitance load is proportional to the input step voltage.

Threshold switch occurs in the CMOS inverter, when the input step voltage is between 2.3V and 2.6V. It

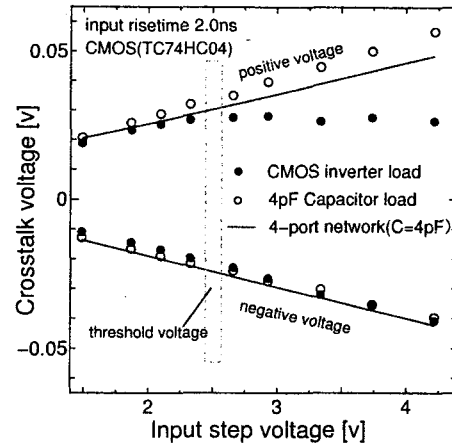


Figure 11. Relation between input-V and crosstalk-V

is expected that threshold switch affects the positive crosstalk voltage. As stated in subsection 3.2, the magnitude of the positive crosstalk voltage depends on the reflection at far-end of the driving line.

We conclude as follows. The far-end crosstalk waveform for the CMOS inverter load which never causes threshold switch (the input voltage is below about 2.5V) depends on the input capacitance of the CMOS inverter. The CMOS inverter load which causes threshold switch (the input voltage is above about 2.5V) has an effect in suppressing the positive (reflectal) voltage of the far-end crosstalk.

If the cause of the effect is clarified, it is possible to improve the simulation model in order to reproduce the crosstalk waveform for the CMOS inverter load.

References

- [1] A.Feller, H.R.Kaupp and J.J.Digiacom, "Crosstalk and reflections in high-speed digital systems", Proceedings - Fall Joint Computer Conference, Spartan Books, Washington D.C., pp.511-524, 1965
- [2] Stephen Lum, Michel Nakhla, and Qi-jun "Sensitivity Analysis of Lossy Coupled Transmission Lines with Nonlinear Terminations", IEEE Transactions on Microwave Theory and Techniques, Vol.42, NO.4, pp.607-615, Apl. 1994
- [3] H.R.Kaupp, "PULSE CROSSTALK BETWEEN MICROSTRIP TRANSMISSION LINES", 7th International Electronics Circuit Packaging Symposium Record (Wescon 66), 2/5, pp.1-12, 1966
- [4] Yasuaki Noguchi, Minoru Ohtani, Ken Mariko and Fujihiko Matsumoto, "Crosstalk of microstrip lines with capacitor loads", INT. J. ELECTRONICS, 1998, VOL 85, NO.3, pp.327-336.
- [5] Yoshio kami, Toshio Onigata "Step Response of Coupled Printed-Circuit Traces", TECHNICAL REPORT OF ICICE EMCJ92-4 pp.23-28.