A Realization of a Grounded Transconductor Using a CMOS Complementary Pair

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Abstract: This paper describes a realization of a linearized transconductor using a CMOS complementary pair. The proposed transconductor is driven by a grounded signal source. How to cancel the offset current is described. Moreover, how to control the transconductance is described. It is shown that power consumption of the proposed transconductor without the control circuit is about half as low as that of the conventional Wang's OTA through computer simulation.

Keywords: Transconductor, grounded, OTA and complementary pair

1. Introduction

Recently, many techniques concerned with the linearized transconductors have been presented [1]–[3]. It is well known that the transconductors can be applied to many kinds of building blocks such as filters, multipliers, oscillators and so on. The linear V-I convertable input voltage range of the transconductors is called a linear input voltage range. Because the linear input voltage range affects the distortion of the output signal, it is desirable that the transconductance amplifier has a wide linear input voltage range.

It is known that the linear input voltage range of the Wang's OTA [1] is comparatively wide. This circuit includes three MOSFET's connected between the power supply lines, which means that this circuit requires comparatively high supply voltage. When we consider diminishing the supply voltage and power consumption, the number of the MOSFET's connected to the power supply lines should be decreased [3].

In this paper, a linearized transconductor realized by using a CMOS complementary pair is proposed. The proposed transconductor is driven by a grounded signal source. How to cancel the offset current is proposed. How to control the transconductance is proposed. The validity of the proposed method is confirmed by using the PSpice simulator.

2. Proposed method

2.1 Transconductor

Figure 1 shows the proposed transconductor realized by using the complementary pair. As shown in this figure, the circuit configuration of the proposed transconductor is similar to that of the CMOS digital inverter. When both of the transistor M1 and the transistor M2 operate in the saturation region, the drain currents \( I_{D1} \) and \( I_{D2} \) can be given by

\[
\begin{align*}
I_{D1} &= K_1(V_{GS1} - V_{TN})^2 \\
I_{D2} &= K_2(V_{GS2} - V_{TP})^2
\end{align*}
\]

(1)

where \( K_1 \) and \( K_2 \) are real. The voltages \( V_{TP} \) and \( V_{TN} \) are the threshold voltages of the pMOS and nMOS, respectively. Both of them slightly differ from each other. For the simplicity, we set

\[
\begin{align*}
V_{TP} &= -(V_T + \delta) \\
V_{TN} &= V_T - \delta
\end{align*}
\]

(2)

where \( V_T \) and \( \delta \) are real. Because \( M_1 \) and \( M_2 \) are the complementary pair, we set

\[
K = K_1 = K_2
\]

(3)

The gate-source voltages \( V_{GS1} \) and \( V_{GS2} \) are given by

\[
\begin{align*}
V_{GS1} &= V_{IN} + V_C + V_P - V_D \\
V_{GS2} &= V_{IN} + V_C - (V_P - V_D)
\end{align*}
\]

(4)
Figure 3. MOS subtractor [4].

\[ V_{OA} = V_a - V_b - V_b \]

(a)

\[ V_{OS1} - V_P \]

\[ V_{OS2} - V_P \]

(b)

Figure 4. Building blocks. (a) Inverter, (b) Half-gain amplifier.

The output current \( I_O \) is given by

\[ I_O = I_{D1} - I_{D2} \]  

(5)

From Eqs.(1)–(5), eliminating \( V_{GS1}, V_{GS2}, K_1, K_2, V_T \) and \( V_{IN} \) leads to

\[ I_O = 4K(V_P - V_D - V_T)(V_{IN} + V_C + \delta) \]

(6)

where \( V_P \) is the supply voltage. The above equation indicates that the transconductance and the offset current can be independently controlled by varying the voltage \( V_D \) and \( V_C \), respectively. The transconductance \( G_M \) is defined by \( G_M = dI_O/dV_{IN} \). The transconductance \( G_M \) of the proposed circuit is given by

\[ G_M = 4K(V_P - V_D - V_T) \]

(7)

The negative transconductance can be realized by using the current mirrors as shown in Fig.2.

2.2 \( V_D \) and \( V_C \)

In order to realize the batteries whose voltages are \( V_C + V_D \) and \( V_C - V_D \) shown in Fig.1, we use the MOS subtractor [4] shown in Fig.3. In this figure, the aspect ratio of the transistor \( M_1 \) is equal to that of the transistor \( M_2 \). In this figure, both of \( M_1 \) and \( M_2 \) are p-channel transistors. The relationships among \( V_A, V_B \) and \( V_O \) are given by

\[
\begin{align*}
V_P + V_{GS1} &= V_A \\
V_O + V_{GS2} &= V_B \\
\end{align*}
\]

(8)

When no current flows out of the output terminal, the drain currents \( I_{D1} \) and \( I_{D2} \) are equal to each other. In this case, the gate-source voltages \( V_{GS1} \) and \( V_{GS2} \) become equal to each other. Substituting \( V_{GS1} = V_{GS2} \) into Eq.(8) leads to

\[ V_O = V_B - V_A + V_P \]

(9)

From the above equation, it is found that this circuit functions as a kind of subtractor. Let us consider the output voltage \( V_{O1} \) of the circuit shown in Fig.4(a). The circuit is equal to the circuit obtained by applying the power supply voltage \( -V_P \) to the terminal B of the circuit shown in Fig.3. Substituting \( V_B = -V_P \) into Eq.(9) gives the output voltage \( V_{O1} \).

\[ V_{O1} = -V_A \]

(10)

The above equation indicates that this circuit functions as an analog inverter. On the other hand, the output voltage \( V_{O2} \) of the circuit shown in Fig.4(b) can be determined by substituting \( V_A = V_O \) into Eq.(9).

\[ V_{O2} = \frac{V_B}{2} + \frac{V_P}{2} \]

(11)

The above equation indicates that this circuit functions as a half-gain amplifier whose bias voltage is \( V_P/2 \).

By using some of the circuits described in the above, the proposed transconductor shown in Fig.5 is obtained. In this figure, \( V_{O3} \) and \( V_{O4} \) become

\[
\begin{align*}
V_{O3} &= V_{IN}/4 - V_{DP}/2 + V_C \\
V_{O4} &= V_{IN}/4 - V_{DN}/2 + V_C \\
\end{align*}
\]

(12)
From the above equation, we find that $V_{IN}$, $V_C$ and $V_D$ are given by the following equation.

\[
\begin{align*}
V_{IN} &= \frac{V_{IN}'}{4} \\
V_D &= -\frac{V_D'}{2} \\
V_C &= V_C'
\end{align*}
\] (13)

where $V_{DP}' = -V_{DN}' = V_D'$. The voltages $V_{DP}'$ and $V_{DN}'$ can be generated by using the circuit shown in Fig.6. In this figure, the output voltages are given by the following formulae.

\[
\begin{align*}
V_{DP}' &= -\frac{V_{DIN}}{2} \\
V_{DN}' &= \frac{V_{DIN}}{2}
\end{align*}
\] (14)

In Eqs.(6), (13) and (14), eliminating $V_{DP}'$, $V_{DN}'$, $V_C'$ and $V_{IN}'$ leads to

\[
I_O = 4K \left( V_P - \frac{V_D}{4} - V_T \right) \left( \frac{V_{IN}'}{4} + V_C' + \delta \right)
\] (15)

2.3 Cancellation of the offset current

Figure 7(a) shows the block diagram for cancellation of the offset current. The blocks surrounded by the broken lines indicate the proposed transconductor. In this figure, $V_X$ and $V_C$ are given by

\[
\begin{align*}
V_X &= V_{IN} + V_C + \delta \\
V_C &= -G \cdot V_X
\end{align*}
\] (16) (17)

In the above equations, eliminating $V_X$ leads to

\[
V_C = -\frac{G}{1+G} (V_{IN} + \delta)
\] (18)

where $-G$ is the total gain from the voltage $V_X$ to $V_C$. When the gain $G$ is sufficiently high, $G/(1+G)$ becomes unity. When $V_{IN} = 0$, the voltage $V_C$ is approximated by

\[
V_C \sim -\delta
\] (19)

From Eqs.(13), (15) and (19), we find that cancellation of the offset current is achieved by applying the voltage $V_C'$ to the other transconductors. Because it is obvious that the gain $G$ is proportional to $R_L$, the gain $G$ can be easily made sufficiently high by removing $R_L$.

Figure 7(b) shows the proposed circuit which cancels the offset current described in the above. In this figure, $C_{ps}$ are inserted to avoid the oscillation problem.

The resulting output current $I_O$ and the transconductance $G_M$ become

\[
\begin{align*}
I_O &= K \left( V_P - \frac{V_{DIN}}{4} - V_T \right) V_{IN}' \\
G_M &= K \left( V_P - \frac{V_{DIN}}{4} - V_T \right)
\end{align*}
\] (20) (21)
3. Computer Simulation

In order to confirm the validity of the proposed method, simulation is carried out using the PSpice simulator. Channel width and channel length of the MOSFET’s are summarized in Tab.1. The element value of the capacitor $C_P$ is 2pF. Figure 8 shows the $I_O-V_{IN}$ characteristics corresponding to conditions $V_P=2.5V$ ($V_{DD}-V_{SS}=5V$) and $V_{DIN}=0V$ at room temperature. From this figure, it is found that we can decrease the offset current by using the proposed method.

In this paper, a linear input voltage range is defined by the input voltage range where the transconductance deviation is within ±1%. Figure 9 shows the transconductance characteristics. This figure indicates that the linear input voltage ranges are $2.1V_{P-P}, 1.9V_{P-P}$ and $1.6V_{P-P}$ for $V_{DIN}=0V, \pm0.25V$ and $\pm0.5V$, respectively. Moreover, it is found that the transconductance can be electrically controlled by varying $V_{DIN}$.

Table 2 summarizes comparison of power consumption. From this figure, we find that total power consumption of the proposed transistor is higher than that of the conventional one. However, power consumption of the proposed transconductor without the control circuit is 48.0% as low as that of the conventional one. Generally, when we apply the transconductors to the analog filter, some of the transconductors may be fabricated on the same IC chip. In this case, the required number of the proposed control circuit is only one. Therefore, it can be concluded that the amount of power consumption of the analog filter realized by using the proposed transconductors becomes lower than that of the conventional one when 2 or more transconductors are fabricated on the same IC chip.

4. Conclusions

In this paper, a linearized transconductance amplifier using a CMOS complementary pair is proposed. How to cancel the offset current is proposed. And, how to control the transconductance is described. It is shown that power consumption of the proposed transistor is lower than that of the conventional one when 2 or more transconductors are fabricated on the same IC chip.

The further investigation is required to apply the proposed transconductor to an analog filter.

References