High Speed 2D Discrete Cosine Transform Processor

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Abstract

On modern computer culture, the high quality data is required in multimedia systems. So, the technology of data compression for data transmission is necessary now.

This paper presents the pipeline architecture for the low and column address generator of 2D DCT/IDCT (Discrete Cosine Transform/Inverse Discrete Cosine Transform. In the proposed architecture, the area of hardware is reduced by using the DA (distributed arithmetic) method and applies the concepts of pipeline to the parallel architecture.

As a result, the designed pipeline of the low and column address generator for 2D DCT/IDCT architecture is implemented with an efficiency and high speed compared with the non-pipeline architecture.

1. Introduction

Today, we are living in the continuous flood of information and intricate pieces of machinery. Most of the people want quick electronic systems that they can get necessary information to their work. And mobile, portable and battery are popular, and they are designed on small and convenient.

Among the efficient techniques of data compress, DCT (discrete cosine transform) reported in 1974 is superior to other techniques, which was adapted as a basic algorithm of image compress in International Standardization Group, and is widely applied in the field of signal treatment. And IDCT (Inverse Discrete Cosine Transform) is also popular in JPEG and MPEG as a technique of image restoration.

DCT/IDCT block in this paper is a main operation block with large amount of operation of which block is generally executed by using multipliers. Then, a multiplier is required with large capacity of hardware executed, and slower operation speed. To increase the operation speed, the authors designed the high speed DCT/IDCT by using DA (distributed arithmetic) technique by Chen algorithm using ROM table instead of multiplier, and row-column decomposition for transposition memory access is performed. [1,2]

For the high speed DCT/IDCT, the authors designed 2D DCT/IDCT with DA and pipeline architecture with a high speed adding operation. In the case that DA is used because the accumulator is required the operation speed of the accumulator affects the slow performance of 2D DCT/IDCT.

2. A Theoretical Background of DCT/IDCT

DCT algorithm is an effective coding system in which image data are transformed into transforming area. For IDCT, data of transform-area are transformed into image data.

A method to realize 2D DCT is categorized into tow areas: RCA (row and column algorithm), that is a technique of low and column decomposition using decomposing characteristics of 2D DCT through two 2D DCT and row-column transposition. In this case, 1D DCT/IDCT is performed in row direction of 2D image and then the results are transposed by transposition memory access before 1D DCT/IDCT is performed again in column direction. This technique has two advantages: one is RCA (row column algorithm), through which structure is simplified as 2D DCT/IDCT is operated from 1D DCT/ IDCT and high-speed operation is expected as it is associated with distributed arithmetic. The other is NRCA (no row column algorithm), in which high-speed algorithm is directly induced f0rom 2D DCT architecture to realize 2D DCT instead of discomposing characteristic.

Distributed arithmetic method is very effective in executing internal operation of input data value and fixed coefficient value. With this method, multiplication is performed using register and accumulator without multiplier. So it is considered as simple and regular to execute and reduce size of hardware. These days, distributed arithmetic has been recognized as more effective in realizing DCT as hardware and results of many studies on DCT architecture based on distributed

arithmetic have been published.

General Eq. (1) and (2) of 1D DCT/IDCT are presented: [3]

$$F(k) = \frac{1}{4}C(K)\sum_{m=0}^{N-1} f(m)\cos[(2m+1)K\pi/16] \quad ...(1)$$

$$f(m) = \frac{1}{4}C(K)\sum_{m=0}^{N-1} f(k)\cos[(2m+1)K\pi/16] \quad .....(2)$$

$$C(K) = \begin{pmatrix} 1/\sqrt{2}, K = 0 \\ 1, C = 1,2,\ldots 7 \end{pmatrix}$$

A general row-column Equation of 1D DCT presented above is given in Eq. (3):

$$\begin{bmatrix} X_e \\ X_o \end{bmatrix} = \begin{bmatrix} C_{N/2} & C_{N/2} \\ S_{N/2} & -S_{N/2} \end{bmatrix} \begin{bmatrix} x_f \\ x_r \end{bmatrix}$$

$$\begin{bmatrix} x_f \\ x_r \end{bmatrix} = \begin{bmatrix} C'_{N/2} & C_{N/2} \\ C'_{N/2} & -S_{N/2} \end{bmatrix} \begin{bmatrix} X_e \\ X_o \end{bmatrix} \quad .....(3)$$

And 1D DCT/IDCT is implemented at 2D DCT/IDCT in a row or column direction and the row and then column algorithm is transposed. 1D DCT/IDCT is implemented at the results in a column or row direction. Chen algorithm reduces unnecessary repetitive operation using periodical characteristic of cosine and is presented in Eq. (4) and (5):

$$\begin{bmatrix} X0 \\ X2 \\ X4 \\ X6 \end{bmatrix} = \begin{bmatrix} A & A & A & A \\ B & C & -C & -B \\ A & -A & -A & A \\ C & -B & B & -C \end{bmatrix} \begin{bmatrix} x0+x7 \\ x1+x6 \\ x2+x5 \\ x3+x4 \end{bmatrix} \quad .....(4)$$

$$\begin{bmatrix} X1 \\ X3 \\ X5 \\ X7 \end{bmatrix} = \begin{bmatrix} D & A & F & G \\ E & -G & -D & -F \\ F & -D & G & E \\ G & -F & E & -D \end{bmatrix} \begin{bmatrix} x0-x7 \\ x1-x6 \\ x2-x5 \\ x3-x4 \end{bmatrix}$$

$$\begin{bmatrix} X0 \\ X1 \\ X2 \\ X3 \end{bmatrix} = \begin{bmatrix} A & B & A & C \\ A & C & -A & -B \\ A & -C & -A & B \\ A & -B & A & -C \end{bmatrix} \begin{bmatrix} X0 \\ X2 \\ X4 \\ X6 \end{bmatrix} + \begin{bmatrix} D & E & F & G \\ E & -G & -D & -F \\ F & -D & G & E \\ G & -F & E & -D \end{bmatrix} \begin{bmatrix} X1 \\ X3 \\ X5 \\ X7 \end{bmatrix} \quad .....(5)$$

$$\begin{bmatrix} x7 \\ x6 \\ x5 \\ x4 \end{bmatrix} = \begin{bmatrix} A & B & A & C \\ A & C & -A & -B \\ A & -C & -A & B \\ A & -B & A & -C \end{bmatrix} \begin{bmatrix} X0 \\ X2 \\ X4 \\ X6 \end{bmatrix} - \begin{bmatrix} D & E & F & G \\ E & -G & -D & -F \\ F & -D & G & E \\ G & -F & E & -D \end{bmatrix} \begin{bmatrix} X1 \\ X3 \\ X5 \\ X7 \end{bmatrix}$$

After an operation of this equation, when the same operation is executed on the transposed row and column, the result of 2D DCT/IDCT is presented. In Eq. (4) and (5), number of multiplication is reduced through an addition and a subtraction of the same row and column. Therefore, it is sure that number of multiplication is reduced.

3. Realization of DCT/IDCT

The results of operation of 1D DCT/IDCT by 2D DCT/IDCT are saved in transpose RAM. Through transpose row-column access, when operation of 1D DCT/IDCT is performed, the results are a result of 2D DCT/IDCT. Architecture of 2D DCT/IDCT is presented in Fig. 1.

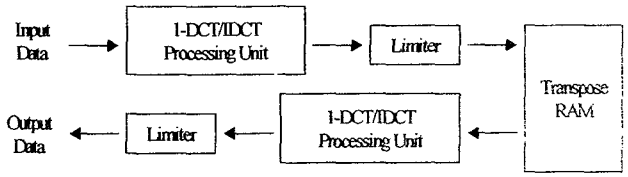


Fig. 1. Architecture of 2D DCT/IDCT

In Fig. 1, instead of multipliers, data saved in ROM table are used to realize a distributed arithmetic technique. As A_kX_k of Eq. (6) and (7) are internal, distributed arithmetic can be applied.

$$y = \sum_{k=1}^{K} A_k X_k \quad ..... \quad (6)$$

In Eq. (6), when X_k is expressed with complementary number of 2, the equation is presented in Eq. (7):

$$X_k = -b_{k0} + \sum_{n=1}^{N-1} B_{kn} 2^{-n} \quad ..... \quad (7)$$

$$y = \sum_{k=1}^{K} A_k \left[-bk\,0 + \sum_{n=1}^{N-1} 2^{-n} \right]$$

$$y = \sum_{n=1}^{N-1} \left[\sum_{k=1}^{K} A_k b_{kn} \right] 2^{-n} + \sum_{k=1}^{K} A_k (-b_{k0}) \quad ..... (8)$$

In Eq. (8), as b is value of 0 or 1, 2^k combination can be applied to the first term of right side. And as b_{ko}, second term of right side, is MSB, y value can be operated when value of 2×2^k is memorized. K bit is address of ROM table that memorizes value of 2×2^k and when consecutive addition with shift of N-1 is made, the operation is completed. And the size of ROM table for signal bit increases twice and when the table becomes address, subtraction instead of addition brings reduction of ROM size to 2^k. A flow chart of 1D DCT/IDCT is presented in Fig. 2.

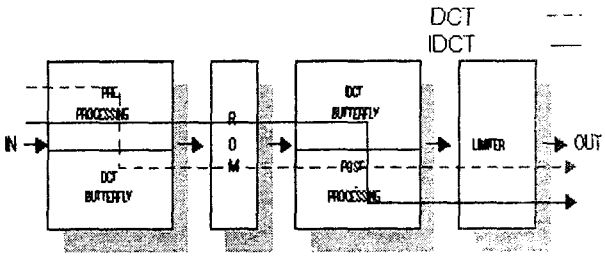
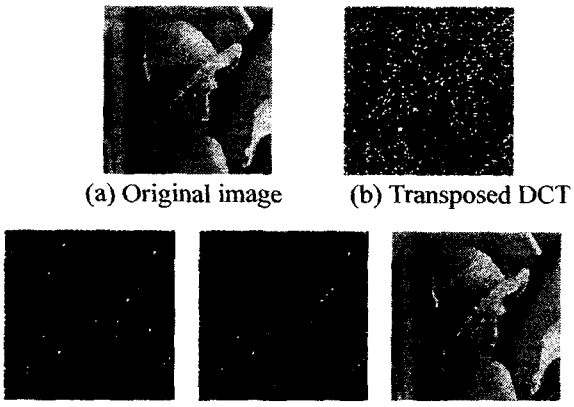


Fig. 2. Block Flow of 1D DCT/IDCT

In Fig. 2, input data is approved in parallel through register of pre-processor and then they pass DCT operation and then through butterfly section for arrangement of input column during IDCT operation. After that, data pass ROM table and DCT passes through pose-processor via butterfly section while IDCT passes by butterfly section and then passes through post-processor. And then it outputs 16 bits after it passes through a limiter.

4. Experimental Results

To verify 2D DCT/IDCT algorithm using DA for this scheme proposed, 2D DCT/IDCT transformed picture of Lena image are shown in Fig. 3. In here, (a) is original image, (b) is transposed DCT, (c) is quantization from transposed DCT, (d) is entropy coding from (c), and (e) is shown transposed IDCT from (d).



(a) Original image (b) Transposed DCT

(c) Quantization (d) Entropy Coding (e) Transposed IDCT

Fig. 3. 2D DCT/IDCT transformed picture of Lena images using DA scheme proposed.

Through the simulation results in this scheme, the authors proved that the algorithm was improved about 0.053 for MSE(Mean Square Error) at Lena image. Table 1 is compared results as the conventional DCT/IDCT and 2D DCT/IDCT using DA.

Table 1. Compared results with the Conventional DCT/IDCT and 2D DCT/IDCT using DA.

	MSE	PSNR[dB]
Conventional DCT/IDCT	33.262461	32.911260
2D DCT/IDCT using DA	33.209355	32.918199

In this scheme, it is examined the adders constructed in many ways as proposed in Table 2. When 32bits adder was constructed, bit was divided into 4-4-5-6-7-6 and ripple adders were used to reduce a delay to 4+1+1+1+1(=9). Bit was divided into 1-2-3-4-4-5-6-7 to reduce a delay to a rough value. However, a circuit where Ripple Carry Adders are added to Carry Select Adders was designed for a short circuit and speedy calculation. The synthesis result of 32bits adder proposed is shown in Fig. 3.

Table 2. Compared characteristics between the conventional and proposed adder.

Adder (32bit)	A number of gate	Timming(ns)
ripple carry adder	378	57.53
ripple carry (chain)	493	31.73
carry select adder	639	28.70
Transform carry select adder	651	25.56
4,4,5,6,7,6 bit ripple adder	669	29.29
1,2,3,4,4,5,6,7bit ripple adder	675	30.37
Suggest 32bit adder	669	20.88

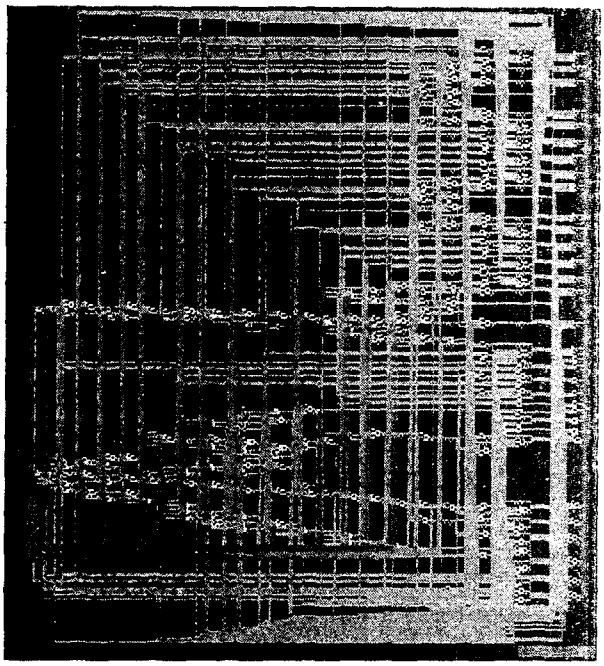


Fig. 3. Synthesis result of 32bit adder proposed.

In this paper, simulation and synthesis of all circuits were performed by Synopsys design tool. For target library, xcv300 produced by Xilinx was used. Xilinx foundation was used for 2.1 P&R tool. Synopsys VSS was used for timing of the system. The maximum clock speed was 36.232MHz and the operation speed of stable state was about 33.341Mhz. The size of the synthesized circuit has 45,644 gates.

The entire block of 2D DCT/IDCT and the result of synthesis are each shown in Fig. 4. And Table 3 is the compared results with as the non-pipeline architecture.

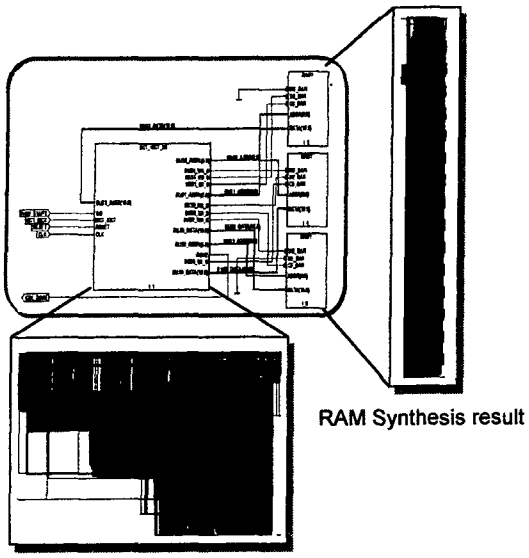


Fig. 4. Top level of 2D DCT/IDCT and synthesis results 2-D DCT/IDCT.

Table. 3. Compared operation time between the architecture of non-pipeline 1D and 2D pipeline.

	8×8 operation speed(ns)
Non-pipeline 1D	10495(Row)+10495(Column)
Used 2D pipeline	13991

5. Conclusions

In this paper, DA and the pipelining techniques are used to design the improved elements of 2D DCT/IDCT. Because the accumulator causes low performance of the system, by using DA, the accumulator would be needed only one. To increase speed of the operation, a new adder and pipeline architecture is designed. A new adder, in which Ripple Carry Adder is combined with Carry Selector Adder to consider the efficiency of area and high speed of multiplication respectively. As for this new adder, area cost increases about 1.05 times but the operation speed increases about 1.2 times. And this paper presents the pipeline architecture for the row and column address generator of 2D DCT/IDCT using DA. That is, 2D is divided into 1D and 1D each other and they are applied as a concept of pipeline to increase the operation speed about 66.6%.

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