A 16-bit adiabatic macro blocks with supply clock generator for micro-power RISC datapath

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Abstract: A 16-bit adiabatic datapath for micro-power RISC processor is designed. The datapath is composed of a 3-read and 1-write multi-port adiabatic register file and an arithmetic and logic unit. A four-phase clock generator is also designed to provide supply clocks for adiabatic circuits and the driving capability control scheme is proposed. All the clock line charge on the capacitive interconnections is recovered to recycle energy. Adiabatic circuits are designed based on efficient charge recovery logic(ECRL) and are implemented using a 0.35 μm CMOS technology. Functional and energy simulation is carried out to show the feasibility of adiabatic datapath. Simulation results show that the power consumption of the adiabatic datapath including supply clock generator is reduced by a factor of 1.4 ~ 1.5 compared to that of the conventional CMOS.

1. Introduction

In recent years, studies on adiabatic computing have been grown for low power systems [1-7] such as hand held computers and PDAs. A method based on adiabatic technique uses an AC power supply for the recovery of energy and an efficient supply clock generator is essential to show the feasibility of adiabatic circuits.

A datapath for a 16-bit RISC microprocessor is designed based on the adiabatic concept and an efficient clock generator with controllable driving capability for adiabatic circuits is also designed.

2. Design of 16-bit adiabatic datapath

ECRL(Efficient Charge Recovery Logic) [8] type adiabatic logic families are used in this paper and AC-type supply clocks are needed to supply power. Adiabatic circuits require four-phase sinusoidal clocks for cascading logic stages. ECRL adiabatic circuits use a differential signal scheme, and the basic ECRL gate is shown in Figure 1.

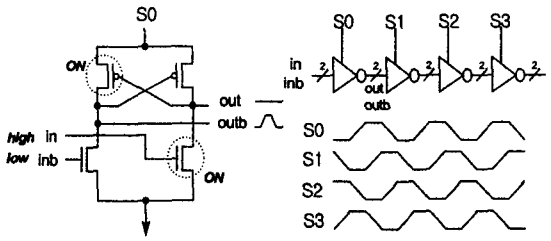

Figure 1. The basic structure of ECRL circuit

The datapath consists of an ALU(arithmetic and logic unit) and a multi-port register file. The block diagram of the datapath is shown in Figure 2. The subtraction operation needs a carry input signal and inversion gates so the subtraction result is obtained in seven phases. The gate count optimization is performed to reduce the power consumption. The total gate number of the proposed adder is reduced by a factor of 10% compared to the previous adiabatic adder.[8]

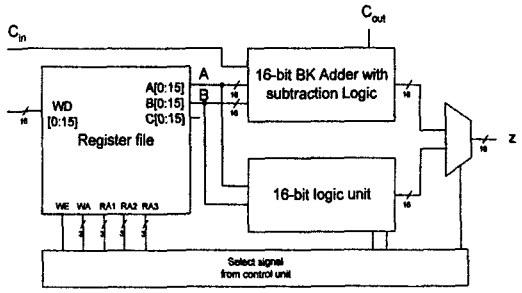

Figure 2. The structure of adiabatic datapath

The operations of logic unit are AND, NAND, OR, NOR, XOR and NOT, and the adder is designed based on Brent-Kung adder.[9] The lower 4-bit block diagram of arithmetic unit is shown Figure 3. The schematic of the PG generator for the adder and the logic unit is shown in Figure 4 and Figure 5. Though the logic operation is performed in single phase, 2-phases are needed to pass MUX's and additional buffer phases are inserted to synchronize with the output of the adder. The output of each unit passes the final MUX so that total 8-phases(2-clocks) are needed to get the final result of the ALU.

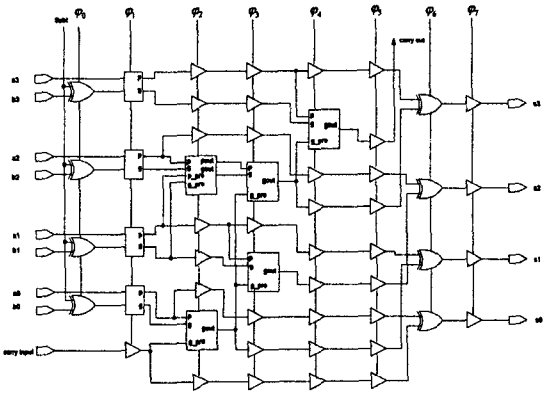

Figure 3. The lower 4-bit block diagram of arithmetic unit

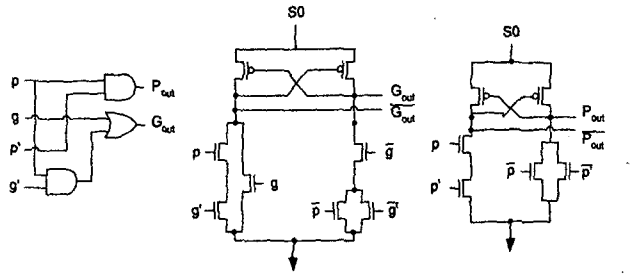

Figure 4. The schematic of PG generator

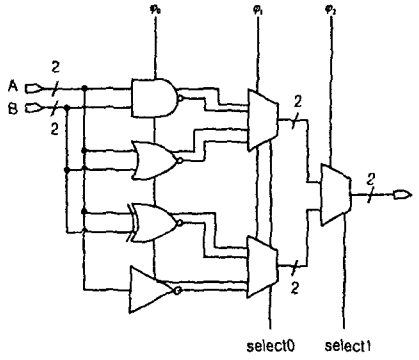

Figure 5. The schematic of logic unit

The 3-read and 1-wirte multi-port register file is designed in adiabatic manner to reduce energy. The cell structure of multi-port register file is shown in Figure 6. A 3-bit is used for register addressing and cross-coupled PMOS is used as a sense circuit to recover the charges in bit-lines. The write operation needs 2 phases and the read operation is composed of 3 phases. The read operation has an one-phase delay from the beginning of the write operation, so reading the changed data in the same cycle is possible in this register file.

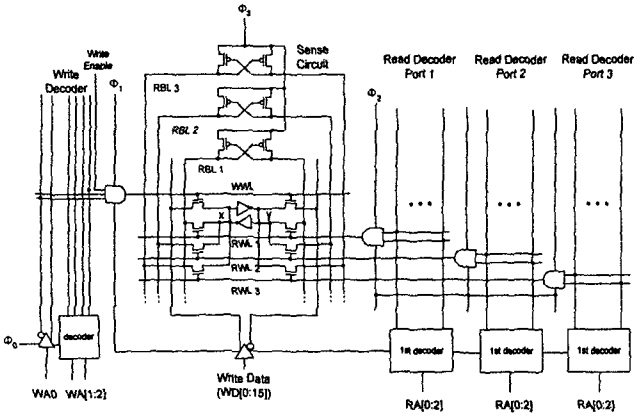

Figure 6. The structure of adiabatic register

3. Supply clock generator

The AC supply is needed to return the delivered energy back to the supply efficiently. The LC resonant circuit is used to supply 4-phase supply clocks. It consists of one inductor, two capacitors and MOS switches. The switch transistors shown in Figure 7 are connected to the supply and are used to maintain the swing of supply clocks by compensating the energy loss.

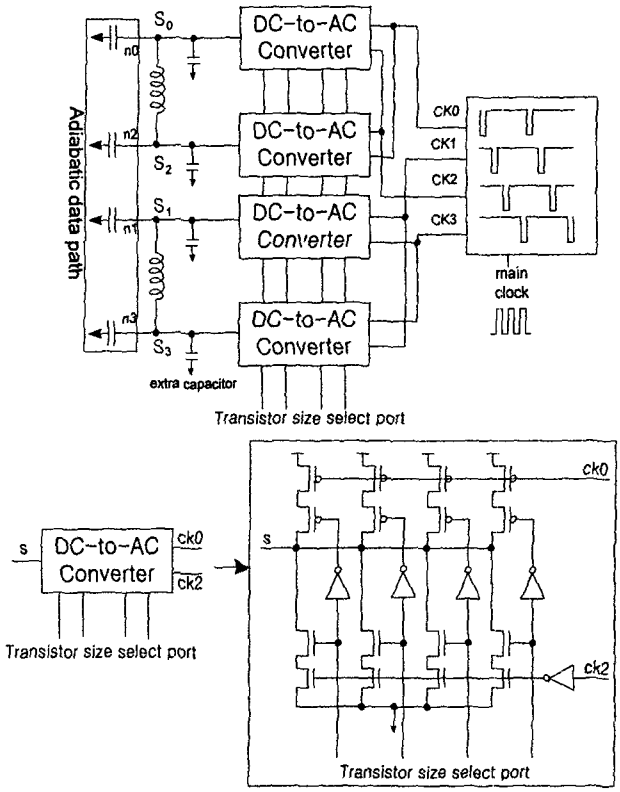

Figure 7. The block diagram of supply clock generator

The operating frequency of datapath is determined by the resonant frequency calculated from the external inductance and the equivalent capacitance of the supply clock node. The equivalent capacitance of the supply clock node is calculated using the equation $T = RC_{eq}$. Table 1 shows the calculated equivalent capacitances of supply clock nodes for adiabatic datapath.

Since the equivalent capacitances of the supply clock nodes are different, small external capacitors are added to match the capacitances of the supply clock nodes. The amplitude of the supply clock grows as the DC power supplies energy through the MOS switches.

Table 1. The equivalent capacitance of supply clock node

node	S0	S1	S2	S3
C_{eq} [pF]	1.67	2.80	1.16	2.26

4. Simulation and results

The 16-bit adiabatic datapath is designed using a 0.35μm CMOS technology, and SPICE simulation is carried out using the layout extracted net-list. A CMOS datapath with a single-ended signal scheme is also designed to compare the power consumption.

The efficiency of the supply clock generator is varied according to the size of switching transistors, and is simulated by varying the combination of the switching transistors. The size of the switching transistor increases as the operation frequency goes up. This trend shows that the larger current is needed for the higher frequency operation. The optimal sizes of NMOS switching transistors are listed in Table 2.

Table 2. The width of NMOS switching transistor at maximum energy efficiency

frequency [㎒]	10	20	50	100	200
Width[㎛]	3	10	15	35	50

The operation of register file is shown in Figure 8. Reading operations are carried out for each read port, after writing '10100110' to the register sequentially.

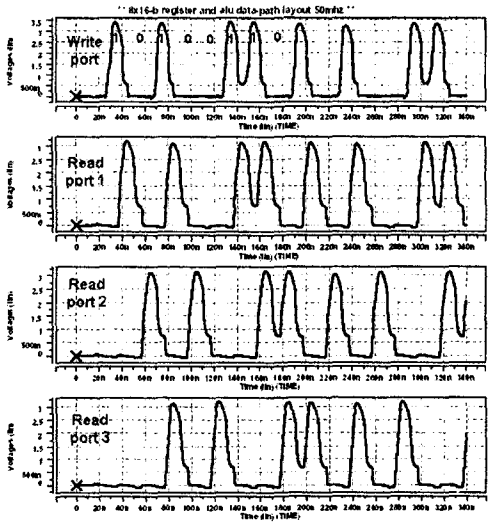

Figure 8. The simulation result of multi-port adiabatic register file

The operation of ALU is shown in Figure 9. The 1st and 2nd plot show the outputs of arithmetic unit and logic unit. The 3rd plot shows one output of two blocks according to select signal.

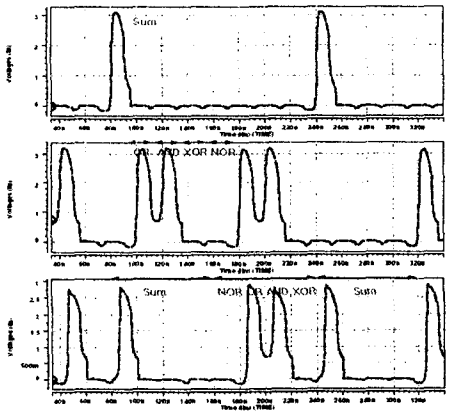

Figure 9. The SPICE simulation result of data path

A 16-bit adiabatic macro block layout is shown Figure 10. A 0.35 ㎛ CMOS 1-poly and 3-metal process is used and the area of proposed macro block is about 0.617 ㎜ x 0.944 ㎜. The area under the register file is reserved for shift block.

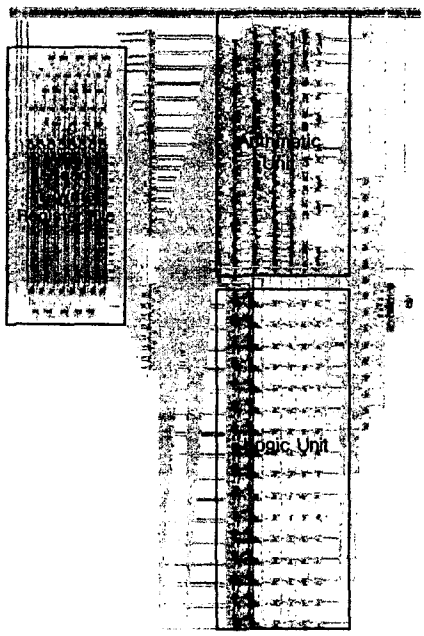

Figure 10. A 16-bit adiabatic macro block layout

The energy consumption of the ECRL and the conventional CMOS ALU part is compared in Figure 11. The energy consumption of the adiabatic ALU is about 68%~72% of that of CMOS

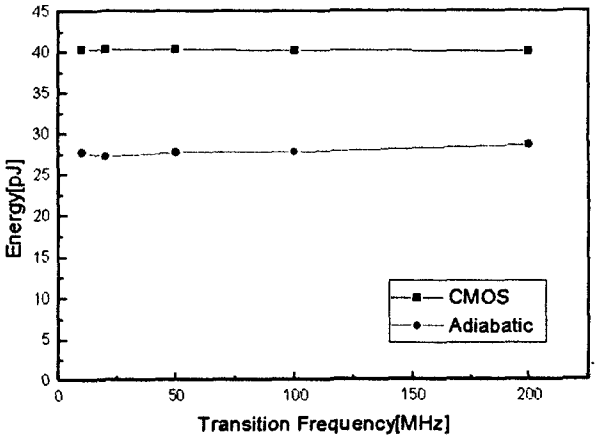

Figure 11. Energy versus transition frequency for ALU

5. Conclusions

An adiabatic macro block and a supply clock generator are designed using a 0.35 ㎛ CMOS technology. The energy and functional simulation is performed using the net-list extracted from the layout. The energy gain of the adiabatic ALU is improved by a factor of 1.4~1.5 compared to that of

the conventional CMOS. The proposed design methodology of adiabatic circuits is applicable and feasible to the micro-power microprocessors.

Acknowledgement

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