An Ultra-High Speed 1.7ns Access 1Mb CMOS SRAM macro

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Abstract: This paper describes a 0.13um ultra-high speed 1Mb CMOS SRAM macro with 1.7ns access time. It achieves ultra-high speed operation using two novel approaches. First, it uses process insensitive sense amplifier (Double-Equalized Sense Amplifier) which improves voltage offset by about 10 percent. Secondly, it uses new replica-based sense amplifier driver which improves bit-line evaluation time by about 10 percent compared to the conventional technique. The various memory macros can be generated automatically by using a compiler, word-bit size from 64Kb to 1Mb including repairable redundancy circuits.

Introduction

There have been many approaches to achieving high performance SRAM for years. Sense amplifier was an important issue because endurance against process mismatches affects bit-line swing and bit-line evaluation time[1][2]. Sense amplifier driver circuit has been recently discussed with respect to the performance insensitiveness to the operation conditions[3]. Especially in the low operating voltage, the driver circuit sensitiveness to the operation conditions becomes worse, resulting in the reduction of SRAM performance. In this paper we propose robust sense amplifier and driver circuits for high-performance SRAM to reduce access time significantly.

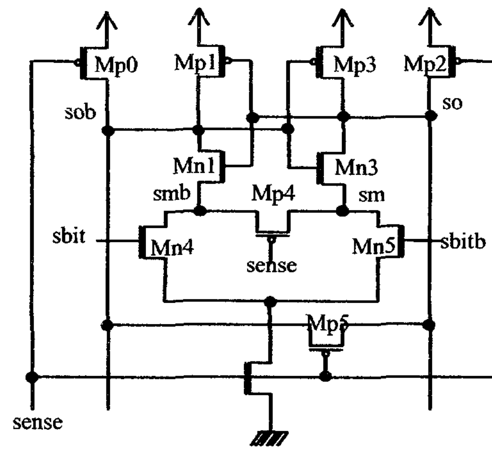
A New Sense Amplifier
(Double-Equalized Sense Amplifier)

A conventional differential latch type sense amplifier (Fig.1-a) has some merits compared to the other types of sense amplifier. For example, it has the simplicity of functionality compared to double-stage or triple-stage sense amplifier and for this reason, it occupies a small area and evaluates fast the bit-cell data. But it has the disadvantage to be sensitive to process mismatches. So, that type of sense amplifier requires the minimum voltage offset to recover the process unbalances, such as the threshold voltage, parasitic capacitance, transconductance mismatches. And the minimum voltage offset which is required to amplify the correct data of bit-cell affects the timing and power performance of memory very significantly.

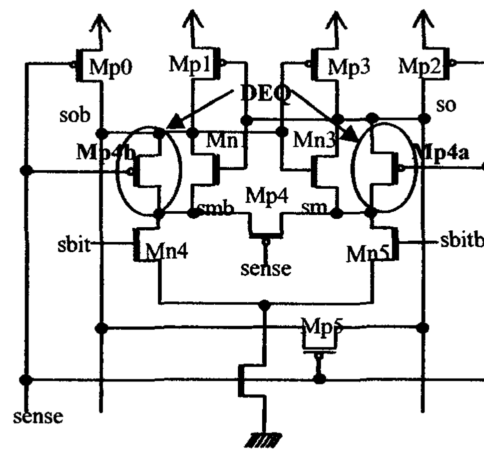
In the viewpoint of process mismatches, we proposed a new type of differential sense amplifier to reduce the minimum voltage offset. The proposed sense amplifier(Fig.1-b) has the similar shape except that it has the two additional transistors, called Double-Equalizing PMOSs(DEQ). To explain the role of DEQ, let's assume that there is a threshold mismatch between two balanced TRs (Mn1,Mn3). Fig.2 shows the conventional graph of Ids vs. Vds and Vgs NMOS according to the following expressions.

$$Ids=\beta[(Vgs-Vth)Vds-Vds^2*0.5] \quad \text{if } 0<Vds<Vgs-Vth \quad (1)$$
$$Ids=\beta[(Vgs-Vth)^2*0.5] \quad \text{if } 0<Vgs-Vth<Vds \quad (2)$$
$$\text{where } \beta=(\mu*\varepsilon/tox)*(W/L)$$

Also, there is an Ids difference between Mn1 and Mn3 because there is a Vth mismatch between Mn1 and Mn3. (in Fig.2 , solid line shows Ids graph of (-)ΔVth and dot line shows Ids graph of (+)ΔVth vs. Vds,Vgs).



(a) Conventional



(b) Proposed

Fig. 1 The differential latch type sense amplifier

And then from the graph, we can find out that ÄIds is small in the area where Vds and Vgs are simultaneously small. If we want to reduce the influence of Vth mismatch, we must operate the two NMOS Mn1,Mn3 in the area where Vds is small. The DEQ can keep the two internal nodes (drain and source of the latch NMOSs of the sense amplifier) same potential until the sense amplifier is enabled, and it enables the process mismatches of the latch NMOSs to be unlikely to affect the operation of the sense amplifier.Table 1 shows the minimum voltage offset of the conventional and the proposed DEQ sense amplifier under the various process mismatches. We could reduce the minimum voltage offset of the sense amplifier to endure the process imbalances by DEQ TRs. And it could help to improve the delay time from a memory cell to data out from 730ps to 600ps.

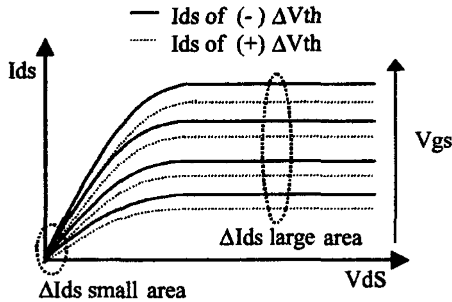


Fig. 2. Ids vs.Vds and Vgs
(The Vth of two NMOSs is different for process mismatch)

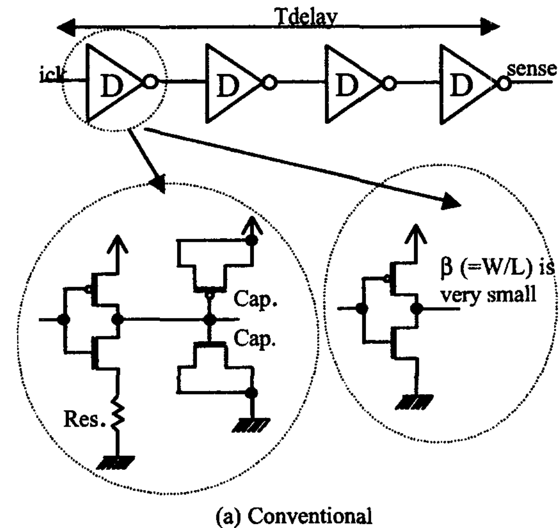
@1.2V, 25°C,process=NN, mismatch=5%

Case		mn1 mn3	mn mn5	mp0 mp2	mp1 mp3	mp4a mp4b	Cso Csob	Csm Csmb	Conv	DEQ
NO	1	X	X	X	X	X	X	X	45mV	35mV
Width	2	O	X	X	X	X	X	X	48mV	35mV
	3	X	O	X	X	X	X	X	55mV	45mV
	4	X	X	O	X	X	X	X	47mV	36mV
	5	X	X	X	O	X	X	X	46mV	35mV
	6	X	X	X	X	O	X	X	45mV	39mV
length	7	O	X	X	X	X	X	X	61mV	44mV
	8	X	O	X	X	X	X	X	60mV	52mV
	9	X	X	O	X	X	X	X	47mV	37mV
	10	X	X	X	O	X	X	X	46mV	35mV
	11	X	X	X	X	O	X	X	45mV	37mV
Cap.	12	X	X	X	X	X	O	X	65mV	46mV
	13	X	X	X	X	X	X	O	53mV	44mV

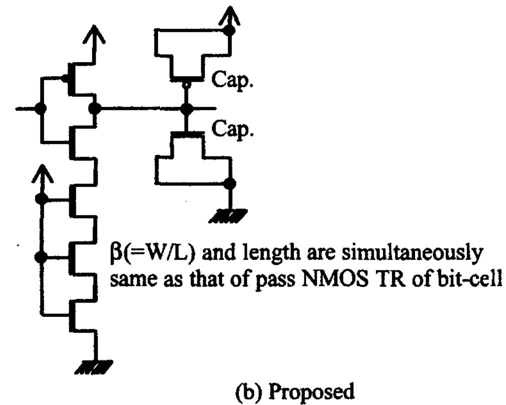
Table.1. The minimum voltage offset of conventional and proposed(DEQ) sense amplifier under the various process mismatch cases.(X : no mismatch , O : mismatch)

A New Replica-Based Sense Amplifier Driver Circuit

The SRAM used in ASIC applications must guarantee the memory stability under the commercial or industrial operating voltage, temperature and process ranges. The conventional sense amplifier driver circuits can be implemented in the peripheral area of memory block using the devices of large resistance and capacitance(Fig.3-a). The above approach has the characteristic that it generates the sense amplifier activating signal after the voltage swing of the bit-line reaches the enough level under the various conditions. However, in this approach, it is hard to design the sense amplifier driver because the time variations of delay cells change very much through the various conditions.



(a) Conventional



(b) Proposed

Fig.3 Sense amplifier driver circuits

Let's call the sense amplifier activating time as Tdelay and the bit-line evaluation time as Tbit. Generally, we design the sense amplifier driver circuits at the worst condition which Tbit is largest and Tdelay is smallest among all conditions we take care of. But, the condition of the minimum voltage offset being worst in the sense amplifier is not same as that of bit-cell evaluation time being worst. For example, even thought the sense amplifier driver circuit is designed to track the bit-cell evaluation very well under a certain condition, it may unnecessarily slow down the

access time at the other condition. To solve this problem, we propose the new replica-based sense amplifier driver circuit(Fig.3-b). The proposed sense amplifier driver circuit can track well the bit-cell evaluation at all conditions and improve the access time while guaranteeing the memory stability.

Basically, we know that β(=W/L) of delay cell must be equal to that of TRs in bit-cell in order to track the DC characteristics of the bit-cell. And by an experiment, we find out that currents (Ids) of MOSs can change most likely under the various conditions when they have the same length(L). So, we implement the new approach which is composed of 3~5 series NMOS TRs with the length same as that of bit-cell pass TR in order that series NMOSs of delay cell have the same β(=W/L) ratio as that of a bit-cell pass TR. To verify whether the new sense amplifier driver circuit tracks the bit-line evaluation time very well, we assume the conditions of voltage, temperature and process like Table.2. Table.2 shows the corner conditions of voltage, temperature and process in 0.13um technology.

Condition	Voltage	Temp.	PROCESS	
			NMOS	PMOS
1	1.35V	-55°C	FAST	FAST
2	1.35V	-55 °C	FAST	SLOW
3	1.35V	-55 °C	SLOW	FAST
4	1.35V	-55 °C	SLOW	SLOW
5	1.35V	125 °C	FAST	FAST
6	1.35V	125 °C	FAST	SLOW
7	1.35V	125 °C	SLOW	FAST
8	1.35V	125 °C	SLOW	SLOW
9	1.05V	-55°C	FAST	FAST
10	1.05V	-55°C	FAST	SLOW
11	1.05V	-55°C	SLOW	FAST
12	1.05V	-55°C	SLOW	SLOW
13	1.05V	125°C	FAST	FAST
14	1.05V	125°C	FAST	SLOW
15	1.05V	125°C	SLOW	FAST
16	1.05V	125°C	SLOW	SLOW

Table.2. The corner conditions of voltage, temperature, process in 0.13um technology

Fig. 4 shows the sense amplifier delay and the bit-cell evaluation delay under the conditions shown in Table 2. The conventional sense amplifier driver circuit shows the sense amplifier worst condition at condition11 and the difference between Tbit and Tdelay at condition16 is 123%. But the proposed replica-based one shows the sense amplifier worst condition at condition15 and the difference at condition16 is 111%. So, we can reduce bit-line evaluation time by 10% at worst condition16 using the proposed replica-based sense amplifier driver.

Conclusions

An ultra-high speed 1.7ns access 1Mb CMOS SRAM macro with 1.57x2.05 mm^2 was developed using 0.13um CMOS ASIC technology. We propose new DEQ sense amplifier circuit and replica-based sense amplifier driver circuit to achieve the ultra-high performances. With the two novel circuits, we could reduce the access time by more than 15%. The various memory macros can be generated by using a compiler, word-bit size from 64Kb to 1Mb including repairable redundancy circuits. Table 3. shows the features of the SRAM macro. Fig. 5. shows micrographs of 1Mb macro.

References

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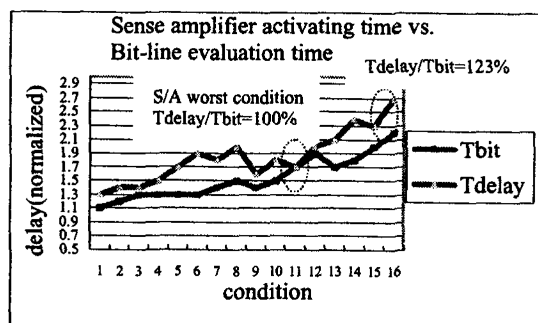
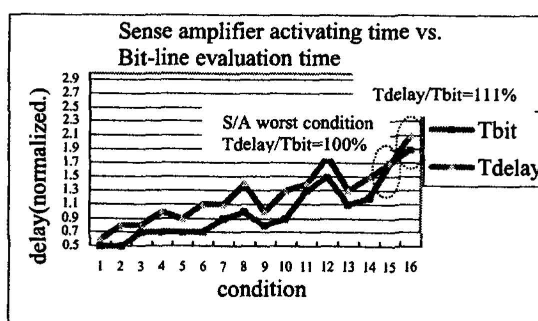
[2] Ali Hajimiri et al., "Design Issues in Cross-Coupled Inverter Sense Amplifier", *ISCAS '98, Vol. 2,* pp.149-152, 1998.

[3] Bharadwaj S Amrutur et al., "A Replica Technique for Wordline and Sense Control in Low-Power SRAM's", *IEEE J.Solid-State Circuits,Vol.33,* pp.1208-1219, 1998.



(a) conventional



(b)proposed

Fig.4 Sense amplifier driver delay(Tdelay) vs. bit-line evaluation delay(Tbit) under corner conditions.

(Condition : 1.2V, 25°C, process=typical)

Word depth	2048 – 32768
Bit per word	32 – 128
Clock Acces Time	1.3ns – 1.7ns
Operating Freqency	512MHz – 662MHz
Power dissipation @1MHz	58uW - 225uW

Table. 3. Features of the SRAM Macro

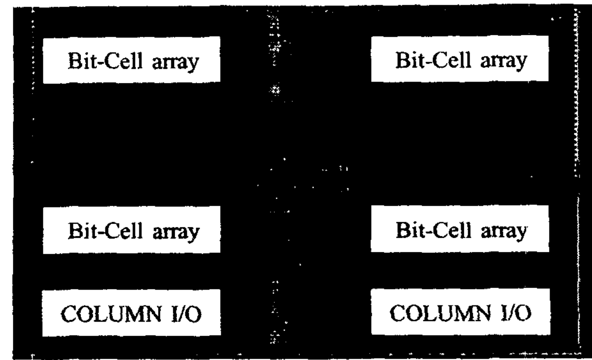


Fig.5. Micrographs of the 1Mb SRAM macro