Sense Amplifier Design for A NOR Type Non-Volatile Memory

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Abstract: We have investigated the precharge type sense amplifier, it is suitable for voltage sensing in a NOR type single transistor ferroelectric field effect transistor (1T FeFET) memory read operation. The proposed precharge type sense amplifier senses the bit line voltage of 1T FeFET memory. Therefore, the reference cell is not necessary compared to current sensing in 1T FeFET memory. The high noise margin is wider than the low noise margin in the first inverter because requires the output of precharge type sense amplifier high sensitivity to transition of input signal. The precharge type sense amplifier has very simple structure and can sense the bit line signal of the 1T FeFET memory cell at low voltage.

1. Introduction

It is very important circuit to sense amplifier (SA) in memories read circuits. The SA senses the bit line signals of the memories and determines the outputs of the memories. The SA is used to retrieve the stored data in the memory array by amplifying small signal variations on the bit lines. Many current modes SAs have been presented in the open literature [1, 2]. The precharge type SA precharges the bit lines signals of the memories for the precharge time and senses for the evaluation time. The precharge type SA is not suitable for high-speed operation circuit in NAND type memories for long precharge time. So, the sizes of precharge transistors in NAND type memories are very large in order to fast precharge time. But, the precharge type SA is suitable for high speed operation circuit in NOR type memories with suitable sizes of precharge transistors. And, the precharge type SA has very simple circuit and very easy senses the bit lines signals of memories. The 1T FeFET memory has a great advantage for memory since it has not only nonvolatile characteristics but also fast memory access time [3-5]. The 1T FeFET memory has NOR types structure in this paper. It can store data using hysteresis characteristic and polarization reversal between voltage and accumulated electric charge. We propose the precharge type SA for a NOR type 1T FeFET memory.

2. Design of precharge type SA circuit

The in/output of a precharge type SA has HIGH(VDD) for the prechagre time, and senses a bit line signals of memory cell for the evaluation time. Fig.1 shows the proposed precharge type SA for the 1T FeFET memory.

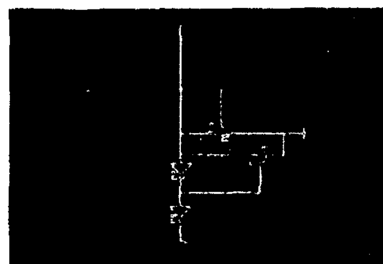

Fig. 1 The precharge type sense amplifier circuit

It is composed of two input signals, one output signal, two pull-up P-type MOSFETs (MP1, MP2), and two inverters (INV1, INV2). When is the enable input signal LOW, the pull-up P-type MOSFETs are ON, the in/output of proposed precharge SA has HIGH(VDD) and it is precharge time. But, When is the enable input signal HIGH, the pull-up P-type MOSFETs are OFF, the output of proposed precharge type SA senses the input signal and it is evaluation time. The sizes of pull-up P-type MOSFETs and inverters play role in this circuit. As are the sizes of

pull-up P-type MOSFETs large, the output of this circuit does not change according to input signal. We are determined the suitable sizes of pull-up P-type MOSFETs. The output of precharge type SA changes when does input transit HIGH to LOW. Because requires the output of precharge type SA sensitivity to transition of input signal, the sizes of P-type MOSFETs of the first inverter larger than that of N-type MOSFETs. The high noise margin is wider than low in the first inverter for sensitive to input transition. The size of the second inverter is normal. The logic threshold voltage of the first inverter is 2.06V at 3.3V and of the second inverter is 1.65V at 3.3V. This means that the maximum voltage of bit line has about 2.06V.

3. Readout Simulation of 1T FeFET Memory

The 1T FeFET memory circuit is composed of 1T FeFET memory cells and precharge type SAs. The proposed structure of 1T FeFET has the isolated column common well lines. The column common well was electrically isolated from adjacent column common well in order to bit operation. A 1T FeFET memory cells are organized in a matrix types. Source and well lines of 1T FeTET memory cell are tied with. The sense amplifier circuits are connected bit lines, respectively. The 1T FeFET memory cells are connected parallel at one bit lines, so they are NOR type memory. The sense amplifier circuit determines the output of a NOR type 1T FeFET memory cell. The read operation of 1T FeFET makes use of a threshold voltage shift. The threshold voltage depends on the condition of each cell. The threshold voltages of programmed cells have less than of non-programmed cells. In this paper, the threshold voltage of programmed cell has 1.9V and of non-programmed cell has 2.9V. So, the read voltage of 1T FeFET memory cell is 2.5V. This means that the memory window of 1T FeFET memory cell requires more than 1V at least. When reading a programmed cell, the reading voltage applied to the gate of the 1T FeFET becomes larger than the threshold voltage. Therefore, the 1T FeFET is in the "on state" and current flows, for evaluation time. When reading a non-programmed cell, the reading voltage applied to the gate of the 1T FeFET becomes smaller than the threshold voltage. Therefore, the 1T FeFET is in the "off state" and current does not flow, for evaluation. In this way, we determine outputs of 1T FeFET memory cells as voltage sensing of each cell. So, The reference cell is not necessary compare with current sensing in a NOR type 1T FeFET memory. We made a readout circuit simulation for 4 by 4 1T FeFET.

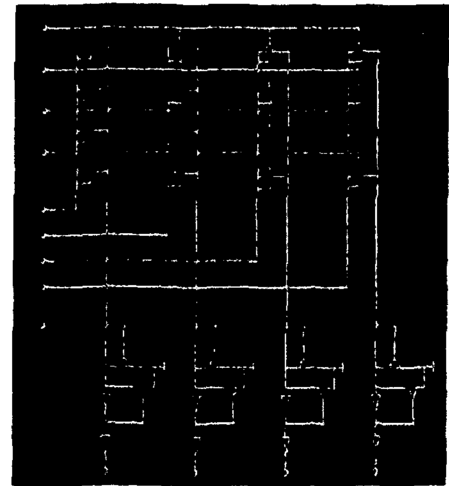

Fig. 2 Schematic of 4 by 4 1T FeFET memory circuit

In Fig. 2, the input signals are word lines of 4, source (well) lines of 4, respectively, and enable signal for precharge type SA. The precharge type SA is connected each bit line of 1T FeFET memory cell. The supply voltage is 3.3V and the read voltage is 2.5V. Fig. 3 shows the simulation results under condition precharge time are 90ns and evaluation time is 10ns with 900f bit line capacitance. Fig. 4 shows the simulation results under condition precharge time are 10ns and evaluation time is 90ns with 900f bit line capacitance. As shown Fig. 3 and 4, the proposed SA well operates in a NOR type 1T FeFET memory.

4. Conclusions

We design the precharge type SA design which is suitable for voltage sensing in the NOR type 1T FeFET memory read operation. The proposed SA can very well sense a bit

line voltage of the NOR type 1T FeFET memory cell at 3.3V@100ns.

5. References

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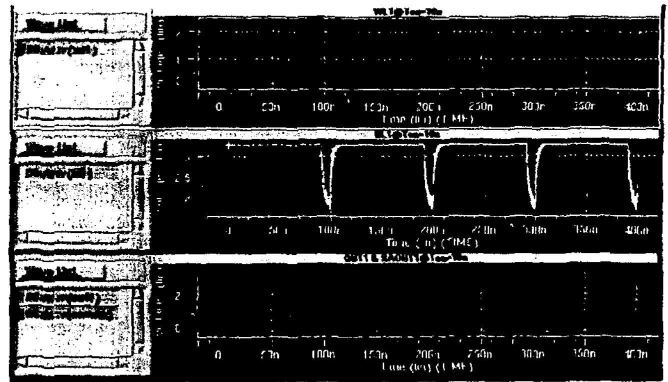

Fig. 3 Simulation Results of 1T FeFET Read Operation at 3.3V@100ns(precharge time is 10ns, evaluation time is 90ns)

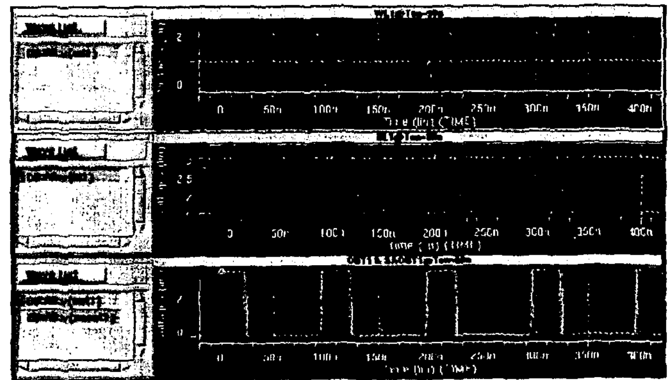

Fig. 4 Simulation Results of 1T FeFET Read Operation at 3.3V@100ns(precharge time is 90ns, evaluation time is 10ns)