Ternary Content Addressable Memory with Hamming Distance Search Functions

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Abstract: The flexibility of content addressable memory (CAM) can greatly be extended through the use of trits (ternary digits). Trits consist of binary logical values "0" and "1" with addition of "x" ("don't care"). The "don't care" is extremely useful for providing compact representation of sets of bit strings. In this paper, we propose a new ternary CAM with Hamming distance search functions. Each memory cell in the CAM consists of a pair of lambda diodes which can store trits, namely, a logical "0", "1" and "x" ("don't care"). The CAM can compare stored data and an input data in parallel, and find stored data with Hamming distance within a certain range ("near match"). Also, the interrogation characteristics of the ternary CAM are analyzed in detail. Furthermore, the results obtained these analyses are fully confirmed by simulation using the circuit analysis program HSPICE.

1. Introduction

Content addressable memory (CAM), especially full parellel CAM, provides a unique exclusive fast data-search function by accessing stored data by its content rather than its memory location indicated by an address. Such data-search capability is useful in many applications, including image pattern recognition, cache tag tables, artificial intelligence, packet switching in communication networks and data base accelerators [1-5]. Conventional CAM's implement the exact match operation, and all not exactly matching words are treated equally as nonmatching. That is to say, the outputs of the CAM's are the contents and/or the addresses of stored data that exactly match an input data. If an exact match word is not found, a no-match flag is asserted.

Recently, CAM's with Hamming distance search functions have been reported [6-8]. The CAM's can compare stored data and an input data in parallel, and find stored data with Hamming distance within a certain range ("near match"). The range of Hamming distance can be soft-programmed. Such data-search functions are extremely useful in a variety of image and speech processing and relational data base applications [9,10]. The conventional CAM's with Hamming distance search functions are composed of SRAM cells capable of storing two states (binary logical values "0" and "1"). The flexibility of CAM can greatly be extended through the use of trits (ternary digits). Trits consist of binary logical values "0" and "1" with addition of "x" ("don't care"). The "don't care" is extremely useful for providing compact representation of sets of bit strings [11,12].

In this paper, we propose a new ternary CAM with Hamming distance search functions. The CAM can store three states, namely, "0", "1" and "x". The ability to store the "don't care" state is useful in logical inferencing and pattern-matching applications [13]. Section 2 describes the circuit configuration of the proposed CAM. Furthermore, the interrogation characteristics of the CAM are analyzed in detail. In Section 3 , the results obtained from these analyses are fully confirmed by simulation using the circuit analysis program HSPICE. Finally, conclusions are given in Section 4.

2. Circuit configuration of the proposed CAM

2.1 CAM cell array

The proposed ternary CAM with Hamming distance search functions is shown in Fig. 1 (a). The CAM consists of three main parts, namely, CAM cell array, comparators and reference circuits. Also, a CAM cell is shown in Fig. 1 (b). The CAM cell comprises a pair of lambda diodes ($T_1 \sim T_4$) with load resistors (R_L), access transistors (T_5 and T_6) and interrogation transistors ($T_7 \sim T_{10}$) connected to a pull-up resistor (R_N). The CAM cell can store three states that correspond to the voltages at nodes N_L and N_R as shown in Table 1.

Each CAM cell is connected to a match line as shown in Fig. 1 (a). In interrogation operation, corresponding to the search data (input data), voltages as shown in Ta-

Table 1 Definitions of stored data.

N_R \ N_L	"L" Level	"H" Level
"L" Level	"x"	"1"
"H" Level	"0"	

Table 2 Definitions of search data.

search data \ bit line	B_L	B_R
"1"	"L" Level	"H" Level
"0"	"H" Level	"L" Level
"Mask"	"L" Level	"L" Level

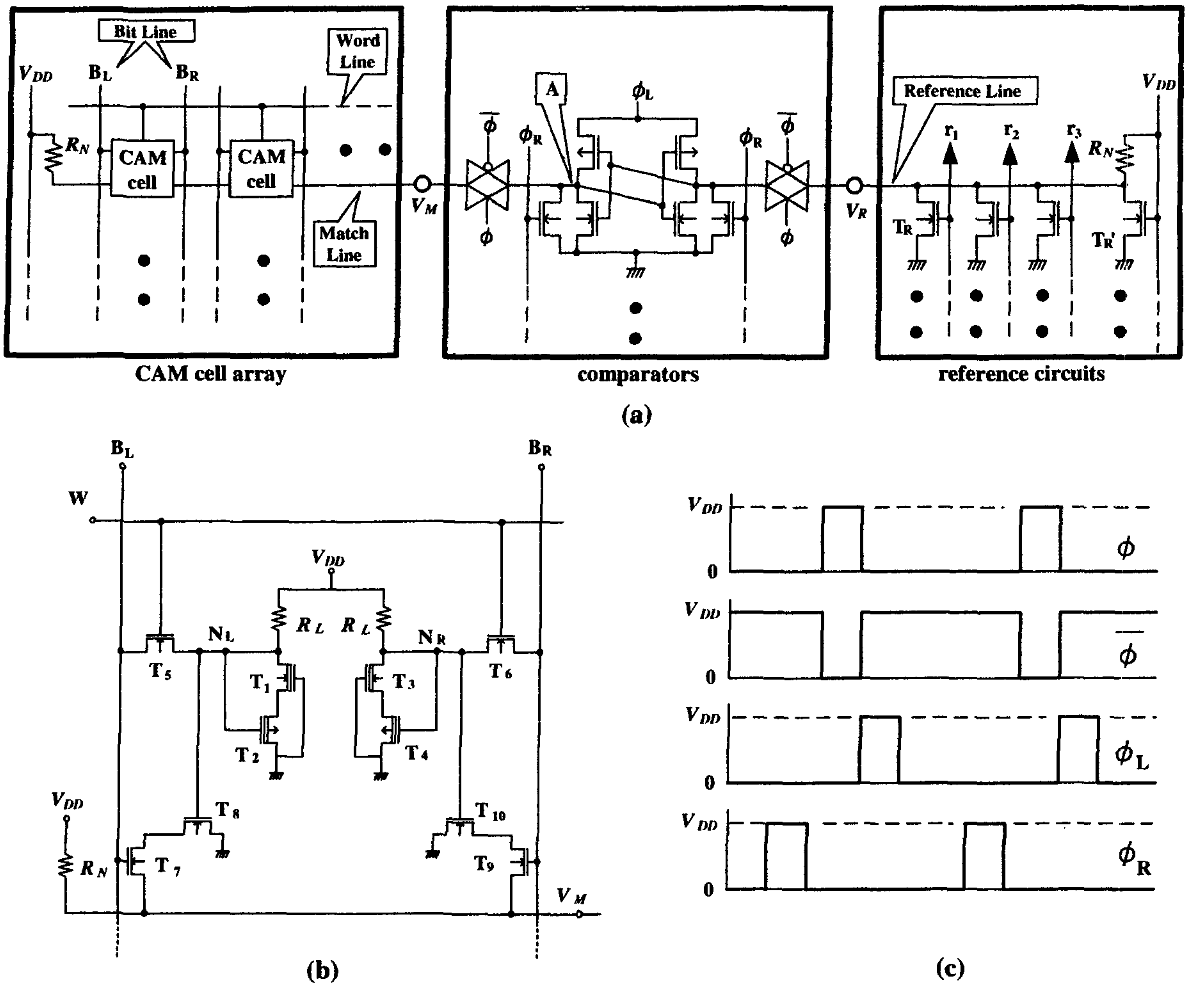

Fig. 1 Circuit configuration of the proposed CAM. (a) proposed CAM. (b) CAM cell. (c) clock signals.

ble 2 are supplied to bit lines B_L *and* B_R*, respectively.* Therefore, the match line normally remains at the high level (V_{DD} [V]) unless there is mismatch between the input data and stored data. On the other hand, if at least one unmatched bit between the input data and stored data is found, the match line voltage V_M is reduced from V_{DD}[V]. Assuming that T_8 and T_{10} in Fig. 1 (b) act like ideal switches, the match line voltage V_M is approximately given as follow:

$$V_M = V_{DD} \quad V_T + \frac{1}{k\beta_N R_N}$$

$$\sqrt{\left[V_{DD} \quad V_T + \frac{1}{k\beta_N R_N}\right]^2 \quad \frac{2V_{DD}}{k\beta_N R_N}}, \qquad (1)$$

$$\beta_N > \frac{2V_T}{(V_{DD} \quad V_T)^2 R_N},$$

where V_T and β_N are the threshold voltage and the channel conductance of T_7 and T_9, respectively. k is *the number of unmatched bits, namely,* Hamming distance between the input data and stored data.

2.2 Reference circuit

The reference circuit is to determine range of Hamming distance in the interrogation operation. That is to say, the circuit can fix the "acceptable" Hamming distance within a certain range by applying the reference signals r_1, r_2 and r_3 to gate terminals of T_R. For example, if r_1 is the high level (V_{DD} [V]) and others are the low level (0 [V]), this combination of the reference signals shows that the "acceptable" Hamming distance is "1". In the interrogation operation, to find stored data that the Hamming distance between the stored data and the input data is less than "2", the high level voltages are supplied to two terminals r_1 and r_2. Also, to set the Hamming distance "3", the high level voltages are applied to all terminals r_1, r_2 and r_3. Therefore, the reference line voltage V_R is given as follow:

Table 3 MOSFET Device Parameters

Symbol	Parameter name	nMOS	pMOS	Unit
V_{TO}	Zero-bias threshold voltage	±0.8	±0.8	V
N_A	Substrate doping	1.4×10^{17}	8.5×10^{16}	cm ^{3}
t_{ox}	Gate-oxide thickness	96	96	Å
L	Channel length	1.0	1.0	μm
W	Channel width	1 & 2 &20	4 & 8	μm
λ	Channel-length modulation	0.03	7.95	V ^{1}
ϕ_S	Surface inversion potential	0.70	0.70	V
μ_0	Low field bulk mobility	546.2	135.5	cm^2/V · s
γ	Body-effect parameter	0.59	0.46	$V^{1/2}$

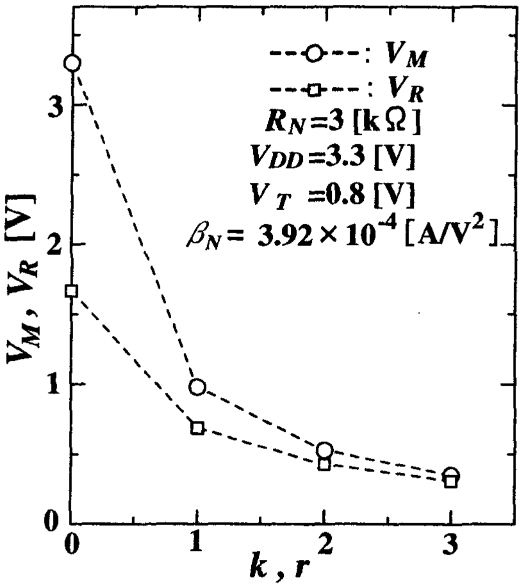

Fig. 2 Calculated results of V_M and V_R as function of k and r.

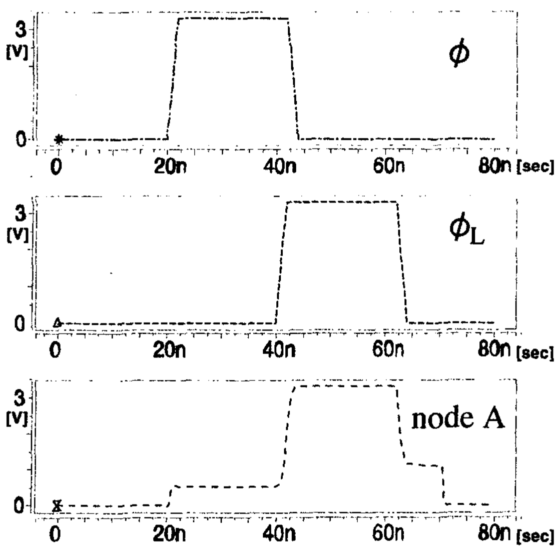

Fig. 3 Simulation waveforms. (a)clock signal ϕ. (b)clock signal ϕ_L. (c)voltage at node A.

$$V_R = V_{DD} \quad V_T + \frac{1}{(r+1/2)\beta_N R_N}$$

$$\sqrt{\left[V_{DD} \quad V_T + \frac{1}{(r+1/2)\beta_N R_N}\right]^2 \quad \frac{2V_{DD}}{(r+1/2)\beta_N R_N}}, \qquad (2)$$

$$\beta_N > \frac{4V_T}{(V_{DD} \quad V_T)^2 R_N},$$

where β_N is the channel conductance of T_R. The channel conductance of T'_R is $\beta_N/2$. And, r is the number of T_R that the high level voltages are applied to their gate terminals.

2.3 Comparator

The comparator compares the match line voltage V_M and the reference line voltage V_R. The comparator is driven by the four clock signals ϕ, $\bar{\phi}$, ϕ_L and ϕ_R as shown in Fig.1(c). V_M and V_R are given into the comparator when ϕ is the high level, and compared when ϕ_L is the high level. If V_M is higher than V_R, then the voltage at node A goes to V_{DD} [V]. On the other hand, if V_M is lower than V_R, then the voltage at node A goes to 0 [V]. Therefore, by detecting the voltage at node A, we can find stored data with Hamming distance within a certain range. During ϕ_R is the high level, the comparator is reset to prepare for the next interrogation operation.

3. HSPICE simulation

To verify the interrogation operation of the proposed CAM, we carried out computer simulation by using the circuit analysis program HSPICE. The HSPICE level 3 MOS model provided by MOSIS, for a typical 0.5 μm CMOS process, is used in all our simulation runs. Table 3 shows MOS device parameters used for our simulations. Fig. 2 shows calculated results of the match line voltage V_M and the reference line voltage V_R as a function of k and r. As can be seen in Fig. 2, when $k < r$ or $k = r$, the match line voltage V_M is higher than the reference line voltage V_R. On the other hand, when $k > r$,

V_M is lower than V_R. Therefore, by comparing V_M and V_R, we can find stored data with Hamming distance within a certain range.

Fig. 3 shows an example of simulation waveforms of a comparator operation. The simulation was performed under the condition of $k = r = 3$. This is the most severe condition for the comparator, because the voltage difference between V_M and V_R is the smallest. As can be seen in Fig. 3, when the clock signal ϕ goes to 3.3 [V], two transfer gates in Fig. 1(a) are closed. And then, V_M and V_R are given into the comparator. In the next cycle, when ϕ goes to 0 [V] and ϕ_L becomes 3.3 [V], the comparator carries out the comparison between V_M and V_R. In this simulation, V_M is higher than V_R because of $k = r = 3$ as shown in Fig. 2. Therefore, the voltage at node A rises to 3.3 [V] as shown in Fig. 3 (c). The simulation results show that k is smaller than r, or k is equal to r.

4. Conclusion

In this paper, we proposed a new ternary CAM with Hamming distance search functions. The CAM can store trits ("0", "1" and "x"), and find stored data with Hamming distance within a certain range. These features are very useful in a variety of image and speech processing and relational data base applications. Also, the interrogation characteristics of the CAM were analyzed in detail. The theoretical results had good coincidence with the simulation results using the circuit analysis program HSPICE.

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