Design and Implementation of OCQPSK/HPSK Modem using Digital Signal Processors for Software Defined Radio Applications

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Abstract : It is general opinion that the future mobile multimedia networks will use different standards and a prospective solution to this problem will be software defined radio (SDR) techniques. SDR provides the flexibility to support multiple air interfaces and signal processing functions at the same time. Especially, digital signal processors and FPGAs are widely used for implementation of these adaptive and flexible functions of a baseband modem for SDR applications. Also, it is known that the modulation schemes of OCQPSK (Orthogonal Complex QPSK) and HPSK (Hybrid PSK) are used for IMT-2000 services of cdma2000 and WCDMA, respectively. Thus, in this paper, we design and implement an OCQPSK / HPSK modem using a DSP chip of Texas Instrument's TMS320C6701. One modulation scheme is operated by adaptive selection between the two schemes and 5 physical traffic channels differentiated by orthogonal codes are implemented in one DSP chip and each channel has 1Mbps data rates and 8Mcps chip rates.

1. Introduction

With the growing attentions to new mobile multimedia applications including cellular video and audio services, wireless internet access and wireless LANs, there will be a demand for flexible mobile radio systems which provide multimode, multiband and multirole communication schemes. Because each mobile multimedia service has different frequency band assignments and modulation techniques, SDR has recently drawn much attention as a means to support flexible multimedia services. SDR is a technique which replaces hardware based devices by software controlled digital signal processors. Mobile terminals may receive information about appropriate transmission format from basestation.

This operation can be performed by downloading software programs. Therefore, SDR provides the possibility of adaptive changes of modulation or multiple access schemes. In the design of multimode SDR terminal, it is important to consider digital implementation of as much signal processing functions as possible attempting to extend the digital boundary further towards the antenna.

And also high performance digital signal processing devices like DSP, FPGAs and ASICs ensure increasing radio flexibility. On going technological advances are certain to reduce formerly required analog processing steps, like mixing, filtering to a minimum level. Many researches about SDR system design and implementation have used DSP chips for the purpose of computation and multimode operations due to its flexible programmability.

In this paper, we design and implement an OCQPSK/HPSK modem using TMS320C6701 DSP chip of Texas Instruments. Both of OCQPSK and HPSK modulation schemes are adopted in IMT-2000 services of cdma2000 and WCDMA, respectively, and each modulation method can be chosen by external selection in the implemented modem with SDR concepts. We design and implement 5 traffic channels differentiated by orthogonal codes into one DSP chip, and each channel has 1 Mbps data rates and 8 Mcps chip rates. The resulted modem can be used in a mobile multimedia service system as a software defined radio applications by adaptively taking the traffic channels up to 5 candidate traffic channels corresponding to the service type and required quality. In section 2, we describe the modulation schemes and in section 3, we explain the used DSP chip. The implementation results and conclusions are discussed in section 4 and 5, respectively.

2. OCQPSK/HPSK Modulation

In mobile communications, battery usage duration is one of the most important characteristics of the mobile station, and the efficiency of the terminal power amplifier is key to maximize battery life. Amplifiers are typically most efficient when they operate close to their saturation level. Therefore, mobile station amplifiers should ideally be designed so that the average power level of the signal is as close as possible to this saturation level. This works well for second generation mobile communication modulation schemes, such as OQPSK(Offset QPSK) or GMSK(Gaussian Minimum Shift Keying). OQPSK avoids symbol transitions through zero, which reduces the peak-to-average power ratio of the signal. GMSK is a constant amplitude modulation scheme, so peak-to-average power ratio is not a problem. For these formats, the headroom required in the amplifier to prevent compression of the signal and interference with the adjacent frequency channels is small. Thus, the amplifier can operate more efficiently. However, in third generation mobile communication systems, such as WCDMA(3GPP) and cdma2000(3GPP2), the mobile can transmit multiple channels at different amplitude levels. Modulation formats such as OQPSK or GMSK do not prevent zero-crossings for multiple channels and are no longer suitable. There is a need for a modulation format or a spreading technique that can accommodate multiple channels at different power levels while producing signals with low peak-to-average power ratios. The OCQPSK, also known as HPSK, has been proposed as the spreading technique for cdma2000 and WCDMA. The differences between them are just the spreading codes used. The block diagrams of these modulation schemes are shown in Fig. 1 and Fig. 2.
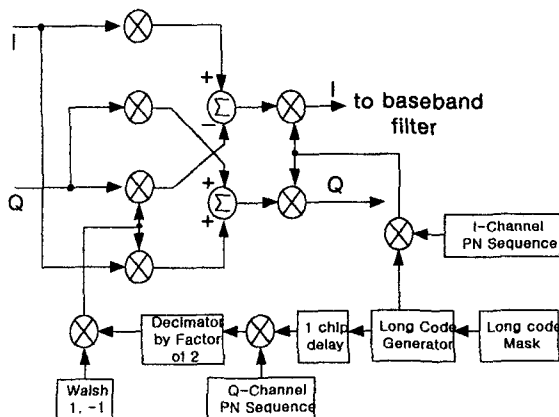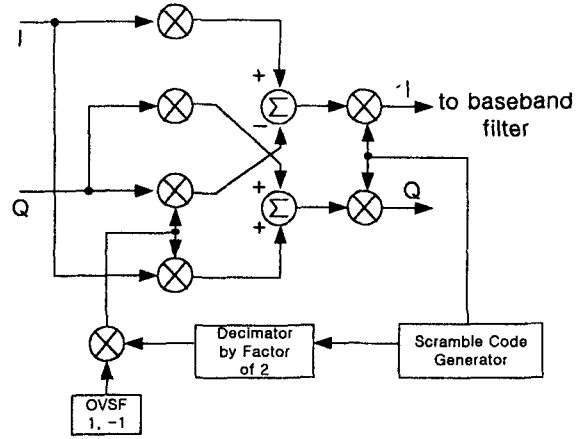

Fig. 2. Block diagram of HPSK modulation.

Basically, the structures of OCQPSK and HPSK modulator are same with different spreading codes. For example, Walsh code and OVSF(orthogonal variable spreading factor) code are used in the same position in each modulator. If we use notations of I_d, I_s, Q_d, and Q_s for I and Q channel data and spreading code, respectively, the resulting I and Q components can be described as follows:

$$
\begin{aligned}
I + jQ &= (I_d \bullet I_s - Q_d \bullet Q_s) \\
&\quad + j(I_d \bullet Q_s + Q_d \bullet I_s) \\
&= (I_d + jQ_d) \bullet (I_s + jQ_s) \\
&= A_d \bullet A_s \bullet \exp[j(\phi_d + \phi_s)]
\end{aligned}
\tag{1}
$$

where, A_d and $\exp[j\phi_d]$ are the amplitude and the phase of the $I_d + jQ_d$ signal, and A_s and $\exp[j\phi_s]$ are the amplitude and the phase of the $I_s + jQ_s$ signal.

3. TMS320C6701 DSP Chip

The DSP chip of TMS320C6701 of Texas Instruments is a high performance floating point DSP with 6 nsec instruction cycle time, 167 MHz clock rate and eight 32 bit instructions per cycle. The CPU core has eight highly independent functional units, that is, 4 ALUs for floating and fixed point, 2 ALUs for fixed point and 2 multipliers for floating and fixed point. Also 4 channel bootloading DMA controller, 16 bit host port interface(HPI) and 32 bit external memory interface(EMIF) are included. Fig. 5 is showing the block diagram of DSP structure.

This device contains several peripherals for communication with off-chip memory, co-processors and serial devices. EMIF is the interface between the CPU and external memory and provides all of the proper timing to access various types of memory.
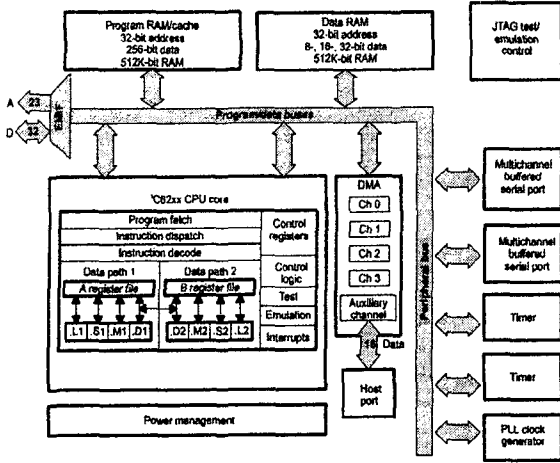

Fig. 1. Block diagram of OCQPSK modulation.

Fig. 3. Block diagram of DSP structure

4. Design and Implementation

4. 1. Designed Modem Structure

We designed and implemented a baseband modem which treats 5 traffic channels in a DSP chip as shown in Fig. 4 and 5. The orthogonal codes of either Walsh code or OVSF code can be used for channelization and Walsh code of 8th order is shown in Fig. 4 and 5 for simplicity. Each channel has 1Mbps data rates and 8 Mcps chip rates. Each data bit is multiplied by Walsh code and 1 Mhz data signal spectrum is spread to 8 MHz. If we use serial to parallel data converter before modulator, up to 5 Mbps data rates can be transmitted in about 10MHz bandwidth. In each traffic channel, a sequence of frames of 20msec length is transmitted, and each frame contains 20,000 data bits and 160,000 spreading chips.
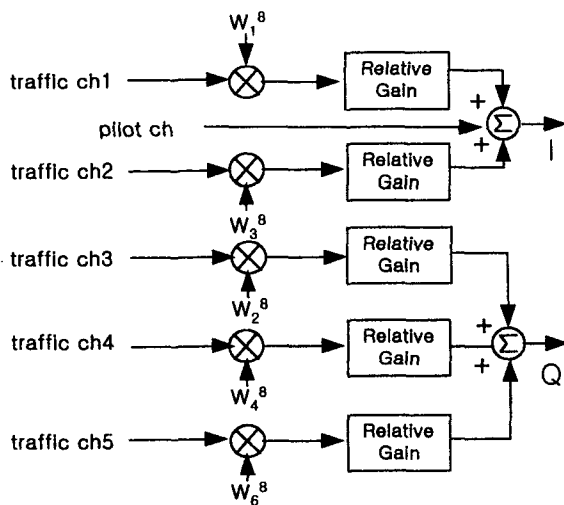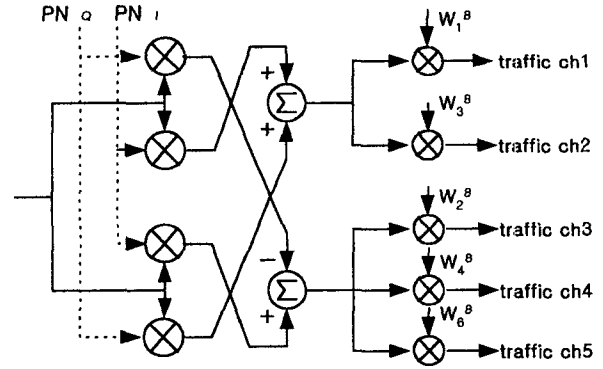

Fig. 4. Structure of designed modulator

Fig. 5. Structure of designed demodulator

4. 2. Implementation and Test Results

The programming for modem operation is performed using Code Composer Studio of Texas Instruments and targeted to an emulator of ADTM 6701 processor module of Aditec company as shown in Fig. 6.
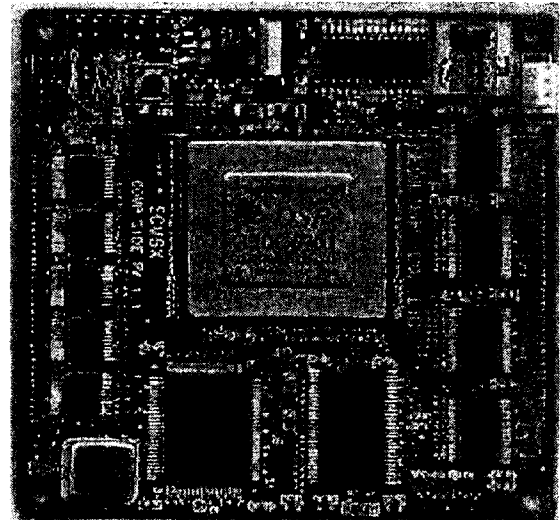

Fig. 6. Configuration of processor module

Fig. 7 shows the generated data before complex modulation from 5 channels. The information data bits are randomly generated in the DSP chip and saved in an extended memory for comparison with received data. One bit duration is measured as 1μsec through logic analyzer Agilent 1681A. The data bits are spread by 8-ary orthogonal symbol set and summed into I and Q channels as shown in Fig. 4. The structure of pseudo noise(PN) code generator of cdma2000 is different from that of WCDMA as described above. Thus, we programmed both PN code generators into a DSP chip and designed that one PN code generator between the two is chosen by external selection corresponding to the communication environment conditions and requirements.

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This concept is a part of software defined radio techniques for multimode systems. The mode selection can be performed by any method. Fig. 8 is the resulting spread data formats after complex spreading. The I and Q data lines are summed and then looped back to the demodulator. The received path is divided into two paths, that is, I and Q paths and these two paths are multiplied by PN codes and orthogonal codes as shown in Fig. 5. The resulting despread data is shown in Fig. 9 and there is no data error because of noiseless channel. From these results, it is known that the DSP codes for modulation and demodulation are programmed without errors and the implemented modem operates properly. And the modulation mode change is successfully achieved.
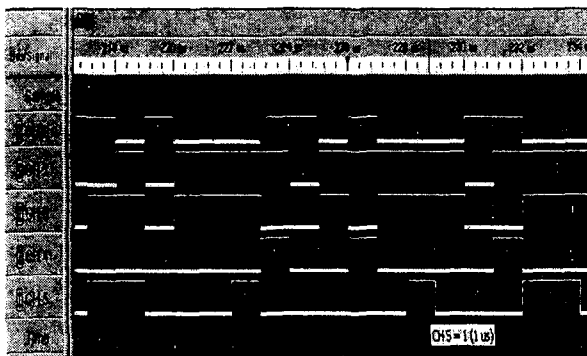

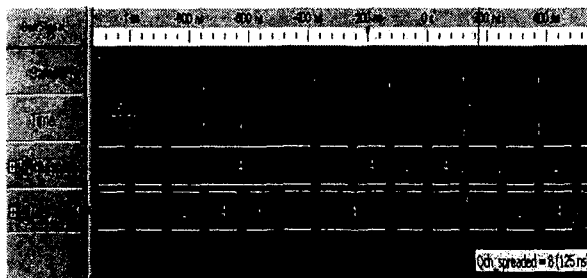Fig. 7. Data bit stream of 5 traffic channels
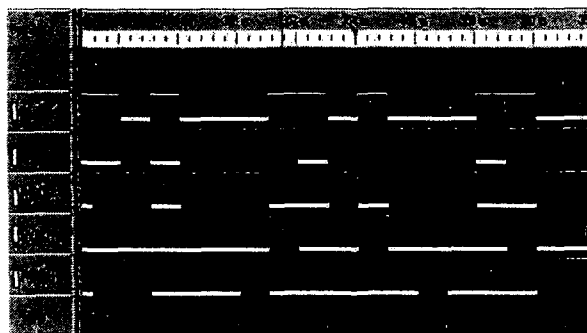

Fig. 8. I and Q signal after complex spreading

Fig. 9. Recovered data after despreading

5. Conclusions

In this paper, a baseband modem with OCQPSK /HPSK scheme is designed and implemented for SDR applications using TMS320C6701 DSP chip. These modulation schemes are adapted for IMT 2000 services, i. e., cdma2000 and WCDMA, respectively. Also, these two schemes have similar modulator structure except for spreading codes known as PN codes. Thus, we programmed both PN code generators into a DSP chip and designed that one PN code generator between the two is chosen by external selection corresponding to the communication conditions and requirements. And this concept is a part of software defined radio techniques with multimode operation. We designed the modem treating 5 traffic channels, and each channel has 1 Mbps data rates and 8 Mcps chip rates. From the measured data formats at transmitter and receiver, we can know that the DSP codes are successfully programmed and the modem operates properly.

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