Phase control of interleaved converters based on WTA

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Abstract: We consider interleaved buck converters using a switching rule based on Winner-Take-All (ab. WTA) nonlinearity. We clarify that this system exhibits various bifurcation phenomena. We also show that the switching phase of each converter is controlled by the WTA. Using a simple test circuit, ripple reduction and typical phenomena are verified in the laboratory.

1. Introduction

Parallel connection of switching converters [1]-[4] is an interesting technique from both practical and fundamental viewpoints. The interleaved converters have *current sharing* and *ripple reduction functions* [1]-[4]. The current sharing can provide lower voltages with higher current capabilities for microprocessors; and can improve reliability and fault tolerance [1][4]. The ripple reduction is convenient to reduce size and losses of the filtering stage; and also can decrease switching and conduction losses and EMI levels [1][5]. In order to realize such capabilities, phase control of each converter current is an important key.

In this paper, we consider interleaved buck converters using a switching rule based on WTA nonlinearity. The switching can realize flexible phase control and the system can generate various interesting synchronous phenomena. In order to analyze the dynamics, we simplify the system into a piecewise constant (ab. PWC) model. The PWC model has piecewise linear solution and is well suited for theoretical analysis. Using the PWC model, we consider various synchronous phenomena and ripple reduction property. Using a simple test circuit, ripple reduction and typical phenomena are verified in the laboratory.

2. Interleaved converters

Fig.1 shows the interleaved buck converters consisting of a power source V_1, N buck converters ($N \geq 2$) and a load. The j-th converter, $j \in \{1, \cdots, N\}$, includes a

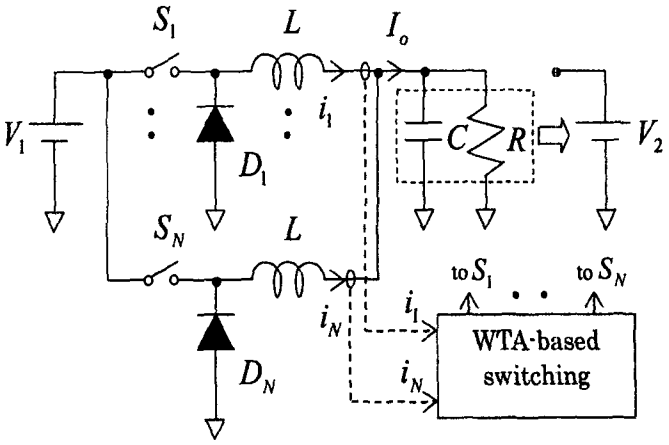

Figure 1. Interleaved buck converters.

current-controlled switch S_j, a linear inductor L_j and an ideal diode D_j.

Each converter current i_j is sampled periodically with period T. The converter having the minimum sampled current i_j becomes a winner at sampling time $t = nT$ ($n = 0, 1, 2, \ldots$). In order to define the switching rule, let the j-th converter be one of the three modes (see Fig.2).

State 1: S_j = ON, D_j = OFF and $0 < i_j < J$
State 2: S_j = OFF, D_j = ON and $0 < i_j < J$
State 3: S_j = OFF, D_j = OFF and $i_j = 0$

The converter that becomes a winner at sampling time $t = nT$ is changed into State 1. Let the j-th converter be State 1. In this case the converter is connected to the power source and the current i_j increases to a threshold J. At the moment when i_j reaches J, the converter is changed into State 2. Let the j-th converter be State 2. In this case the converter is connected to the load and the current i_j decreases to zero. If i_j reaches zero then the converter is changed from State 2 to State 3. Let the j-th converter be State 3. In this case the current

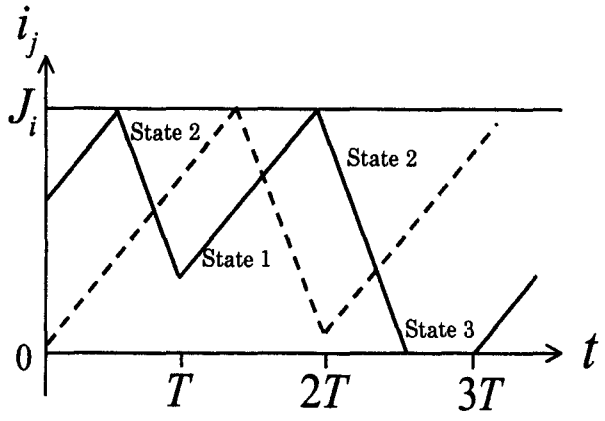

Figure 2. Switching rules.

i_j is zero and thus the converter is changed into State 1 at next sampling time $t = nT$. The switching rule is defined as the following:

$$\begin{array}{l} \text{State 1} \rightarrow \text{State 2 if } i_j = J \\ \text{State 2} \rightarrow \text{State 1 if } t = nT \text{ and } i_j = \text{min.} \\ \text{State 1} \rightarrow \text{State 3 if } i_j = 0 \\ \text{State 3} \rightarrow \text{State 1 if } t = nT \end{array} \quad (1)$$

For simplicity, we assume that the time constant RC is much greater than the sampling period T and the diode is ideal. In this case, referring to [5][6], we can replace the load with a constant voltage source V_2 and the circuit dynamics can be described by the following piecewise constant (ab. PWC) model:

$$L\frac{d}{dt}i_j = \begin{cases} V_1 - V_2 & \text{for State1} \\ -V_2 & \text{for State2} \\ 0 & \text{for State3} \end{cases} \quad (2)$$

where $j \in \{1, 2, \ldots, N\}$. The output current is given by $I_o \equiv \sum_{j=1}^{N} i_j$. This PWC model has piecewise linear solution and well suited for theoretical analysis. Using the dimensionless variables and parameters.

$$\tau = \frac{t}{T},\ x_j = \frac{i_j}{J},\ a = \frac{T}{LJ}(V_1 - V_2),\ b = \frac{T}{LJ}V_2. \quad (3)$$

Equations (1) and (2) are transformed into equations (4) and (5), respectively.

$$\frac{d}{d\tau}x_j = \begin{cases} a & \text{for State 1} \\ -b & \text{for State 2} \\ 0 & \text{for State 3} \end{cases} \quad (4)$$

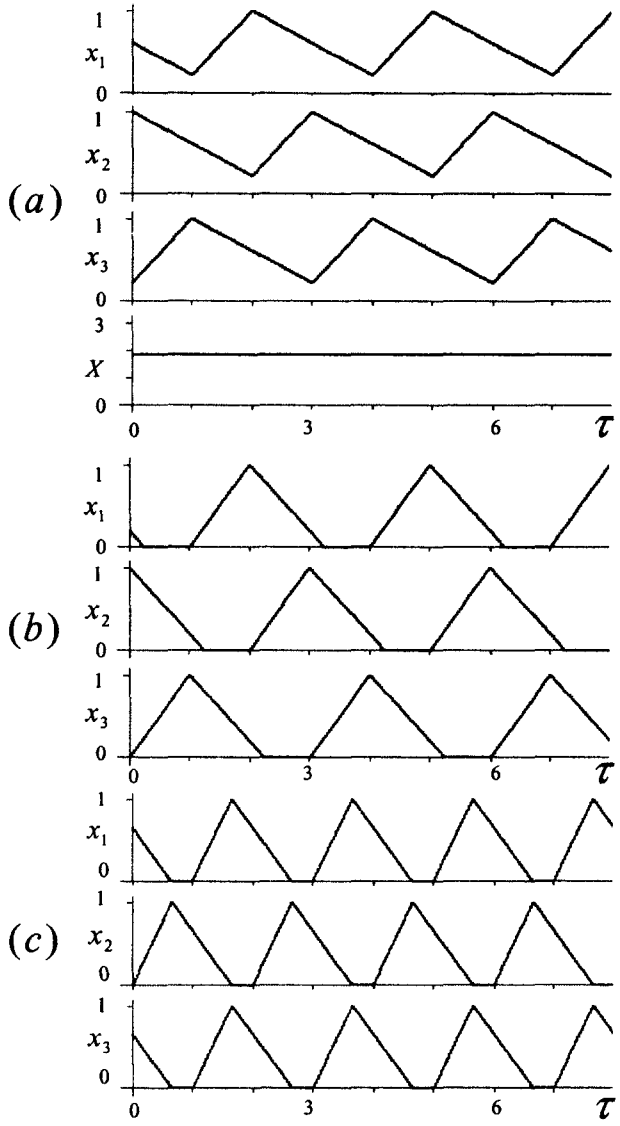

Figure 3. Typical synchronous phenomena ($N = 3$) (a) 3-SYN (CCM) for $(a, b) = (0.78, 0.38)$. (b) 3-SYN (DCM) for $(a, b) = (1.00, 0.80)$. (c) 2-OSYN for $(a, b) = (1.50, 1.00)$.

$$\begin{array}{l} \text{State 1} \rightarrow \text{State 2 if } x_j = 1 \\ \text{State 2} \rightarrow \text{State 1 if } \tau = n \text{ and } x_j = \text{min.} \\ \text{State 1} \rightarrow \text{State 3 if } x_j = 0 \\ \text{State 3} \rightarrow \text{State 1 if } \tau = n \end{array} \quad (5)$$

The dimensionless output current is given by $X(\tau) \equiv \sum_{i=1}^{N} x_j(\tau)$.

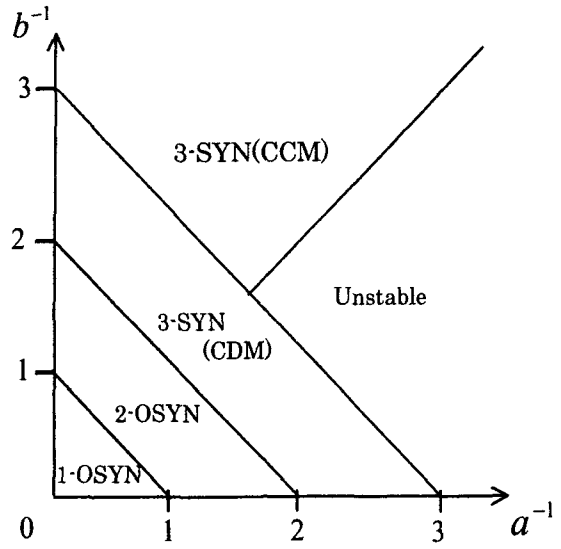

Figure 4. Parameters condition of each synchronous phenomenon ($N = 3$).

3. Typical phenomena

Here we define typical phenomena. The system is said to operate in a discontinuous conduction mode (ab. DCM) (continuous conduction mode (CCM)) if the system operates to (not to) include State 3. The system is said to exhibits N-phase synchronization (ab. N-SYN) if each converter current is periodic with period T_N and has phase difference $\frac{T_N}{N}$ to each other. The system is said to exhibits M-phase overlapping synchronization (ab. M-OSYN) where $M < N$ if the system exhibits M-SYN with overlapping. Fig.3 shows typical phenomena for $N = 3$. In Fig.3 (a) we can see that the WTA-based switching can distribute phases and the system exhibits 3-SYN with ripple reduction. The DCM may be inconvenient for the ripple reduction, however the system can exhibit interesting phenomena. Fig.3 (b) shows 3-SYN in CCM and Fig.3 (c) shows 2-OSYN having two winners at $\tau = 1$. We have clarified that the M-OSYN is possible only in the DCM. Using the PWC model, we have derived parameters condition for each phenomenon [6]. The results for $N = 3$ is shown in Fig.4. It should be noted that the condition is derived theoretically.

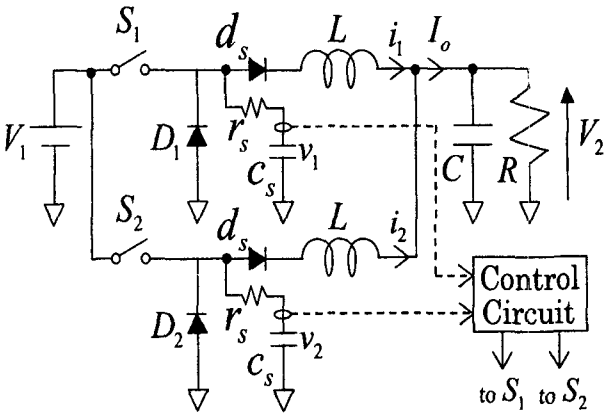

Figure 5. A simple test circuit ($N = 2$).

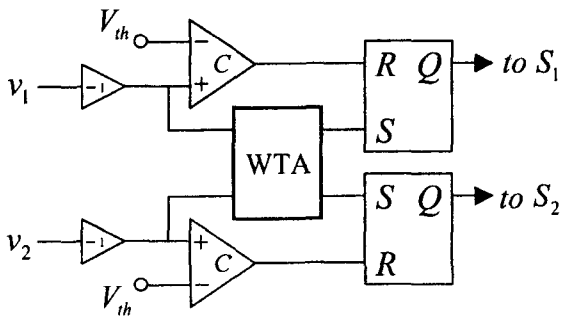

Figure 6. A control circuit ($N = 2$).

4. Experiments

As shown in Fig.5 we have designed a simple test circuit for $N = 2$. Fig.6 shows a control circuit that realizes WTA-based switching. In Fig.5, we have adopted "simple current sensing technique" [3]. Using the sensing technique, v_1 and v_2 can be used to estimate the inductor current i_1 and i_2, respectively. That the current from the load to $r_s c_s$ is prevented by the diode d_s. Note that d_s is not need for CCM. In Fig.6, these voltages are applied to set and reset terminals of the 2 flip-flops, respectively. The outputs of the flip-flops control switches S_1 and S_2 in Fig.5. Using this circuit, we have verified 2-SYN(CCM), 2-SYN(DCM) and 1-OSYN corresponding to (Fig.7 (a), (b) and (C)), respectively. The WTA circuit for $N = 2$ can be replaced with a comparator and two AND circuits. This simple test circuit is aimed at basic laboratory experiments and can be developed into the circuit for $N \geq 3$.

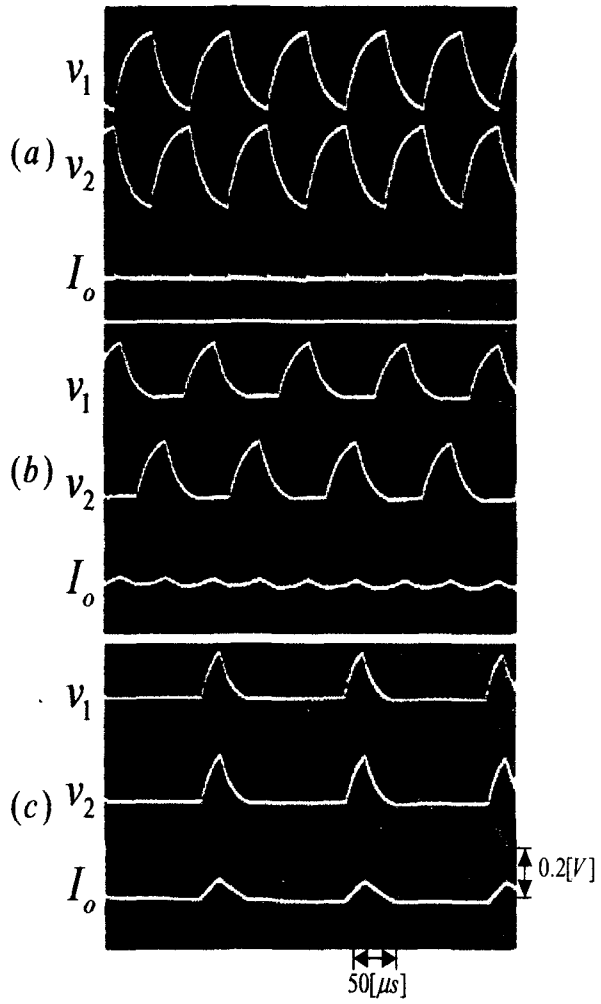

Figure 7. Observed typical wave forms (N=2) ($L \doteq 100[mH]$, $r_s \doteq 51[k\Omega]$, $c_s = 330[pF]$) (a) 2-SYN (CCM). $V_1 \doteq 3.2[V]$, $V_2 = 0.7[V]$, $V_{th} \doteq 3.0[V]$, $T \doteq 47.2[\mu s]$, $I_o \doteq 1.4[mA]$. (b) 2-SYN (DCM). $V_1 \doteq 2.2[V]$, $V_2 \doteq 16.0[mV]$, $V_{th} \doteq 1.9[V]$, $T \doteq 58.1[\mu s]$, $I_o \doteq 0.3[mA]$. (c) 1-OSYN. $V_1 \doteq 2.4[V]$, $V_2 \doteq 8.0[mV]$, $V_{th} \doteq 1.7[V]$, $T \doteq 158.7[\mu s]$, $I_o \doteq 0.1[mA]$.

5. Conclusion

We considered interleaved buck converters using a switching rule based on WTA nonlinearity. We also showed that the switching phase of each converter is controlled by the WTA. Using a simple test circuit, ripple reduction and typical phenomena are verified in the lavoratory. Future problems development of efficient control method for practical applications and design of the practical circuits.

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