The Design of a Multiplexer for Multiview Image Proceessing

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Abstract: In this paper, we defined necessary operations and functional blocks of a multiplexer for 3-D video systems and present our multiplexer design. We adopted the ITU-T's recommendation(H.222.0) to define the operations and functions of the multiplexer and explained the data structures and details of the design for multiview image processing.

The data structure of TS(Transport Stream) and PES (Packetized Elementary Stream) in ITU-T Recommendation H.222.0 does not fit our multiview image processing system, because this recommendation is for wide scope of transmission of non-telephone signals. Therefore, we modified these TS and PES stream structures. The TS is modified to DSS(3D System Stream) and PES is modified to SPDU(DSS Program Data Unit). We constructed the multiplexer through these modified DSS and SPDU. The number of multiview image channels is nine, and the image class employed is MPEG-2 SD(Standard Definition) level which requires a bandwidth of 2~6 Mbps. The required clock speed should be faster than 54(= 6 × 9)MHz which is the outer interface clock speed. The inside part of the multiplexer requires a clock speed of only 1/8 of 54MHz, since the inside part of the multiplexer operates by the unit of byte. we used ALTERA Quartus II and the FPGA verification for the simulation.

1. Introduction

While demands for high-quality picture increases gradually, United States of America began HDTV's commercial broadcast in 1998, popularization of regular high-quality reflex was begun. As for Korean digital broadcasting policy, Korea began capital region DTV broadcasting before World Cup 2002 game. Accordingly, because 2-D image used on ground wave TV now, we can assuming 2-D's HD (High Definition) maturity in service. Accordingly, we interest in three-dimensional picture augmented gradually now. For these reason, three-dimensional terminal technology have needed third dimension display unit and three-dimensional image processing description as element technology, and this technology include actual feeling awareness and actual feeling embodiment technology. The multiview image processing technology is conformed to multiview display unit as kind of third dimension image processing technology. The multiview image processing technology contains information, compression of multiview video signal, reconstitution, composition, and image processing technology about acquired at the same time in nine cameras. The number of realization of Multiview image processing is 16. We cannot realize in real time in current communication network. Middle image composition technology is being studied lower bandwidth in former part. If we use it, we can compose middle image using nine images. We can reduce the required bandwidth by half level because we can compose images of 16 visual points in nine images. But, the multiplexer must deliver by one bit stream and requires faster speed than present system because we must send nine channels of image outputs at the same time. We designed a multiplexer which satisfies all these necessity.

2. Structure of Multiplexer for Multiview

We altered the rule regarding the packet structure that is used in multiview (ITU-T H.222.0) [1]. The PES packet rules were modified systems changed slightly and renaming SPDU (System Program Data Unit). Figure 1 shows the modified SPDU packet. We will now explain the differences between the SPDU and PES packet. Multi-view information flag indicates information about multi-view video ES (Element Stream)'s reference that is included to SPDU and display information about frame index. Master or slave flag presents whether SPDU have present reference packet ID is object or subject. Middle image displays new image composing both of images. So, We need reference between images. The reference packet ID presents SPDU's identification which becomes a reference. The other values are agreed with contents of rule.

We must send a 3-D data stream based on 2-D format of MPEG-2. TS packet used for transmission has a little modification. This packet is named as DSS (3-D System Stream). This packet's structure is shown at figure 2. Differences are as following. TS packet's OPCR flag, splicing point flag, transport private data flag and adaptation field extension flag be set as 0. Because 3-D video is a part, which is no

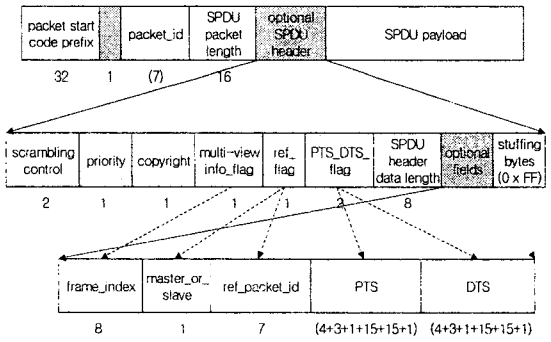

Figure 1. SPDU Packet Syntax

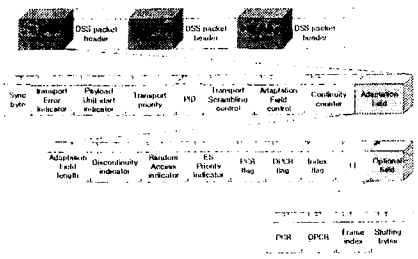

Figure 2. DSS Packet Syntax

realized in present, this flags are not used. Unemployed data informs that there is no data filling flag by zero. Then, because data not used when the demultiplexer treats header. Display index information of frame of video data exists in present DSS packet. Frame index field is a content that is not in rule and SPDU is defined in this research. Frame index counted circularly to 0 ~ 255 being value that is transmitted from each video encoder. There is PSI for acquired data transmission of 9 visual points, there is some alteration. PSI (Program Specific Information) is table that has information about program that is composed DSS stream. PAT (Program Association Table), PSI is classified PMT (Program Map Table), NIT (Network Information Table), CAT (Conditional Access Table). NIT and CAT are not embodied and PAT, PMT are used changed.

3. Multiplexer

The multiplexer block is acquired for nine videos by 188bytes unit that makes and sends stream information that putting each ES in one DSS stream. In this paragraph will explain the functions of several blocks are included to multiplexer.

3.1 Bandwidth

If we examine whole block construction, each nine stream receives data stream from each Video Encoder. Because PAT, PMT and NULL part are necessary packet information in DSS header creation are payload that create Section in interior. PAT, PMT and NULL do not have input stream. Design pattern of SPDU and DSS Header are similar. Outside input is PTS EN, DTS EN, PCR EN value that is each one bit enables signal value, and stream of one of nine streams defined by eight bits, one byte. Bandwidth between SPDU and DSS is 12 bytes. One of SPDU consists of one byte input stream and input pin of three enable signal. We designed state machine in SPDU module, it makes decrease wire and then we can implement SPDU by binding each block. Figure 3 shows whole structure.

3.2 SPDU header creation

The SPDU packet is consisted of header and payload that is input stream. The Header is consisted of basis header and addition header that always attached. Addition header part attached what kind of payload about information and other information. About one AU must create one header. Input cost is PCR_EN signal, PTS, DTS enable signal that is stream and one bit that enter by one header unit. PCR value receives Clock of 54MHz, and trigger in 1/600 in 10 bit

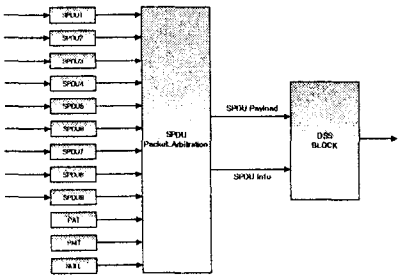

Figure 3. Whole Structure of Multiplexer

counter in interior from video encoder enable signal. In 1/600 in 33 bit counter receiving this signal triggered do. 33 bit counter values are amounts to PTS and DTS value. PTS and DTS are attached on SPDU header if receive enable signal of each one bit in video encoder (figure 4).

Figure 5 shows one of 9 SPDU header creation. SPDU mux is received enable signal from header. Beside that mux pass the payload.

3.3 SPDU Buffer & Buffer Controller

originally SPDU buffer must store and handle all of AU of one, but SPDU check start code and end code to diminish buffer size and SPDU Packet length value set by 0. If code stream that inform AU's beginning to buffer enters, Buffer controller reads this and remits enable value in SPDU header creation. Header creation charging enable values by interior counter create and send. Generation methods of nine SPDUs are similar with each others. For example about SPDU first, SPDU second, SPDU third, second gets into middle stream. Fourth-fifth-sixth SPDU and seventh-eighth-nineth SPDU are similar. AU is Video stream unit and AU has three Start code are video sequence start code, group of picture, picture start code and its principle is same

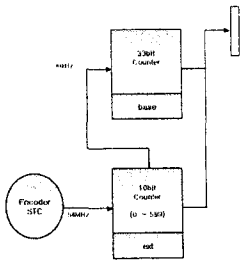

Figure 4. PCR Counter & PTS/DTS Counter

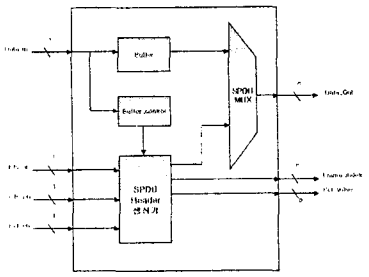

Figure 5. SPDU Interior Structure

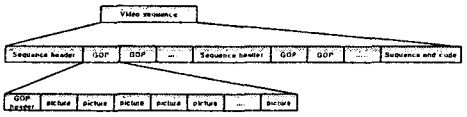

Figure 6. AU

with figure 6. Five kinds of start codes and end codes are mixed.

① Video sequence start code - picture start code
② Picture start code - picture start code
③ Picture start code - GOP start code
④ GOP start code - picture start code
⑤ Picture start code - video sequence start code

3.4 PAT Section

PAT includes PMT's PID that have PID of DSS packet of video, audio, and PCR compose program number and the program as table display information about program included inside DSS packet that is transmitted present. This research is defined only one program about nine streams. So, program ID is only one in PAT and PAT's loop is only one. While PAT Section's creation holds value as SPDU header creation, PAT is passed output by state value.

3.5 PMT Section

PMT about one program nine stream ID and PCR to send information stream ID values of nine stream public opinion one define though send because PCR value inserts in appointment stream in DSS appointment stream by user one select (Fifth SPDU selection). Because PAT and other point is not one program and ID value about nine streams is included, each ID of nine streams comes to loop. This time, user defines ID value. Section's creation with SPDU header creation similarly value preserve (register use) or value is passed by output by State value while change. PAT and PMT value are designed for pass to the DSS by every 0.3 seconds.

3.6 CRC32

PAT, PMT acquires CRC32(32bits) for error check. CRC32 is applied and designed as H.222.0's recommendation. CRC32 is a value that makes 32 registers value set by zero. Block algorithm is shown with figure 9. If CRC32 receives value, CRC32 do Exclusive-or and the result is stored to

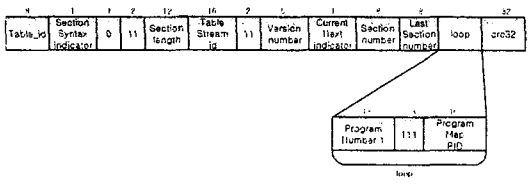

Figure 7. PAT Section

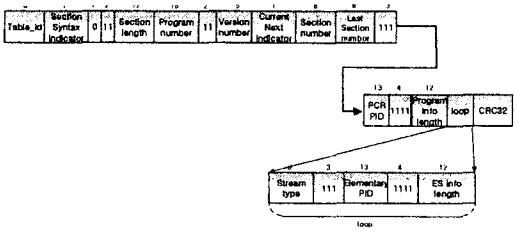

Figure 8. PMT Section

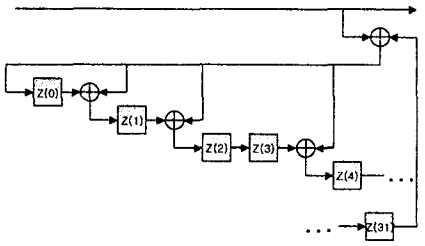

Figure 9. CRC32

each register. In the case of CRC32 of PAT, all bits of PAT section pass CRC32 step. All values are passed CRC32 and CRC32 value attaches PAT Section. PMT section acts by form like PAT.

3.7 Packet Arbitration

Nine Packet Arbitration's stream and PAT, PMT and NULL are 12 Payloads to pass DSS, and remainder must wait for an opportunity 11 intervals that one stream is processed. We need buffer controller, and also input clock of the buffer of and output clock must demand. DSS block should be fast 12 times than 12 inputs from SPDU. Actuality design did so. PAT, PMT and Null packet(fill by one) Is payload, too. But Null packet is created inside of DSS block. Values is created in each SPDU are stored to second SPDU step. if second SPDU steps buffer is fill with stream, second SPDU step propagate enable value to arbitration controller. Arbitration controller only control stream which is received enable signal from SPDU block until selected one of SPDU stream are send. (Figure 10)

3.8 DSS Header Creation

Creation of DSS header is simpler than SPDU header. Inside of DSS is operated by eight bits. DSS clock must slower than DSS output because go out by one bit in output. Also, DSS must calculate empty part to be filled with stuffing bytes (fill by one) because header size is variable. Because PCR value is included to specify SPDU stream (fifth SPDU). If fifth SPDU is received, PCR value is operated. Although PCR value is optional field value, the weight of occupation in header is high and fifth SPDU also becomes critical path. If PAT, PMT and end part of SPDU is payload, payloads are smaller than DSS payload size. DSS header made remainder part can analyze in demultiplex. We must insert stuffing byte between header and payload. Figure 11 shows interior of DSS block. Basis structure of frame is similar with SPDU block. Other points need some value,

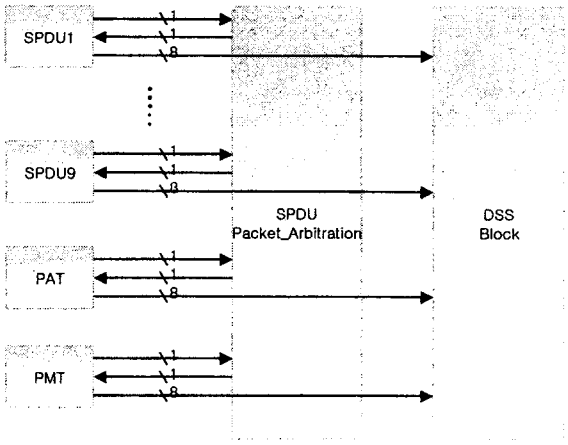

Figure 10. Packet Arbitration

before header is created (PCR, frame index, continuity counter value). Also, the DSS interior clock should be faster than SPDU interior clock because DSS must create header whenever DSS send by 188 bytes unit. Continuity counter part put on exterior of DSS, because we considered Quartus II [2] special quality. Transmission bandwidth of block interior did by one byte.

3.9 Clock of multiplexer

The working speed of the multiplexer SD level image was decided by Compression algorithm's improvement the speed by 2 ~ 6 Mbps. Therefore, the speed is embodied nine videos become 9 (channels) × 6 (max. bit rate) = 54 Mbps finally, system clock became 54MHz. But, DSS interior designed to act by 54 / 8 = 6.75 MHz acting with the speed of 1/8 of output because is displayed by one bit created by one byte unit in interior. The output of multiplexer interface part acts by 54MHz and the multiplexer interior part acts by 6.75 MHz. But, each SPDU input Clock is 27 MHz. If we design interior bandwidth by 1 byte, 11 SPDUs wait for DSS treat one SPDU stream. transmission is impossible. Because the multiplexer operating by one byte when create header in SPDU interior, first SPDU step is achieved by one byte and 12 register put in second SPDU steps. The 12 registers is placed front and behind buffer(FIFO). We use bandwidth by 12 byte to be passed to the DSS. Owing to we use 24 registers in second SPDU steps, we solved interior clock problem. Inside of DSS acts by one byte.

4. Result

The designed multiplexer units is composed of multiplexer unit, UART LOGIC(RX unit, TX unit) and FIFO unit. Function of the multiplexer was verified by using the Quartus II tool for FPGA design and verification, and the verified HDL model was synthesized using Samsung Electronics 0.35 micron standard cell library. The results show that operation condition of 3.3V, 25℃ and its logic elements is 8,245 except memory block.

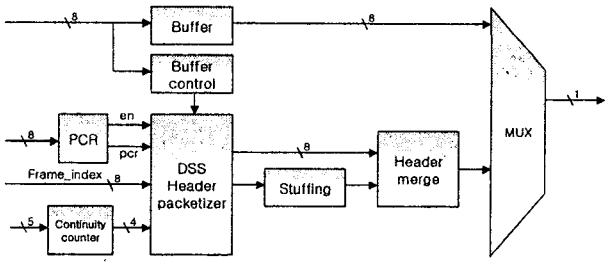

Figure 11. DSS Interior

References

[1] ITU-T 1996, "ITU-T H.222.0(07/95) transmission of non-telephone signals", 1995

[2] KETI (Korea Electronics Technology Institute), "SD image Composition/Compression/save/refreshing and video chipset design technology next generation New Technology development work 16 visual points", 2000

[3] ALTERA FPGA design tool and environment, IDEC teaching material , 2002.

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[5] Donald E. Thomas, Philip Moorby, "The Verilog Hardware Description Language," 1991.