A Simple Current-Mode Analog Multiplier-Divider Circuit Using OTAs

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Abstract: An analog multiplier-divider circuit that realized through the use of OTAs, which does not require external passive circuit elements and temperature compensated, is proposed in this paper. Since the scheme is realized in such a way that employs only OTA as a standard cell, the circuit is simple and can be easily constructed from commercially available IC. The circuit bandwidth is wide and close to the transistor f_T. Simulation results that demonstrate the performances of the multiplier-divider circuit are included.

1. Introduction

Analog multipliers and dividers are important nonlinear building blocks that have found useful in a wide range of applications, such as telecommunication, control, instrumentation and signal processing. At present, because of the main featuring of wider bandwidth, greater linearity, wider dynamic range and simple circuitry compared with their voltage-mode counterparts, current-mode circuits have been received growing interest in analog signal processing circuits. Many techniques to design current-mode analog multiplier-divider circuits have been presented in the literature [1-3]. Recently, a multiplier-divider circuit using only two second-generation current-controlled current-conveyors (CCCIIs) has been presented, where no resistors, no capacitors and no MOS transistors are required by such a realization scheme [4].

It is well accepted that OTA is a useful circuit building block in the design of analog circuits. It has been employed in the realization of active network elements, such as filters, oscillators, instrumentation amplifiers and gyrators. The OTA is a commercially available, low cost device that incorporates all the attractive features of an operational amplifier (OA). Since OTA is a programmable device and has only a single high-impedance node, this makes the OTA an attractive device for high frequency and programmable basic building block [5,6]. Therefore, the implementation of analog circuits in such a way that employs only OTA as a standard cells will not only be easily constructed from readily available cells, but also significantly simplified the design and layout. A circuit technique to employ OTAs to implement analog multiplier has been presented [7]. However, the circuit is voltage-mode circuit and only multiplication function is implemented. In this paper, a current-mode temperature compensated multiplier-divider circuit using only OTAs as active circuit elements has been presented, where no passive elements are required by this realization scheme. PSPICE simulation results will be used to demonstrate the performance of the proposed scheme.

2. Basic principle

The schematic diagram of the proposed current multiplier-divider circuit using OTAs is shows in Fig. 1. The input signal current i_{in1} is injected into the operational transconductance amplifier OTA1, which is connected as a grounded resistor. The voltage across the OTA1 is then used as the input voltage for the OTA2 and OTA3. The input signal current i_{in2} is added with the bias current I_{B2} of the OTA2. If g_{m1}, g_{m2} and g_{m3} are the transconductance gains of the OTA1, OTA2 and OTA3, respectively; then, from routine circuit analysis, the output currents I_{O2} and I_{O3} of the OTA2 and OTA3, respectively, can be written as

$$I_{o2} = \frac{g_{m2}}{g_{m1}} i_{in1} = \frac{(I_{B2} + i_{in2})}{I_{B1}} i_{in1} \tag{1}$$

and

$$I_{o3} = -\frac{g_{m3}}{g_{m1}} i_{in1} = -\frac{(I_{B3})}{I_{B1}} i_{in1} \tag{2}$$

where $g_{m1} = I_{B1}/2V_T$, $g_{m2} = (I_{B2}+i_{in2})/2V_T$ and $g_{m3} = I_{B3}/2V_T$ and V_T is the thermal voltage.
If we set $I_{B2} = I_{B3} = I_B$, the output current I_{OUT} of the circuit, that is the summation of the currents I_{O2} and I_{O3}, can now be given by

$$I_{out} = I_{o2} + I_{o3} = \frac{i_{in1} i_{in2}}{I_{B1}} \tag{3}$$

which is in the form of a current-mode analog multiplication-division function. The circuit performs as a four-quadrant multiplier if i_{in1} and i_{in2} are the input signals, while it performs as a divider circuit if i_{in1} (or i_{in2}) and I_{B1} are the input signals. It should be noted that, since it is the ratio of OTAs transconductance gain, the output current I_{out} is less sensitive to temperature.

The major factors that contribute to the error and non-linearity in the circuit can be classified as follows. The first factor is due to the offset current at the output port of the OTA1. From (3), if I_{os} is the offset current, the output current I_{out} can be rewritten as

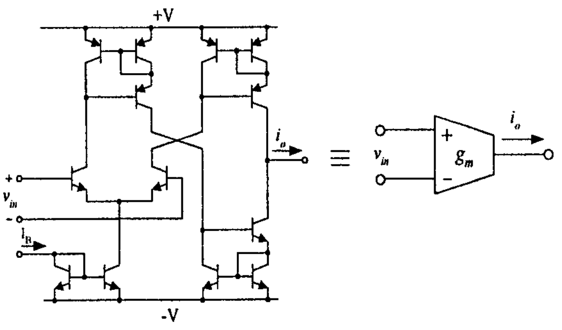

Fig. 1 The schematic diagram of the OTA.

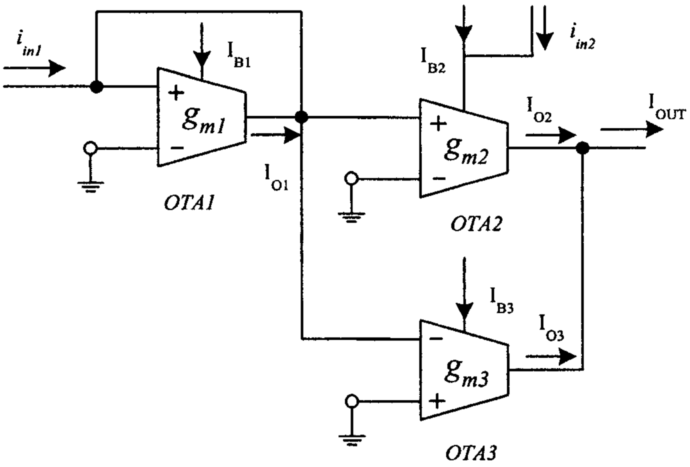

Fig. 2 The proposed current-mode multiplier-divider circuit using OTAs.

$$I_{out}=\frac{(i_{in1}+I_{os})i_{in2}}{I_{B1}} \qquad (4)$$

We can see that, particularly for the peak value $|i_{in1}| \leq I_{os}$, the multiplication for the positive peak and the negative peak of i_{in1} will not be equal. Thus the signal peak value should be selected such that $|i_{in1}| \geq I_{os}$. While the offset currents at the output ports of the OTA2 and OTA3 are not contribute to the multiplication error, but will produce a DC current at the output of the circuit. The second factor affecting the non-linearity of the circuit is due to the limited linear range of the input stage of the OTA2 and OTA3. For a bipolar-based OTA, where the input stage is a conventional differential pair, the input differential voltages for linear operation are restricted to be less than 26 mV. Since $1/g_{m1}=2V_T/I_{B1}$, this restricted linear range can be improve by increasing I_{B1}.

3. Simulation results

As shown in Fig.1, in this work an OTA that realized in bipolar transistor technology will be employed as active circuit elements. Its transconductance gain ($gm=V_T/2I_B$) can be tune by the DC bias current (I_B). The performance of the proposed multiplier-divider circuit of Fig.1 was verified through the use of SPICE simulation results. All the OTA was simulated by using the bipolar transistor parameters of the 2N3904 and 2N3906 for the NPN and PNP transistors, respectively. The transistors f_T were 186 MHz. The circuit of Fig. 2 was simulated using the PSPICE circuit simulation program. The multiplier function was tested by multiplying two sinusoidal signals. The result obtained are shown in Fig. 3 for i_{in1} = 0.5sin(2π 1000t) mA, i_{in2} = 0.5sin(2π3000t) mA and I_{B1} = 1mA. Since the DC offset current will distort the output signal, a DC current of about 6μA was injected at the output of the OTA1 to adjust the offset to be less than ±0.1μA. Similarly, a DC current of about 4μA was used to keep the offset current at the output of the circuit to be less than ± 0.1μA. The power supply voltages were set to Vcc = 10V and VEE = -10V.

The divider function was tested by inverting a triangular signal. The results obtained are show in Fig. 4 . Fig.4 show the simulated transient response of the circuit that function as a divider. The output current I_{OUT}, which in this case is an inverting function of a triangular signal, was simulated for i_{in1} = 100μA, i_{in2} = 300μA, and I_{B1} is a 500Hz triangular wave with amplitude of 100μA and DC component of equal to 200μA.

Fig.5 shows the simulated DC transfer characteristics for the multiplier function, where the bias currents were set to $I_{B1}=I_{B2}=I_{B3}$ = 1mA. The figure shows the plot of the output current I_{OUT} against the input signal current i_{in1} from −1mA to 1mA and the input signal current i_{in2} from −1mA to 1mA with 0.5mA per step. The simulation and calculated data are agree very well over the ±0.8mA input range with an error of less than 0.1%. We can see large non-linearity for i_{in1} close 1mA this is due to that the voltage across the OTA1 is closed to the limited linear range. Fig.5 show the simulated transient response of the circuit that function as a divider. The output current I_{OUT}, which in this case is an inverting function of a triangular signal, was simulated for i_{in1} = 100μA, i_{in2} = 300μA, and I_{B1} is a 500Hz triangular wave with amplitude of 100μA and DC component of equal to 200μA. Fig.6 shows the simulated frequency response of the circuit from the input i_{in1} to the output, with i_{in2} = 100μA and I_{B1} = 1mA. The response indicates that the circuit −3dB bandwidth is about 162 MHz that is close to the transistor f_T. The total harmonic distortion (THD) against input current, for the case that the input signal i_{in2} is a dc current, i_{in2} = 100μA and the input signal current i_{in1} = 0.1sin(2π10000t) mA, is about 0.24% . On the other hand, when the input current i_{in1} is dc current, i_{in1} = 100μA, and the signal current i_{in2} = 0.1sin(2π10000t) mA, the THD is about 0.39%.

Fig.7. Shows the simulation result of the output current (I_{OUT}) due to the change of temperature for operating temperature variations from 0 °C to 100 °C. We set the input signal currents i_{in1} and i_{in2} as dc currents, where $i_{in1} = 1000\mu A$ and $i_{in2} = 60\mu A$, where $I_{OUT} = 60\mu A$. From the figure, the output current varies only from $59.62\mu A$ to $61.38\mu A$, for the temperature 0 °C to 100 °C respectively. This simulation result shows that the temperature dependence of transconductance gains g_{m1}, g_{m2} and g_{m3} of the bipolar OTAs are compensated.

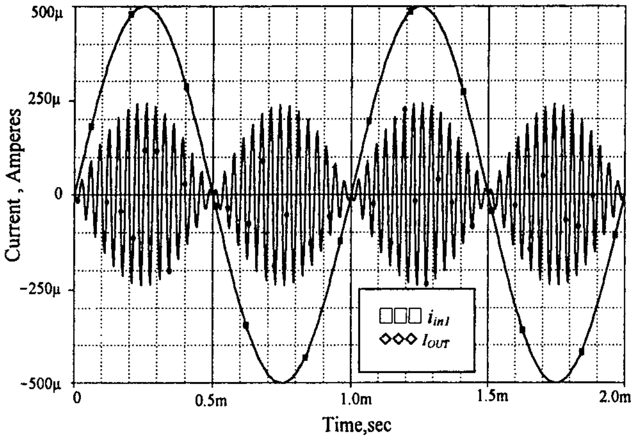

Fig. 3 Simulated transient response for the multiplier function.

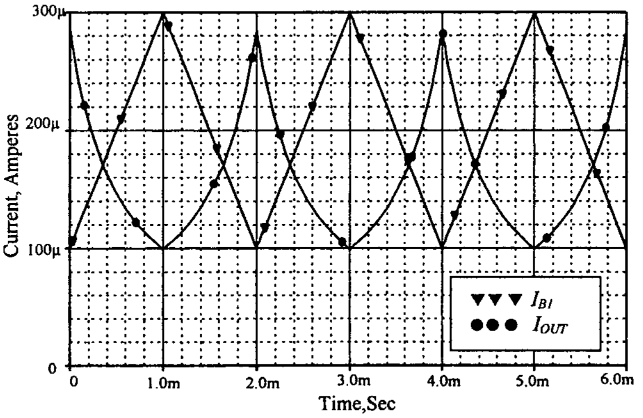

Fig. 4 Simulated transient response for the divider function.

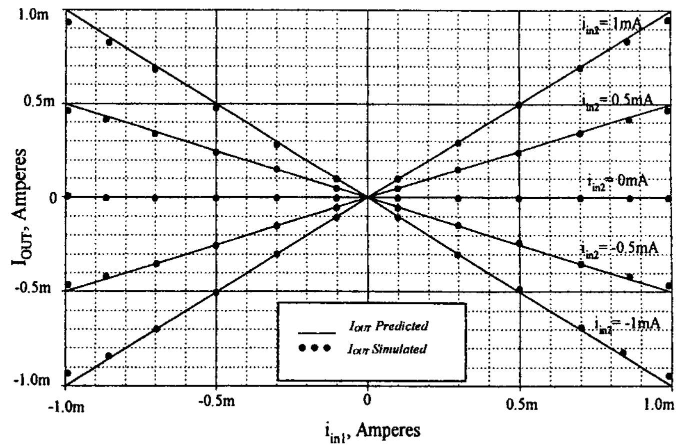

Fig. 5 Simulated DC transfer characteristic of the multiplier-divider.

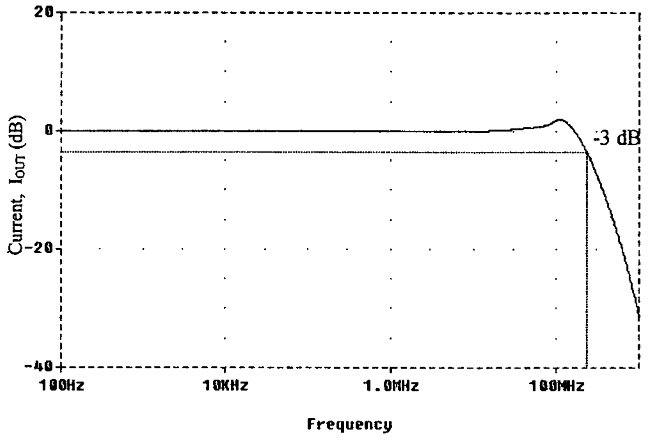

Fig. 6 Frequency response of current-mode multiplier-divider circuit using OTAs.

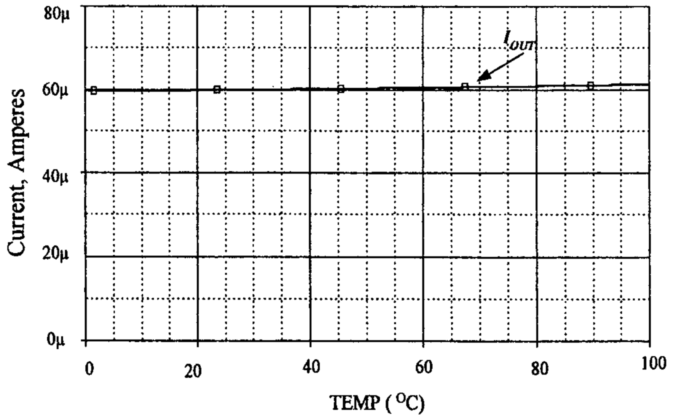

Fig. 7 Frequency response of current-mode multiplier-divider circuit using OTAs.

4. Conclusions

In this paper, we have proposed a temperature compensated analog multiplier-divider circuit that realized through the use of OTAs. The circuit does not require any external passive circuit element. Since, the OTA is a commercially available, a low cost device that incorporates all the attractive features of an OA, therefore, the scheme that employs OTA as a standard cell is simple and can be easily constructed from readily available cells. Simulation results that demonstrate the performances of the multiplier-divider circuit are included.

5. Acknowledgements

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References

[1] Weixin Gai, Hongyi Chen, and E. Seevinck, "Quadratic-translinear CMOS multiplier-divider circuit", *Electron. Letts.*, vol.33, pp.860-861, 1997.

[2] I. Baturone, S. Sanchez-Solano, and J.L. Huertas, "A CMOS current-mode multiplier-divider circuit", *Proc. ISCAS 1998*, pp.520-523, 1998.

[3] Bogdan M. "analog multiplier-divider circuit", *Proc. 1998 IEEE International Symposium on Industrial Electronics*, pp.493-496, 1998.

[4] M. T. Abuelma'atti and M.A. Al-Qahtani, "A current-mode current-controlled current-conveyor-based analogue multiplier/divider", *International Journal of Electronics*, vol.85, pp.71-77, 1998.

[5] R. L. Geiger and E. Sanchez-Sinencio, "Active filter design using operational transconductance amplifiers: A tutorial", *IEEE Circuits Device Mag.*, vol.1, pp.20-32, 1985.

[6] W. Surakampontorn, V. Riewruja, K. Kumwachara, C. Surawatpunya and K. Anuntahirunrat, "Temperature-insensitive voltage-to-current converter and its applications", *IEEE Trans. Instrum. Meas.*, vol.48, pp.1270-1277, 1999.

[7] J. Sila-Martinez and E. Sanchez-Sinencio, "Analogue OTA multiplier without input voltage swing restrictions, and temperature-compensated', *Electron. Letts.*, vol.22, pp.599-600, 1986.