40-GHz-band Low Noise Amplifier MMIC with Ultra Low Gain Flatness

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Abstract: This paper introduces the design and implementation of 40-GHz-band low noise amplifier (LNA) with ultra low gain flatness for wide-band wireless multimedia and satellite communication systems. The 40-GHz-band 4-stage LNA MMIC (Monolithic Microwave Integrated Circuit) demonstrates a small signal gain of more than 20 dB, an input return loss of 10.3 dB, and an output return loss of 16.3 dB for 37□42 GHz. The gain flatness of the 40-GHz-band 4-stage LNA MMIC was 0.1 dB for 37□42 GHz. The noise figure of the 40 GHz-band LNA was simulated to be less than 2.7 dB for 37~42 GHz. The chip size of the 4-stage LNA MMIC was 3.7×1.7 mm^2.

1. Introduction

In recent years, there has been a great growth in mm-wave applications [1]. Monolithic implementation is a key technology for small size, high reliability, good repeatability, high producibility, and low cost because the conventional hybrid IC implementation has a limitation in the high-frequency range due to passive elements with unpredictable parasitics, an operational frequency limit, large size, and, therefore, low producibility.

In this paper, 40-GHz-band LNA MMIC designed and fabricated by using ETRI GaAs 0.2μm PHEMT technology for wide-band wireless LAN systems and satellite communication systems are presented. Also, the fabricated 40-GHz-band LNA MMIC demonstrates a low gain flatness for 37~42 GHz.

2. 40-GHz-band LNA MMIC Design

The schematic of the designed 40-GHz-band 4-stage LNA is shown in Fig. 1. The 40-GHz-band LNA with an operating frequency range of 39~46 GHz is designed using ETRI GaAs 0.2 μm PHEMT with a T-shaped gate for low-noise characteristics. The matching circuits of the LNA are used by open-stubs and microstrip lines. Input matching is adopted for noise-figure minimization, together with gain maximization of LNA. The f_T of the PHEMT for the 40-GHz-band LNA design is 62 GHz, and the maximum stable gain (MSG) of the PHEMT is 9.0~9.8dB for the 40-GHz band. Then, the first stage gain of the 40-GHz-band LNA is adjusted to become maximal, and its noise figure is adjusted to become minimal. Consequently, to obtain a small noise figure for the 40-GHz-band multi-stage LNA is to repeatedly connect the first stage to make it multi-stage. Also, the gate bias circuits of LNA are designed using a 630-Ω NiCr resistor to obtain a low gain flatness for the operating frequency. The simulated S-parameter result of the designed 4-stage LNA is shown in Fig. 2. The designed 4-stage LNA using schematic simulator, LIBRA™, was simulated for a gain of more than 18 dB, a gain flatness of 0.6 dB, an input return loss of more than 10.1 dB, and an output return loss of more than 13.2 dB at 39~46 GHz.

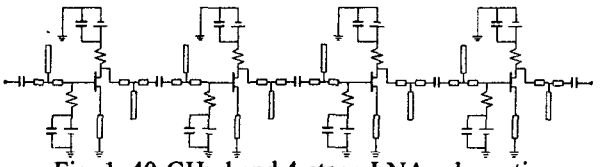
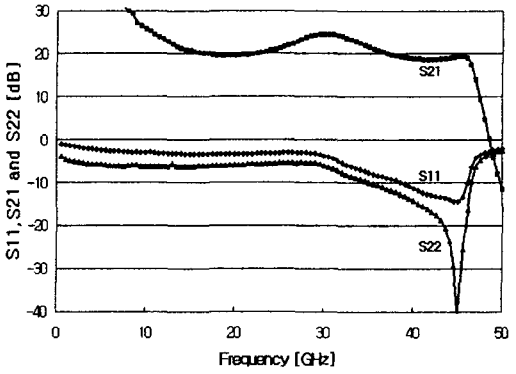
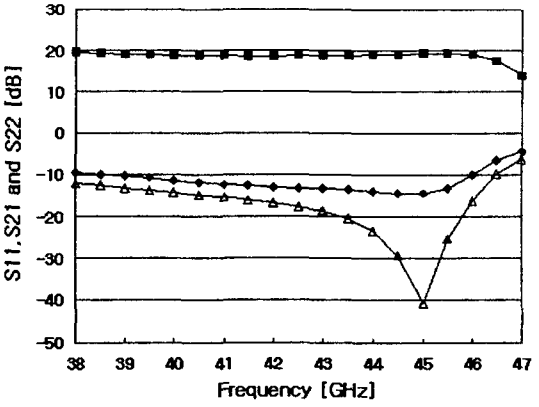


Fig. 1. 40-GHz-band 4-stage LNA schematic



(a) S-parameter for 1 ~ 50 GHz



(b) S-parameter for 38 ~ 47 GHz

Fig. 2. Simulated results of the designed LNA (using schematic simulator)

The noise figure of the designed 4-stage LNA using the schematic simulator is less than 3.9 dB at 39~46 GHz, as shown in Fig. 3. To get stable operation of the 40-GHz-band 4-stage LNA, we inserted the microstrip lines between the sources of the PHEMT and the via holes with a stability

factor, K, of more than 1 and another stability factor, B1, of more than 0 at DC~100 GHz, as shown in Fig. 4. The external DC biasing conditions of V_d and V_g are 4.8 V and -0.1 V, respectively, and the total current consumption of the designed 4-stage LNA is 33 mA.

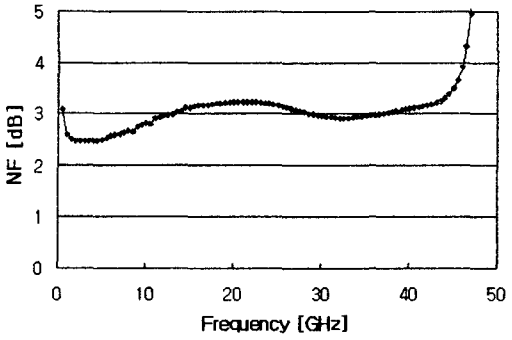


Fig. 3. Noise figure of the designed LNA (using schematic simulator)

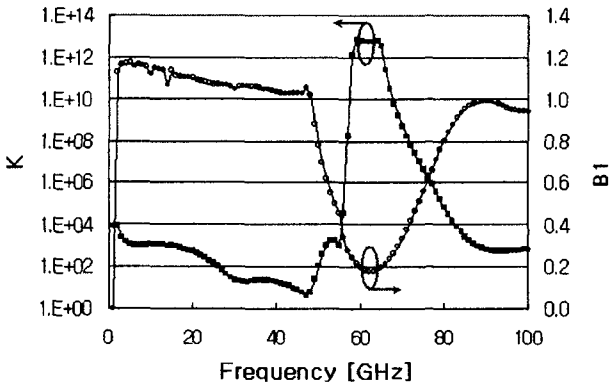
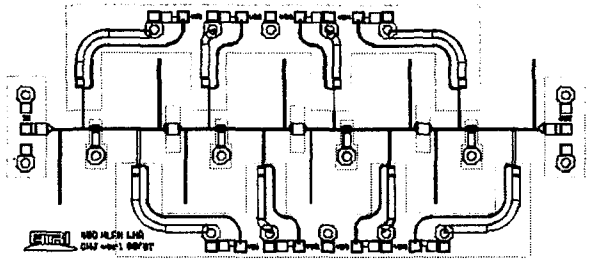
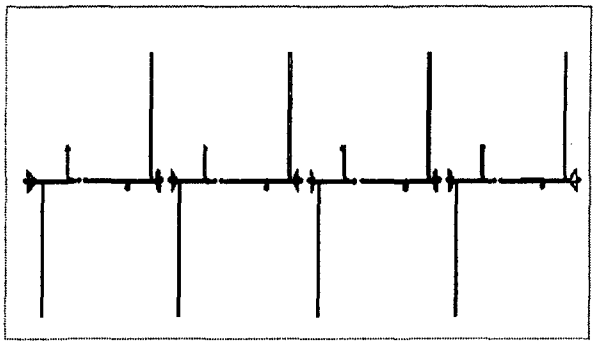


Fig. 4. Stability of the designed LNA for DC~100 GHz

The layout of the designed 40-GHz-band 4-stage LNA MMIC for the ETRI GaAs 0.2μm PHEMT process is shown in Fig. 5(a). The electro-magnetic (EM) simulator, MOMENTUM™, can simulate only passive element, not active device. Therefore, there was excluded PHEMT devices, MIM capacitors, DC bias circuits, and via holes of the 40-GHz-band LNA MMIC layout for EM simulation to get more exact performance estimation, as shown in Fig. 5 (b).



(a) 40-GHz-band LNA MMIC layout



(b) Microstrip lines, open stubs, and ports of the designed LNA for EM simulation

Fig. 5. Layout for EM simulation

Fig. 6 shows comparison the EM simulation with the schematic simulation of the designed 40-GHz-band LNA for 1~50 GHz. The EM simulated S-parameter comparing the schematic simulated S-parameter is shifted down of the operating frequency for the designed LNA, as shown in Fig. 5. The frequency shift was caused by the coupling effects of microstrip lines and open stubs in the designed LNA layout. The noise figure of the designed 4-stage LNA using the EM simulator is less than 2.7 dB at 37~42 GHz, as shown in Fig. 7.

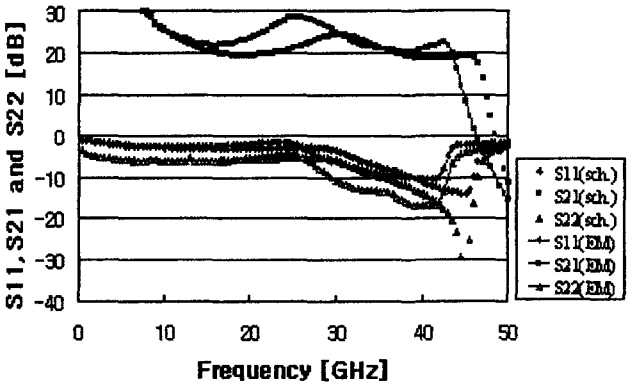


Fig. 6. Comparison the EM simulated results with the schematic

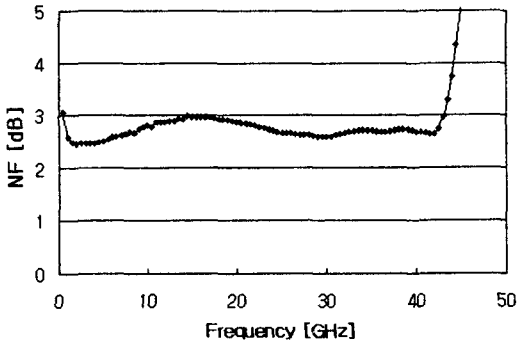


Fig. 7. Noise figure of the designed LNA (using EM simulator)

3. 40-GHz-band LNA MMIC Performance

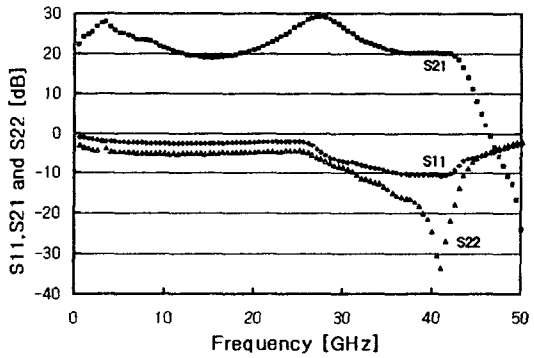
The designed LNA MMIC was fabricated by using the 0.2-μm PHEMT process in ETRI. Fig. 8 shows a photograph of the fabricated LNA MMIC. The chip size of the fabricated 40GHz-band LNA MMIC is 3.7×1.7 mm^2.

Fig. 8. Photograph of the fabricated 40 GHz LNA MMIC

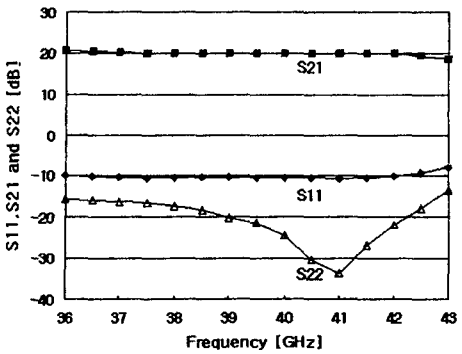
The GSG (ground-signal-ground) pads on the fabricated MMIC chips are for RF input and output on-wafer probing. Each pad has a size of 80×80 μm^2 and a pad-to-pad pitch of 150 μm. The GPGPGPGPG pads are used for the DC bias probing of the fabricated 40-GHz-band LNA MMIC.

On-wafer measurements of the fabricated 40-GHz-band LNA MMIC were performed with a probe-station, an HP8510C network analyzer, an HP83650B signal generator, and an HP8565E spectrum analyzer. The fabricated 4-stage LNA MMIC was measured to show a gain of more than 20 dB, a gain flatness of 0.1 dB, an input return loss of more than 10.3 dB, and an output return loss of more than 16.3 dB at 37~42 GHz, as shown in Fig. 9(a) and (b). The gain of the fabricated 40-GHz-band 4-stage LNA MMIC is better by 6 dB than that of LNA MMIC [5]. The input 1 dB gain compression point (IP_{1dB}) of the fabricated 40-GHz-band 4-stage LNA MMIC was measured to be –10 dBm at 40 GHz, as shown in Fig. 9(c).

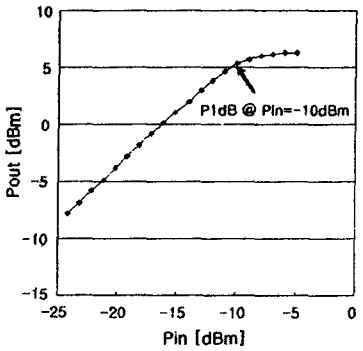
Fig. 10(a) shows comparison the measured S-parameter of the fabricated 40-GHz-band LNA MMIC with the schematic simulation of the designed LNA for 1~50 GHz. The measured S-parameter of the fabricated LNA MMIC comparing the schematic simulated S-parameter is shifted down of the operating frequency for the designed LNA. On the contrary, Fig. 10(b) shows that the measured S-parameter of the fabricated LNA MMIC was similar to the EM simulated S-parameter of the designed LNA for 1~50 GHz.



(a) S-parameter for 1 ~ 50 GHz

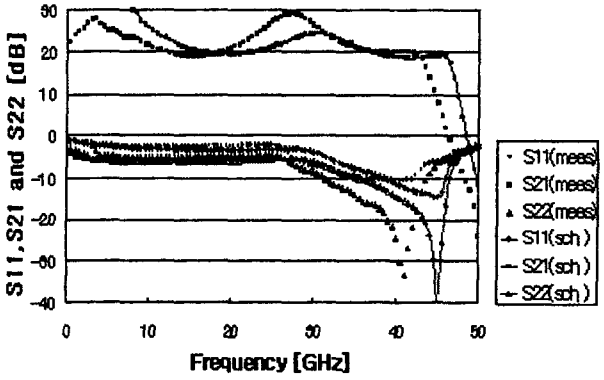


(b) S-parameter for 36 ~ 43 GHz

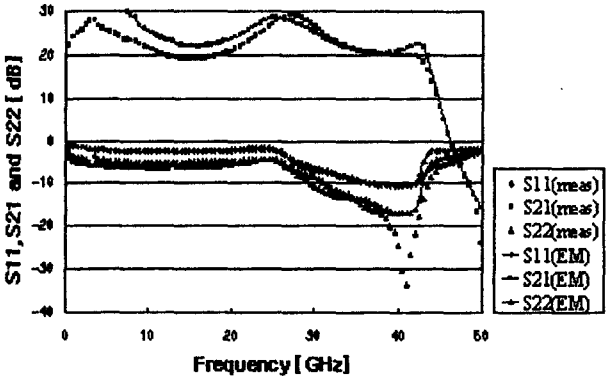


(c) Input P_{1dB}

Fig. 9. Measured results of the fabricated LNA MMIC



(a) Comparison the measured results with the schematic simulation



(b) Comparison the measured results with EM simulation

Fig. 10. Comparison the measured results with simulations of 40-GHz-band LNA MMIC

4. Conclusion

This paper introduces the design and implementation of 40-GHz-band LNA MMIC with low gain flatness for wide-band wireless multimedia and satellite communication systems. The 40-GHz-band LNA MMIC demonstrates a small signal gain of more than 20 dB, an input return loss of 10.3 dB, and an output return loss of 16.3 dB for 37□42 GHz. The fabricated 40-GHz-band LNA MMIC has the ultra low gain flatness of 0.1 dB for 37□42 GHz. The measured S-parameter of the fabricated LNA MMIC was similar to the EM simulated S-parameter of the designed LNA for 1~50 GHz. The measured IP_{1dB} of the fabricated 40-GHz-band LNA MMIC was –10 dBm at 40 GHz. The chip sizes of the LNA MMIC is 3.7×1.7 mm^2.

References

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