Voltage-Mode CMOS Squarer/Multiplier Circuit

B. Boonchu[1] and *W. Surakampontorn*[2]
[1]Mahanakorn University of Technology,
51 Cheum-Sumpan Road, Nong-Chock District Bangkok, Thailand 10530
Phone (662)9883655 ext.239 Fax (662)9883687 Email: boonchai@mut.ac.th
[2]King Mongkut's Institute of Technology Ladkrabang
Ladkrabang, Bangkok 10520, Thailand.Phone: (662) 326-9968, Fax: (662) 739-2398 Email: kswanlop@kmitl.ac.th

Abstract: In this paper, a low-voltage CMOS squarer and a four-quadrant analog multiplier are presented. It is based on a source-coupled pair and a scaled-floating voltage generator which are modified to work as a voltage squaring and a sum/difference circuits. The proposed squarer/multiplier have been simulated with HSPICE, where $-3dB$ bandwidth of $10MHz$ is achieved. The power consumption is about $0.6mW$, from a $\pm 1.5V$ supply, and the total harmonic distortion is less than 0.7%, with a $1.2V$ peak-to-peak $1MHz$ input signal.

Introduction

A squarer circuit is an importance basic building block for the design of analog nonlinear function circuits, for examples, frequency translation, waveform generation, neural networks, and it can be applied to work as a quarter-square multiplier circuit. Usually, the common-source differential squaring circuit configuration as a two-input NOR gate with resistance load is widely used for the design of squarer/multiplier circuits in CMOS technologies [1]-[2]. The other approaches are that based on square-law current to voltage characteristics of MOS transistor which are biased in the saturatoin and nonsaturation region [3]-[9]. The squarer and multiplier proposed in this paper also use the square-law of the MOS transistor. But, however, the proposed circuit does not require resistors to obtain the output signal in voltage [10].

2. Circuit Description

2.1 MOS Differential Squaring Circuit

Fig. 1 shows the voltage-mode squaring circuit and its symbol which is made up of a differential-input source-coupled pair. Assuming that all NMOS devices are biased in the saturation region with individual wells connected to their sources to eliminate the body effect [3]. Let M_1 and M_2 are identical, and the aspect ratio of M_3 be twice that of M_1. If the differential-input voltage V_d, with the same common-mode dc voltage V_C is applied, the drain currents of MOS transistors can be expressed as

$$I_{d1} = K_1(V_C + \frac{V_d}{2} - V_o - V_T)^2 \quad (1)$$

$$I_{d2} = K_2(V_C - \frac{V_d}{2} - V_o - V_T)^2 \quad (2)$$

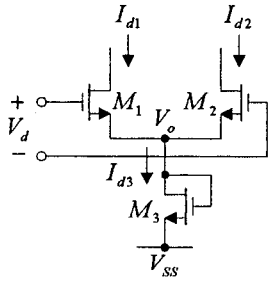
$$I_{d3} = K_3(V_o - V_{SS} - V_T)^2 \quad (3)$$

$$I_{d1} + I_{d2} = I_{d3} \quad (4)$$

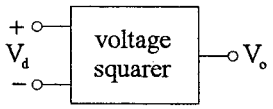
where $K_i = \mu_n C_{ox} W_i / 2L_i$ is transconductance parameter, μ_n is the effective surface mobility, C_{ox} is the gate capacitance per unit area , and V_T is the threshold voltage of the transistor, respectively. The output voltage V_o becomes

$$V_o = \frac{(V_C - V_T)^2 - (V_{SS} + V_T)^2}{2(V_C - V_{SS} - 2V_T)} + \frac{V_d^2}{8(V_C - V_{SS} - 2V_T)} \quad (5)$$

The output voltage V_o is related to the square of the differential-input voltage V_d. The eqns. (1)-(5) are valid if $(V_C - V_{SS} - V_d/2) > 2V_T$, where all devices are biased in the saturation mode.



(a)



(b)

Fig. 1. Voltage-mode squaring circuit (a) circuit and (b) symbol.

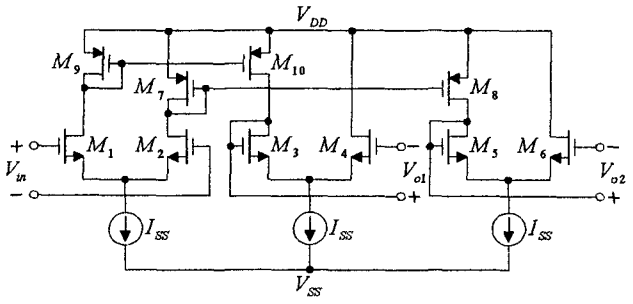
2.2 Scaled Differential-Voltage Generator

A circuit for generating differential-voltage generator is shown in Fig. 2 [8]. Matched transistor M_1 and M_2 form an input differential pair, while the other four identical NMOS devices, M_3, M_4 and M_5, M_6 form floating differential outputs that are biased by current sources I_{SS}

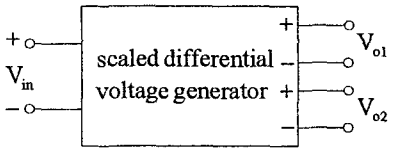
of the same magnitude. If voltage V_{in} is applied to the input, the output voltages V_{o1} and V_{o2} can be given by

$$V_{o1} = -V_{o2} = \sqrt{\frac{K_3}{K_1}} V_{in} \tag{6}$$

The output voltages is a scaled voltage which is equal to input voltage multiplied by a factor that is depend on transconductance parameter of the transistors M_3 and M_1



(a)



(b)

Fig. 2. Scaled differential-voltage generator (a) circuit and (b) its symbol.

2.3 Voltage-Mode Squaring Circuit

By combining the voltage squarer circuit and the scaled differential-voltage that shown in Fig. 1 and Fig.2, respectively, the block diagram of the voltage-mode squaring circuit is shown in Fig. 3, where the reference voltage V_{ref} is the constant dc voltage, V_{in} and V_o are the input and output voltage respectively. From eqns.(5)-(6) we find that

$$V_o = \frac{(V_{ref} - V_T)^2 - (V_{SS} + V_T)^2}{2(V_{ref} - V_{SS} - 2V_T)} + \frac{V_{in}^2}{2(V_{ref} - V_{SS} - 2V_T)} \tag{7}$$

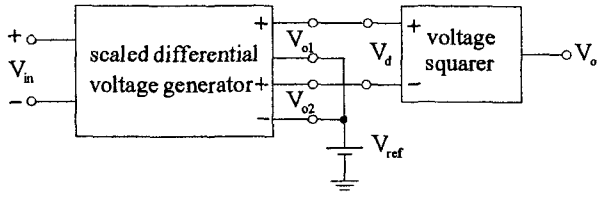


Fig. 3. Block diagram of the proposed squaring circuit.

The eqn.(7) shows that the output voltage V_o is equal to the square of the input voltage V_{in} and a factor which is in the form of the voltage reference V_{ref}. Then, we can adjust the output-offset voltage and the magnitude of V_{in}^2 by tuning V_{ref}.

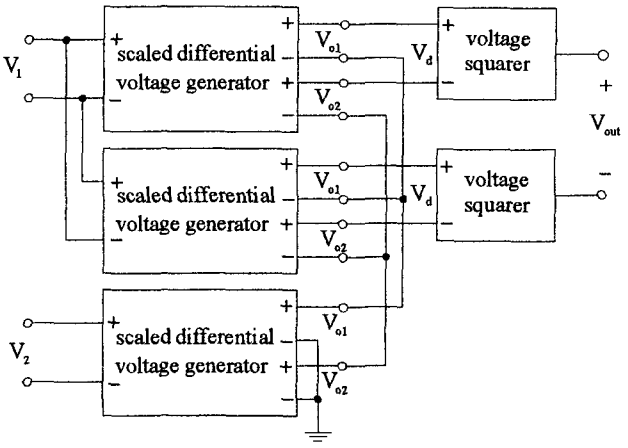


Fig. 4. Block diagram of the proposed multiplier.

2.4 Voltage-Mode Four-Quadrant Multiplier

Fig. 4 shows a block diagram of the four-quadrant analog multiplier that consists of three basic scaled differential-voltage generator and two voltage squarer, where V_1, V_2 and V_{out} are the input and output voltage of the multiplier, respectively. From the quarter-square algebraic identity $(V_1+V_2)^2 - (V_1-V_2)^2 = 4V_1V_2$, therefore, the output voltage of the voltage-mode multiplier can be written as

$$V_{out} = \frac{(V_1+V_2)^2 - (V_1-V_2)^2}{8(V_C - V_{SS} - 2V_T)}$$

$$= \frac{V_1 V_2}{2(V_C - V_{SS} - 2V_T)} \tag{8}$$

The output voltage is equal to the multiplication of the two input voltage and a factor which is in the form of the common-mode dc voltage V_C and the power supply voltage V_{SS}. Consider the multiplier circuit block diagram in Fig. 4, if we set both the input voltages to zero, then V_C will be zero.

The channel length modulation, which causes the effective channel length, and thus the device W/L ratio, to be a function of the device drain-to-source voltage. However, this effect can be neglected if the long channel transistors are used.

3. Simulation Results

The proposed squarer/multiplier circuit have been simulated by HSPICE using the model parameters of HP 0.5μ level 49 CMOS process. For the voltage-mode squaring circuit that is shown in Fig. 1, the aspect ratios of transistors $M_1 - M_2$ are 5/5, and M_3 is 10/5. The ratios

of the devices of the scaled differential-voltage generator that is shown in Fig. 2, $M_1 - M_6$ and $M_7 - M_{10}$ are 5/10 and 20/5, respectively. The power supply voltage is $\pm 1.5V$ and the bias current I_{SS} is $20\mu A$.

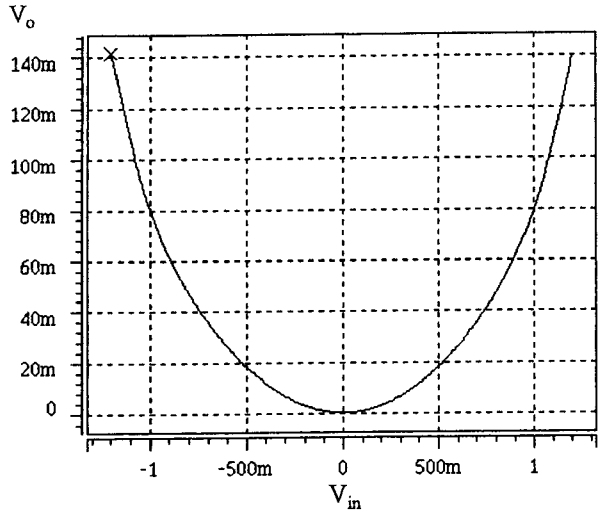


Fig. 5. The transfer characteristic curves of the squaring circuit.

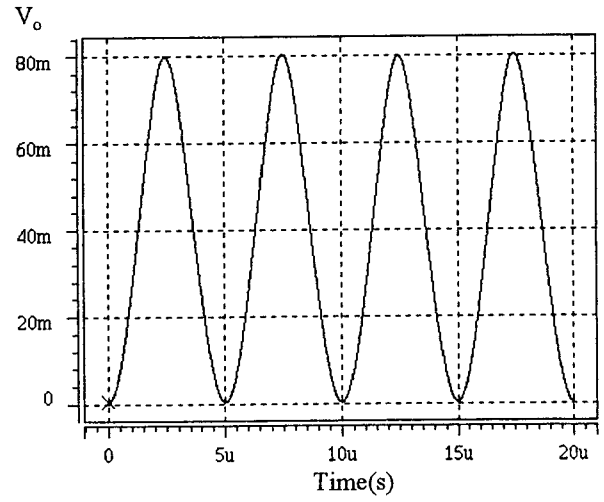


Fig. 6. The output waveform of the proposed squaring circuit

Fig.5 and Fig.6 show the simulations for the voltage-mode squaring circuit. The transfer characteristic curve is shown, where V_{in} is varied from $-1.2V$ to $1.2V$. The output signal shown in Fig.6 is measured by applying the sinusoidal input voltage V_{in} with peak amplitude of $1V$ and the frequency is $100kHz$.

The dc characteristic curves of the proposed multiplier are shown in Fig. 7, for the input voltage V_1 varied from $-0.6V$ to $0.6V$ and V_2 changing from $-0.6V$ to $0.6V$ with $200mV$ steps.

Fig.8 demonstrates the use of this multiplier as an amplitude modulator, a $100kHz$ sine wave is modulated by $2MHz$, where the amplitude of the signals are $500mV$

The total harmonic distortion is measured by setting V_2 to $600mV$ dc voltage. V_1 is the sinusoidal signal with peak amplitude of $600mV$ and the frequency is $1MHz$. The simulated maximum THD is about 0.7%, and the power consumption is about $550\mu W$.

To measure the frequency characteristic of the multiplier, a $600mV$ dc voltage is applied to V_2 while V_1 is the variable frequency sinusoidal input current with peak amplitude of $600mV$. From the simulation, the $-3dB$ bandwidth up to $10MHz$ is achieved.

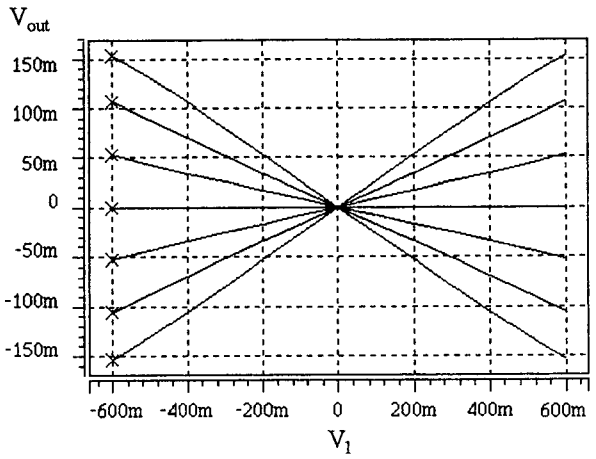


Fig. 7. The transfer characteristic curves of the multiplier

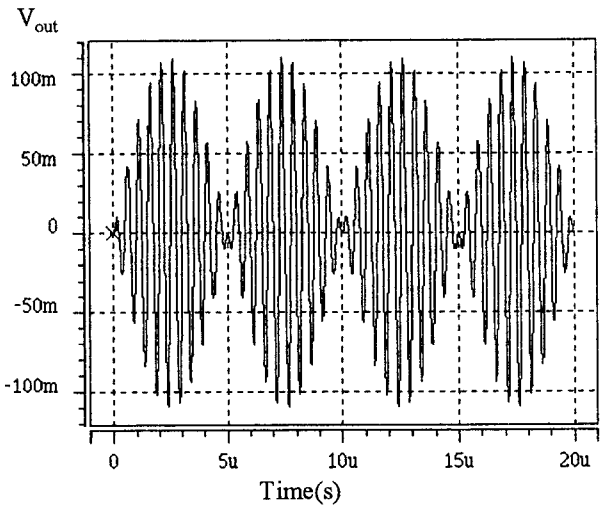


Fig. 8. Amplitude modulation of the two sinusoidal input signals

4. Conclusion

A new CMOS voltage-mode squarer and four-quadrant analog multiplier base on the differential-input source-coupled pair and scaled differential-voltage generator have been presented. To obtain the output voltage, the proposed circuits are performed by using the voltage-mode squaring circuits which does not require a resistor. There performances have been demonstrated by using HSPICE simulations.

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