A Multi-Stage CMOS Charge Pump for Low-Voltage Memories

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Abstract: To remedy both the degradation and saturation of the output voltages in the modified Dickson pump, a new multi-stage charge pump circuit is presented in this paper. Here using PMOS charge-transfer switches instead of NMOS ones eliminates the necessity of diode-configured output stage in the modified-Dickson pump, achieving the improved voltage pumping gain and its output voltages proportional to the stage numbers. Measurement indicates that VOUT/3VDD of this new pump circuit with two stages reaches to a value as high as 0.94V even with low VDD=1.0 V, strongly addressing that this scheme is very favorable at low-voltage memory applications.

1. Introduction

Multi-stage charge pumps have been investigated for many years since they can generate higher voltages than supply voltage (VDD) that are used in programming and erasing in nonvolatile memories such as EEPROMs. In addition, they can also be used in programming the antifuses for post-package fail-bit repair scheme in recent high-density DRAMs [1]. Most MOS charge pumps are based on the circuit proposed by J. Dickson that comprises the diode-configured switches and the pumping capacitors controlled by two out-of-phase clocks (CLK and CLKB) [2]. However, since its voltage pumping gain is significantly reduced with VDD decreasing, some modifications have been carried out to alleviate this gain reduction [3].

One of these modified Dickson pumps is using high-voltage-driven charge-transfer switches that do not lose the pumping voltages, as proposed in NCP-2 scheme in [3]. An example of NCP-2 with two stages is shown in Figure 1, where MD's are the diode-configured transfer switches and MS's are the charge-transfer switches. MN's and MP's are the control switches that control the gates of the charge-transfer switches dynamically, respectively, and C1, C2, and C3 are the pumping capacitors. CLK and CLKB are representing two out-of-phase clocks and VOUT is the output voltage at the load capacitor CL. As stated earlier, using high voltage-driven charge-transfer switches in parallel with diode-configured switches as shown in Figure 1 can eliminate the sacrificial voltage loss when they deliver the generated voltages into the next nodes. However, NCP-2 scheme in Fig. 1 still suffers from the threshold voltage loss due to the diode configuration at the output stage. As shown in Fig. 1, MD0 loses the pumping voltage by a voltage as large as V_{TH} (threshold voltage) of MD0. This degrades the voltage pumping gain especially at low-VDD operation. This can be seen in Fig. 6, where straight line is corresponding to highest voltages that can be generated by charge pump and symbols of solid-circle show voltages generated by NCP-2 in Fig.1. When the stage number is two, 3VDD is highest voltage to generate. In Fig. 6, VOUT/3VDD is 0.7 when VDD is 2.4V and VOUNT/3VDD is 0.55 when VDD is 0.6V, indicating that the degradation of VOUT becomes severe with decreasing VDD. Another problem of NCP-2 is that the output voltages of NCP-2 scheme begin to saturate after they reach to around 7 V in spite of increasing the stage number, as shown in Fig. 7. This also is due to the constraint imposed by its diode-configured output stage, as shown in Fig. 1.

To remedy both the degradation and saturation of the output voltage in NCP-2, we propose a new multi-stage charge pump circuit in this paper. Here using PMOS charge-transfer switches instead of NMOS ones eliminates the necessity of diode-configured output stage in NCP-2, achieving improved voltage pumping gain and output voltage proportional to the stage number. Moreover, the pumping efficiency of the new charge pump can be improved by using non-overlapping two-phase clocks. At the following section, operations of NCP-2 scheme in Fig. 1 and newly proposed scheme will be explained. At the section 3, comparisons of NCP-2 and this new scheme will be done by HSPICE simulation. And, measured results of this new scheme will also be shown. At the final section 4, we will conclude this paper.

2. Circuit Confugurations and their Operations

First of all, let us see the operation of NCP-2 in Fig. 1 in detail. Unlike the conventional Dickson charge pump having only the diode-configured switches [2], NCP-2 scheme has the charge-transfer switches of MS1 and MS2 that are controlled dynamically via MN1, MN2, MP1, and MP2, in addition to the conventional diode-configured switches MD1 and MD2 [3], as shown in Fig. 1. Let us assume that CLK1 goes low and CLK2 goes high. At this moment, a voltage on the node N2 goes 3VDD and a voltage on the node N1 goes VDD, turning on MP1 and turning off MN1, respectively. Since the charge-transfer switch MS1 being controlled by a voltage on the node N2 via MP1 that is internally boosted, is fully turned on, it can deliver a voltage of VDD into the next node N1 without a voltage loss. Simultaneously, a voltage on the node N2 being boosted to have a value of 3VDD, is delivered to the next node of VOUT via the diode-configured MD0. It should be noted here that a voltage loss as much as VTH of MD0 occurs at MD0, degrading the voltage pumping gain of NCP-2, as already addressed at the section 1.

One more thing to note here is that a voltage on node N5 also is lowered by as much as the threshold voltage of MD3. This sacrificial voltage loss gives rise to the saturation of VOUT's especially when the stage number becomes large. To know why the saturation of VOUT's occurs in NCP-2, let us assume that CLK1 goes high and CLK2 goes low. At this moment, a voltage on the node N5 goes 4VDD-VTH(MD3) and a voltage on the node N2 goes 2VDD. Here VTH(MD3) means the threshold voltage of MD3 in Fig. 1. If V(N5)-V(N2) is large enough to turn on MP2, the gate of MS2 is controlled by the voltage on the node N5 via MP2. Here V(N5) and V(N2) mean voltages on the nodes N5 and N2, respectively. To turn on MS2 fully, V(N5)-V(N1) should be larger than VTH(MS2). Since VTH(MS2) is the threshold voltage under severe body-effect and is though to be a little larger than an absolute value of VTH(MP2) with the body and source voltages tied to each other, it gives more severe constraint in generating VOUT than VTH(MP2). In Fig. 7, you can see that VOUT's begin to saturate around 7V even with increasing the stage number more. This is due to the constraint of VTH(MS2) that comes from the diode-configured MD3. To remedy this saturation of VOUT's with increasing the stage number, NCP-3 with the output stage driven by boosted clock with a magnitude of 2VDD has been suggested in [3]. Though NCP-3 shows that its output voltage is proportional to the stage number, NCP-3 has the more severe gate-oxide stress than NCP-2 in Fig. 1 and requires an auxiliary double-boosted clock generator. In NCP-3, a voltage on the node N5 can reach to as high as 5VDD-VTH, while it is only 4VDD-VTH in NCP-2 as shown in Fig. 2.

To remedy both the degradation and saturation of the output voltage in NCP-2, we propose a new multi-stage charge pump circuit in this paper. Here using PMOS charge-transfer switches instead of NMOS's eliminates the necessity of diode-configured output stage in NCP-2, remedying the drawbacks in NCP-2 stated earlier. A voltage doubler where PMOS charge-transfer switches are used to avoid the threshold voltage loss of NMOS transfer switches has already been proposed [4]. Though PMOS switches can deliver the generated voltages to the load without losses, simultaneously, PMOS switches with higher voltages on their sources than their substrate voltages can lose pumped charges into the parasitic pnp bipolars [4]. To avoid those turning-on's, a doubler where the substrates of PMOS charge-transfer switches are controlled by small-auxiliary PMOS bulk switches to have higher voltages than their source voltages always, has been presented [4].

Fig. 3 shows a simple block-diagram of the proposed 2-stage charge pump circuit using PMOS charge-transfer switches. It consists of a main pump block and an auxiliary pump block. And each of them includes a power-up precharge circuit, a pump control circuit, and an output stage. The power-up precharge circuit sets up the first-stage pumping nodes to have voltages of VCC [5]. And, the role of the auxiliary pump is that the substrates of PMOS charge-transfer switches have higher voltages than their sources, as stated just earlier. The auxiliary pump block has the same scheme with the main pump block but sizes of the switches are much smaller than the main pump block.

More detailed scheme is shown in Fig. 4. Here two power-up precharge circuits (PPC) consist of MP0, MP1, MP2, MP3, MN0, and MN1 that are controlled by two-non-overlapping clocks CLK0 and CLK3. C1, C2, C3, and C4 represent the pumping capacitors that are controlled by two clocks CLK1 and CLK2. MP4, MP5, MP6, MP7, MN2, and MN3 control the PMOS charge-transfer switches of MP6 and MP7. MP8 and MP9 deliver the generated voltages into the output load capacitor CL. In Fig. 4, four clocks are used. The detailed waveforms of nodes and 4 clocks are shown in Fig. 5. To simplify the circuit diagram, the auxiliary pump circuit is represented by a box. As stated earlier, the auxiliary pump is the same with the main pump shown in Fig. 4 but only the sizes are different.

Now let us see the operation of the power-up precharge circuit in Fig. 4. When CLK0 goes low and CLK1 goes high, MN0 is turned off and MP1 is turned on. At this moment, a voltage on the node N2 becomes 2VDD and turns off MP0 via MP1. At the other side, CLK2 goes low and CLK3 goes high, turning on MN1 and turning off MP3. At this time, since MP2 is turned on via MP3, the node N3 is precharged by a voltage of VDD. The operation of the main pump circuit to fully turn on the gates of the charge-transfer switches of MP6 and MP7 is as follows. When CLK1 goes high and CLK2 goes low, voltages on the nodes N2, N3, N4 and N5 are 2VDD, VDD, 2VDD and 3VDD, respectively. If a voltage of VDD is larger than the threshold voltages of PMOS and NMOS, a voltage on the node N6 becomes VDD via MN2 and a voltage on the node N7 becomes 3VDD via MP5. Thus, a voltage on the node N4 becomes the same with a voltage on the node N2 via MP6 turned on, and a voltage on the node N5 is separated from a voltage on the node N3 via MP7 turned off. At this moment, a boosted voltage of 3VDD on the N5 is fully delivered to the output without the threshold voltage loss via MP9 that is turned on by a voltage of 2VDD on the node N4.

On the other hand, when CLK1 goes low and CLK2 goes high, voltages on the nodes N2, N3, N4 and N5 are VDD, 2VDD, 3VDD and 2VDD, respectively. At this moment, MP6 is turned off via MP4 and MP7 is turned on via MN3. A boosted voltage of 3VDD on the node N4 is delivered to the output load without the loss, as the same with when CLK1 is high and CLK2 is low.

3. Simulation and Measurement

To verify the operation of the proposed circuit, HSPICE simulation with a 0.12-? m triple-well CMOS technology was performed. Fig. 6 shows the output voltages of the proposed circuit compared with the modified Dickson pump (NCP-2) in a VDD range of 0.0V-2.5V. This figure clearly shows that the proposed charge pump circuit can generate higher voltages than the modified Dickson pump (NCP-2). In Fig. 7, the output voltages of the proposed circuit and the modified Dickson pump are compared with increasing the stage number (N). Here it can be seen that the output voltage of the proposed circuit is proportional to the stage number (N) without indicating any saturation. Fig. 8 shows output voltages of the 2-stage new pump shown in Figure 4 with varying VDD. This figure

indicates that almost 3VDD can be generated by using newly proposed pump scheme in Figure 4 with two stages when VDD ranges from 1V to 1.75V. The degradation of VOUT's is observed in Fig. 8, since the fabrication process does not support high-voltage tolerable CMOS devices.

4. Conclusion

To remedy both the degradation and saturation of the output voltages in the modified Dickson pump, a new multi-stage charge pump circuit is presented in this paper. This new pump using PMOS charge-transfer switches instead of NMOS ones achieves improved voltage pumping gain and its output voltages are shown to be proportional to the stage numbers unlike the previous modified Dickson pump. Measurements and simulations indicate that this new pump is very favorable in particular at low VDD applications.

Acknowledgements

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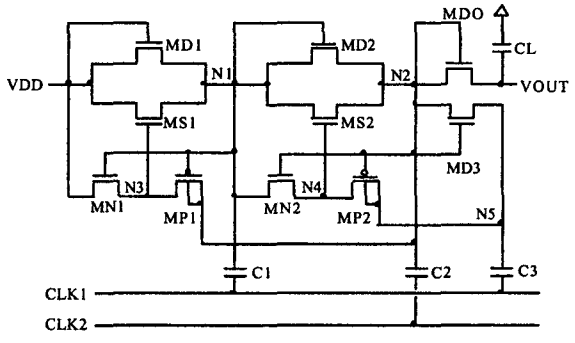

Fig. 1. Modified Dickson pump circuit (NCP-2) that has been proposed in [3].

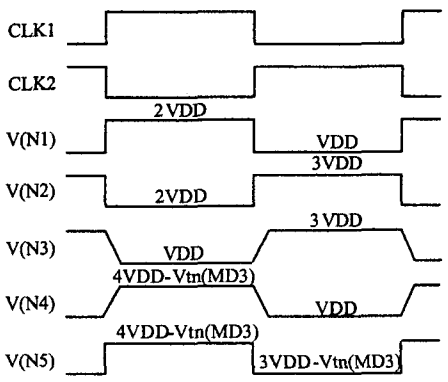

Fig. 2. Waveforms of the modified Dickson pump circuit (NCP-2) shown in Fig. 1.

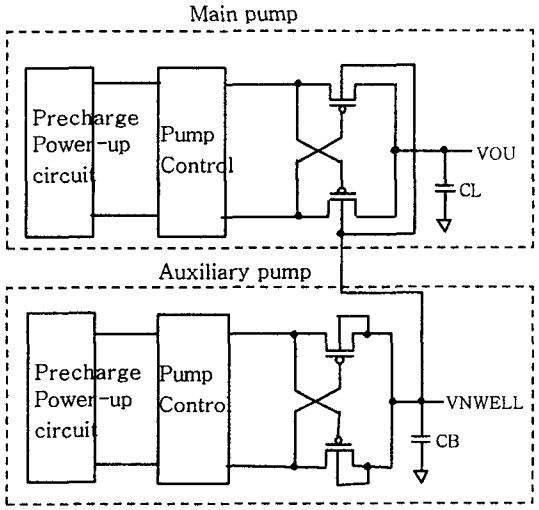

Fig. 3. Simple block diagram of newly proposed pump circuit with 2 stages.

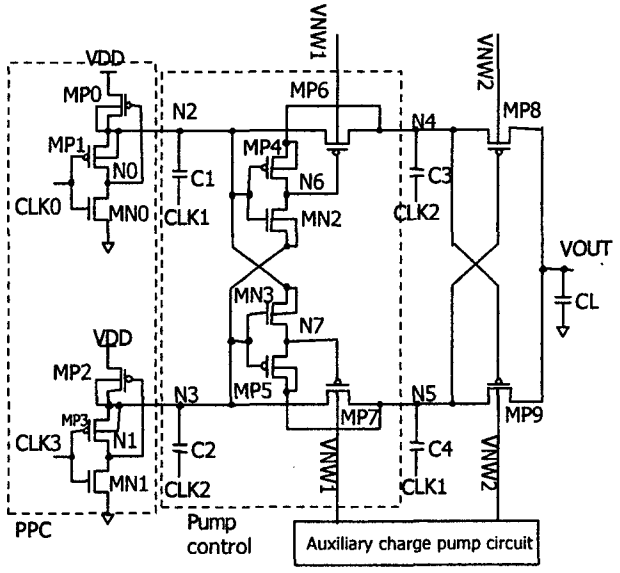

Fig. 4. Newly proposed 2-stage charge pump circuit.

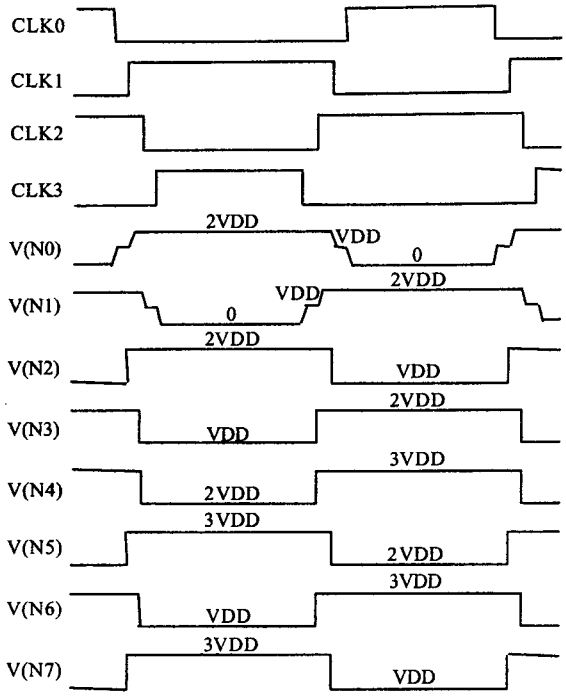

Fig. 5. Waveforms of the signals that are shown in Fig. 4.

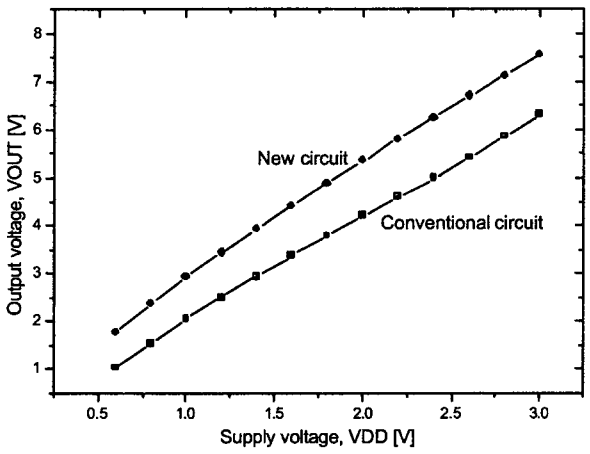

Fig. 6. Output voltages of the 2-stage modified Dickson pump (NCP-2) shown in Fig. 1 and the 2-stage new pump shown in Fig. 4 with varying VDD. The conventional circuit in this figure represents NCP-2 scheme in [3].

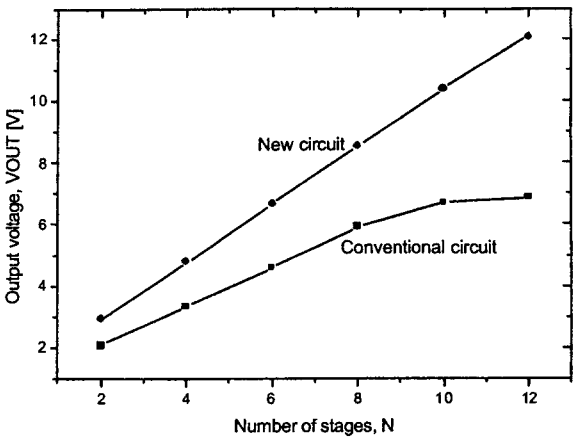

Fig. 7. Output voltages of the 2-stage modified Dickson pump (NCP-2) shown in Fig. 1 and the 2-stage new pump shown in Fig. 4 with varying the stage number (N). The conventional circuit in this figure represents NCP-2 scheme in [3].

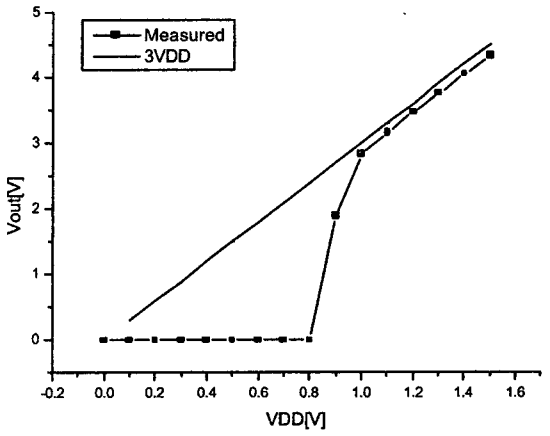

Fig. 8. Output voltages of the 2-stage new pump shown in Figure 4 with varying VDD. This figure indicates that almost 3VDD can be generated by using newly proposed pump scheme in Figure 4 with two stages when VDD ranges from 1V to 1.75V.