Implementation of Systolic Array for the Single-Source Shortest Path Problem

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Abstract : Shortest path problem belongs to the combinatorial optimization problem and plays an important role in the field of computer aided design. It can either be directly applied as in the case of routing or serves as a important subroutine in more complex problems.

In this paper, a systolic array for the SSSP(single-source shortest path problem) was derived. The array was modeled and simulated in RTL level using VHDL, then synthesized to a schematic and finally implemented to a layout using the cell library based on 0.35 μm CMOS 1-poly 4-metal CMOS technology.

1. Introduction

A systolic array [1], [2] formed by interconnecting a set of identical data-processing cells in a uniform manner is a combination of an algorithm and a circuit that implements it, and is closely related conceptually to arithmetic pipeline.

In a systolic array, data words flow from external memory in a rhythmic fashion, passing through many cells before the results emerge from the array's boundary cell and return to external memory. The external memory connected to the systolic array's boundary cell stores both input data and results. Upon receiving data words, each cell performs same operation and transmits the intermediate results and data words to adjacent cells synchronously.

The name systolic derives from the rhythmic nature of the data flow, which can be compared with the rhythmic contraction of the heart in pumping blood through the body.

The underlying principle of systolic array is to achieve massive parallelism with a minimum communication overhead, and generally speaking, a systolic array is easy to implement because of its regularity and easy to reconfigure because of its modularity.

This paper proposes a systolic array for the single-source shortest path problem. It was simulated in RTL level using VHDL [3], [4], synthesized to a schematic, and then implemented automatically using the cell library based on 0.35 μm CMOS 1-poly 4-metal CMOS technology.

2. Single Source Shortest Path Problem

For a given graph $G=(V, E)$, single-source shortest path problem is to find a shortest path from a given source vertex $u \in V$ to every vertex $v \in V$ [5].

Let the number of vertices of G be denoted by n, and suppose we have a set of i vertices (where $1 \le i \le n$), W_i, which satisfies the proprieties [6]:

1) $u \in W_i$
2) for any $w \in W_i$, the shortest u-w path contains only intermediate vertices in W_i.

For any vertex v of G, let $d(i, v)$ denote the length of the shortest u-v path containing only intermediate vertices from W_i (hence, if $v \in W_i$, then $d(i, v)$ is the length of the shortest u-v path). Let $v(i)$ be the vertex not in W_i which has the smallest distance $d(i, v)$ value. Then $d(i, v(i))$ is in fact the length of the shortest u-$v(i)$ path, since using other vertices not in W_i would lead to a longer path.

Hence, if we define $W_{i+1} = W_i \cup \{v(i)\}$, then W_{i+1} also satisfies proprieties 1) and 2) above.

We obtain the following recurrence relation :

$$d(i+1, v) = d(i, v), \text{ if } v \in W_{i+1},\ i \ge 1.$$

$$d(i+1, v) = \min\{d(i, v), d(i, v(i)) + w(v(i), v)\}, \text{ if } v \notin W_{i+1},\ i \ge 1.$$

The initial values are given by :

$d(i,v)=0$, if $v=u$

$d(i,v)=w(u,v)$, if $v \neq u$

For a sample graph, G, composed of eight nodes, Fig. 1, the elements of its distance matrix A are defined as follows :

1. $a_{ij}=$ the distance from vertex i to vertex j.
2. $a_{ij}=\infty$ if there is no edge connecting i and j.
3. $a_{ij}=0$ if $i=j$.

The single-source shortest path problem finding a shortest path from a given source vertex $u \in V$ to every vertex $v \in V$ can be solved by recurrence relation defined above. The values of $d(i,v)$ which is the solution of given sample problem are displayed in Table 1.

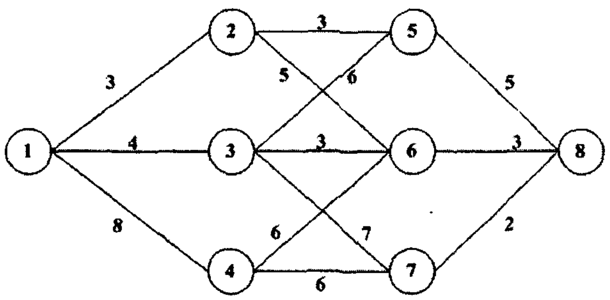

Fig. 1. A graph with edge weight

$$A=\begin{bmatrix} 0 & 3 & 4 & 8 & \infty & \infty & \infty & \infty \\ 3 & 0 & \infty & \infty & 3 & 5 & \infty & \infty \\ 4 & \infty & 0 & \infty & 6 & 3 & 7 & \infty \\ 8 & \infty & \infty & 0 & \infty & 6 & 6 & \infty \\ \infty & 3 & 6 & \infty & 0 & \infty & \infty & 5 \\ \infty & 5 & 3 & 6 & \infty & 0 & \infty & 3 \\ \infty & \infty & 7 & 6 & \infty & \infty & 0 & 2 \\ \infty & \infty & \infty & \infty & 5 & 3 & 2 & 0 \end{bmatrix}$$

Fig. 2. Distance matrix A

Table 1. Calculation of $d(i, v)$

i /v	1	2	3	4	5	6	7	8	V(i)
1	0	3	4	8	∞	∞	∞	∞	2
2	0	3	4	8	6	8	∞	∞	3
3	0	3	4	8	6	7	11	∞	5
4	0	3	4	8	6	7	11	11	6
5	0	3	4	8	6	7	11	10	4
6	0	3	4	8	6	7	11	10	8
7	0	3	4	8	6	7	11	10	7
8	0	3	4	8	6	7	11	10	-

3. Systolic Array Design

In the following, we derive the dependence graph, DG, for a systolic array for the single-source shortest path problem. The recurrence relation in single-source shortest path problem can be represented as single assignment form by introducing an iteration dimension k :

For k from 1 to N-1, where N is the number of vertices
  For i, j from 1 to N
    $d(i+1,j,k)=d(i,j,k)$ if $j \in W_{i+1}$, $i \geq 1$
    $d(i+1,j,k)=\min\{d(i,j,k), d(i,v(i),k)+w(v(i),j,k)\}$
      if $j \notin W_{i+1}$, $i \geq 1$, where j denotes vertex in graph G

The cubic DG for the case N=8 is shown in Fig.3. In DG, we find that there exists a directed path of length 8N along the bold-face arcs. Dependence arcs between constant k planes are not shown for simplicity.

The DG obtained above can now be safely projected in the k = (0, 0, 1) direction. The signal flow graph, SFG, generated by the k projection is shown in Fig.4 for the case N=8. The array uses N^2 processing elements, PEs, and each PE performs same operation. All dependence arcs except input arcs have unit delay.

In general, it is possible to map an M-dimensional SFG directly onto an $(M-r)$-dimensional SFG (r = $1,2,\ldots, M-1$) by a scheme called multiprojection method [7]. The spatial complexity of the initial SFG can be reduced by multiprojection. The systolic array obtained through the projection in the i and k directions is shown in Fig.5. The array uses N PEs and the data pipeline period of the array is N unit delays.

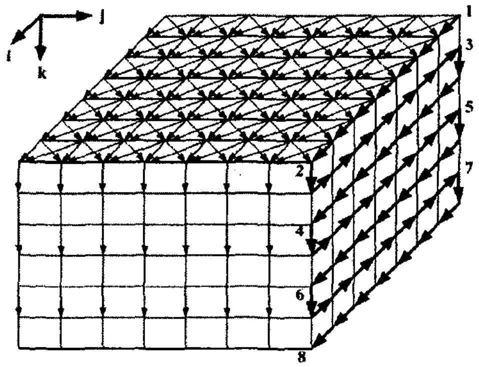

Fig. 3. DG for the case N=8

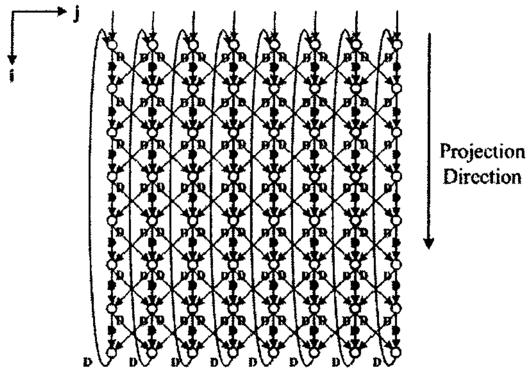

Fig. 4. SFG in *ij*-plane by projection along *k* direction

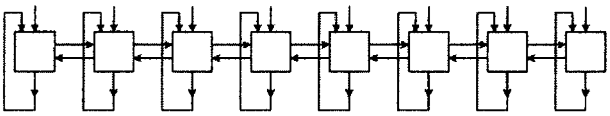

Fig. 5. Systolic array by multiprojection along *i, k* directions

4. Simulation, Synthesis, and Implementation

A systolic array derived for the single-source shortest path problem was modeled and simulated in RTL level using VHDL, and synthesized to a schematic using Synopsys design compiler [3], [8]. The simulation result which is the solution of given sample problem is shown in Fig. 8. The infinity, ∞, is assigned a value of 20. The table for $d(i,v)$ is represented in Fig. 6, Fig.7, and Fig. 8.

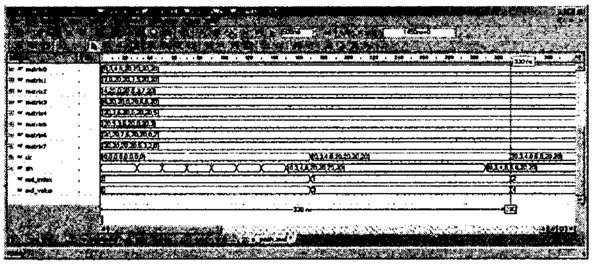

Fig. 6. Simulation showing first two rows of $d(i,v)$ table

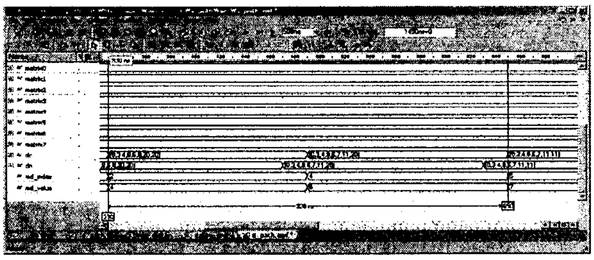

Fig. 7. Simulation showing next two rows of $d(i,v)$ table

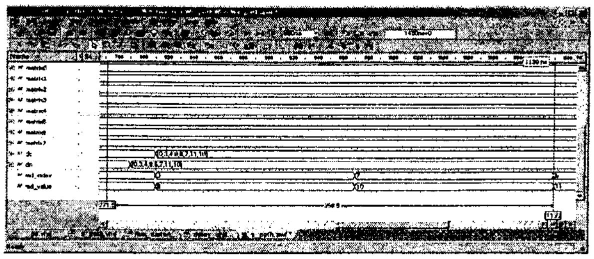

Fig. 7. Simulation showing final four rows of $d(i,v)$ table

Synthesized schematic using Synopsys design compiler for the systolic array for the single-source shortest path problem, SA-SSSP, is shown in Fig. 9. Schematic showing communication between PEs of the systolic array is shown in Fig. 10.

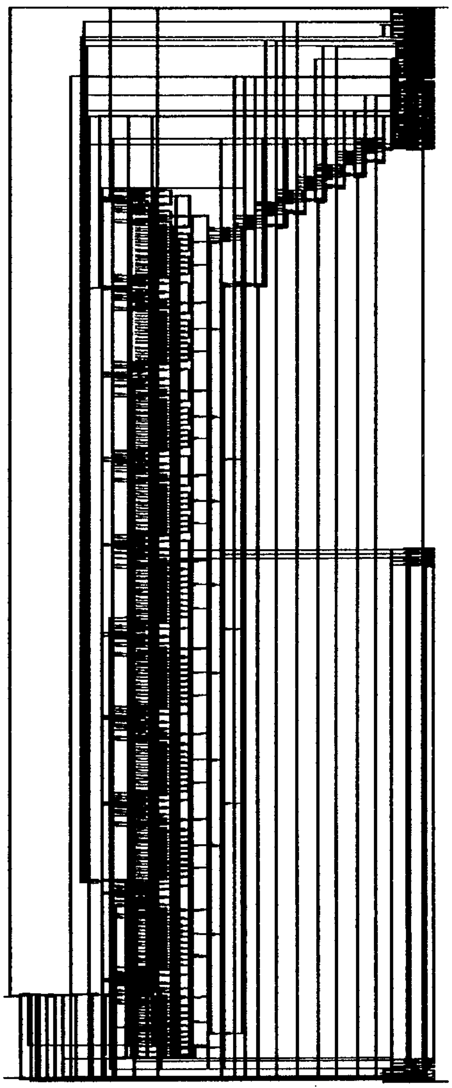

Fig. 9. Synthesized schematic for the SA-SSSP

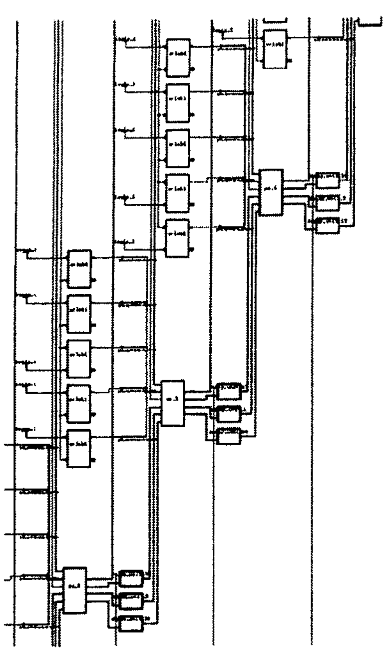

Fig. 10. Schematic for communication between PEs

After being synthesized, a systolic array for the single-source shortest path problem is implemented automatically to a layout using Apollo tool provided by AVANT!. Used cell library is based on 0.35 μm CMOS 1-poly 4-metal CMOS technology. The layout for the schematic, SA-SSSP is shown in Fig. 11.

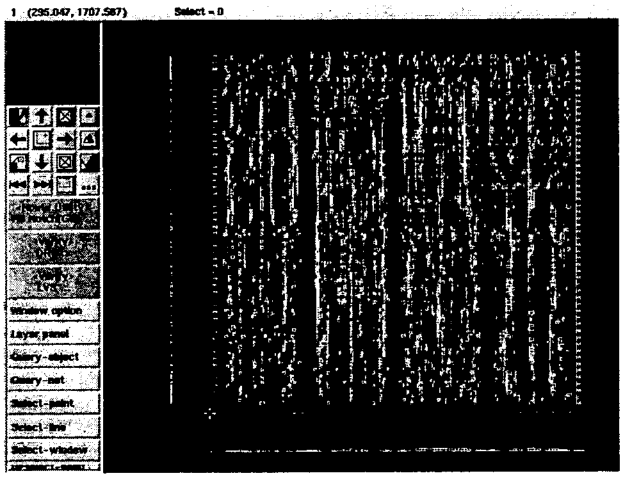

Fig. 11. Layout of SA-SSSP

4. Conclusions

In this paper, we derived a systolic array for single-source shortest path problem. Initial SFG generated by projection in the k direction required N^2 PEs. To reduce the spatial complexity of the systolic array, multiporjection method was used. By this scheme, we could construct a efficient systolic array having N PEs. The derived systolic array through the multiprojection was modeled and simulated in RTL level using VHDL, then synthesized and implemented to a layout.

Single-source shortest path problem is a particular instance of the dynamic programming problem. Next research topic is toward the design of a generalized systolic array that can be applied to any instance of the dynamic programming problem.

References

[1] V.Kumar, A.Grama, A.Gupta, and G.Karypis, *Int. to Parallel Computing-Design and Analysis of Algorithms*, The Benjamin/Cummings Publishing Company, Inc., 1994.

[2] H.T.Kung, "Why Systolic Architectures?", *Computer* Vol.15, No.1, pp.37-46, January 1982.

[3] K.C. Chang, *Digital Systems Design with VHDL and Synthesis*, IEEE Computer Society Press, 1999.

[4] Y.C.Hsu, K.F.Tsai, J.T.Liu and E.S.Lin, *VHDL Modeling for Digital Design Synthesis*, Kluwer Academic Publishers, 1995.

[5] Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, *Intorduction to Algorithms*, McGraw-Hill, 1991.

[6] D.R.Stinson, *An Intorduction to the Design and Analysis of Algorithms*, The Charles Babbage Research Centre, 1987.

[7] S.Y.Kung, *VLSI Array Processors*, Prentice Hall, 1988.

[8] Weng Fook Lee, *VHDL Coding and Logic Synthesis with Synopsys*, Academic Press, 2000.