A 1bit Carry Propagate Free Adder/Subtracter VLSI Using Adiabatic Dynamic CMOS Logic Circuit Technology

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Abstract — This paper describes a design of a 1bit Carry Propagate Free Adder/Subtracter (CPFA/S) VLSI using the Adiabatic Dynamic CMOS Logic (ADCL) circuit technology. Using a PSPICE simulator, energy dissipation of the ADCL 1bit CPFA/S is compared with that of the CMOS 1bit CPFA/S. As a result, energy dissipation of the proposed ADCL circuits is about 1/23 as low as that of the CMOS circuits. The transistors count, propagation-delay time and energy dissipation of the ADCL 4bit CPFA/S are compared with those of the ADCL 4bit Carry Propagate Adder/Subtracter (CPA/S). The transistors count and propagation-delay time are found to be reduced by 7.02% and 57.1%, respectively. Also, energy dissipation is found to be reduced by 78.4%.

Circuit operation and performance are evaluated using a chain of the ADCL 1bit CPFA/S fabricated in a 1.2μm CMOS process. The experimental results show that addition and subtraction are operated with clock frequencies up to about 1MHz.

1. Introduction

Demands for low power and low noise digital circuits have motivated VLSI designers to explore new approaches to the design of VLSI circuits. The Adiabatic (Energy-recovering) logic is a new promising approach, which has been originally developed for low power digital circuits [1]–[3]. In particular, the Adiabatic Dynamic CMOS Logic circuit (ADCL) [3] achieves ultra low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their capacitors. It is known that output voltage of the ADCL gates is supposed to synchronize with the charge of the power supply voltage. As a result, the operating speed of the ADCL circuit gradually becomes low, with the number of gate stages increased. Especially, this problem appears in the ADCL circuit using the Carry Propagate Adder/Subtracter (CPA/S).

On the other hand, the Redundant Binary (RB) number system has the trait of the Carry Propagate Free Adder/Subtracter (CPFA/S) [4]. Because the operations of the RB system consist of the iterative and successive additions and subtractions, they are applied to the complicated arithmetic multiplier units included in the FIR Hilbert Transformer [5].

In this paper, first, we propose a CPFA/S using the ADCL circuit technology. Secondly, we show the simulation results concerned with the 1bit CPFA/S and 4bit CPFA/S realized by using the ADCL and the CMOS logic. Finally, we verify that carrying out design, trial manufacture and evaluation using the ADCL circuit actually, in respect of the CPFA/S integrated circuit ensures the effectiveness of ADCL circuit technique.

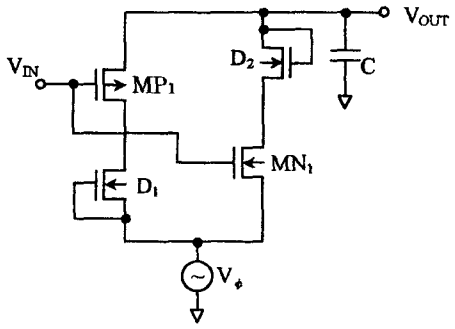


Figure 1. ADCL inverter gate (ADCL–NOT).

Table 1. Propagation-delay time of ADCL circiut.

Logic name	Propagation-delay time
ADCL–NOT	$1\Delta_\phi$
2input ADCL–NAND	$1\Delta_\phi$
2input ADCL–NOR	$1\Delta_\phi$
2input ADCL–ExNOR	$3\Delta_\phi$

2. Basic logic using ADCL circuit

An ADCL inverter gate (ADCL–NOT) is shown in Fig.1. In this circuit, since the output voltage V_{OUT} of the ADCL gate synchronizes with the power supply voltage V_ϕ, the operating speed of the ADCL circuits is determined by the frequency of V_ϕ. The output voltage V_{OUT} is delayed by 0.5 period of the power supply voltage V_ϕ in the ADCL circuit. Therefore, the propagation-delay time unit Δ_ϕ for the ADCL circuit is defined as

$$\Delta_\phi = \frac{1}{2}T_\phi \qquad (1)$$

where T_ϕ is the period of the power supply voltage. As a result, an ADCL–NOT has propagation-delay time of $1\Delta_\phi$. The other propagation-delay time of the ADCL circuits are summarised in Table 1.

3. Carry propagate free adder/subtracter

3.1. Redundant binary representation

The RB representation used in this paper is one of the Signed-Digit (SD) representation proposed by Avizienis [4]. It has a fixed radix-2 and a digit set $\{\bar{1},0,1\}$ where $\bar{1}$ denotes -1. The radix-2 SD code representation of a fractional number X has the general form:

$$X = \sum_{k=0}^{N-1} x_k 2^k \tag{2}$$

where $x_k \in \{\bar{1}, 0, 1\}$. N is the number of ternary digits. The RB representation allows the existence of redundancy. For example, integral number " -3" is expressed as:

$$\begin{aligned} [-3]_{10} &= [0\,0\,\bar{1}\,\bar{1}]_{SD} \\ &= [0\,\bar{1}\,0\,1]_{SD} \\ &= [0\,\bar{1}\,1\,\bar{1}]_{SD} \\ &= [\bar{1}\,1\,0\,1]_{SD} \\ &= [\bar{1}\,1\,1\,\bar{1}]_{SD} \end{aligned} \tag{3}$$

We can compose the CPFA/S by using the above redundancy.

3.2. Structure of CPFA/S

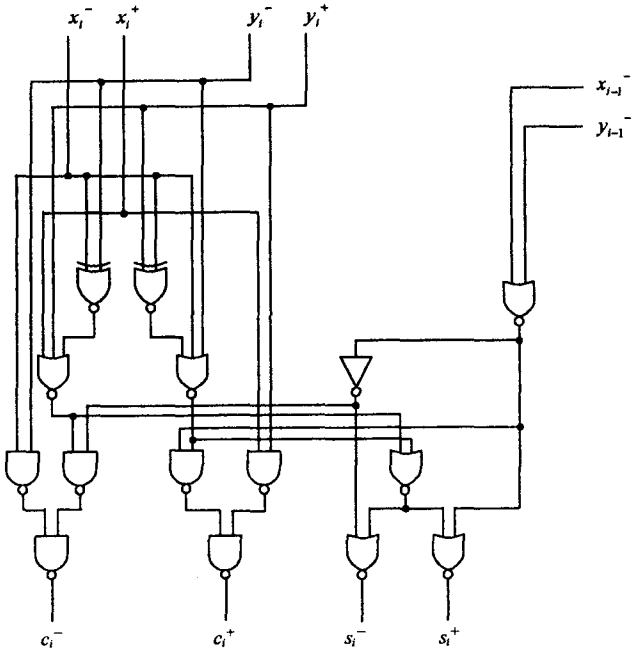
The CPFA/S between two SD number, augend X and addend Y, are performed in i-th place by the following steps:

$$\begin{aligned} \textbf{step1}: \quad x_i + y_i &= 2c_i + s_i \\ \textbf{step2}: \quad z_i &= s_i + c_{i-1} \end{aligned} \tag{4}$$

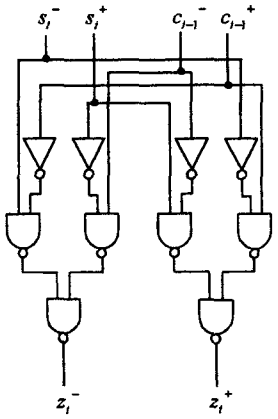
where c_i is intermediate carry, s_i is intermediate sum, z_i is final sum and c_i, s_i, $z_i \in \{\bar{1}, 0, 1\}$. Any arithmetic operation can be defined by a table which contains all possible pairs of digits and by a corresponding table entry which defines the outcome of the operation. In terms of addition, such tables are referred to as *addition tables* and contain all possible combinations of the addend and augend with a corresponding sum digit. Therefore, Eq.(4) can be given as *addition tables*. One of the first binary addition tables is given in [6]. Table 2 is a reproduction of the addition table summarized in [6]. In this table, each sum is represented as s_i and c_i. In the rows (b) and (f), s_i and c_i are determined by the arithmetic

Table 2. Computation addition table.

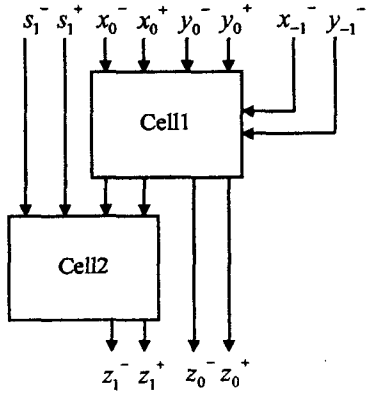
Type	x_i	y_i	x_{i-1}, y_{i-1}	c_i	s_i
(a)	$\bar{1}$	$\bar{1}$	——	$\bar{1}$	0
(b)	0	$\bar{1}$	Both are non-negative.	0	$\bar{1}$
	$\bar{1}$	0	Otherwise	$\bar{1}$	1
(c)	1	$\bar{1}$	——	0	0
(d)	$\bar{1}$	1	——	0	0
(e)	0	0	——	0	0
(f)	0	1	Otherwise	0	1
	1	0	Both are non-negative.	1	$\bar{1}$
(g)	1	1	——	1	0



(a) Intermediate carry logic (Cell1).

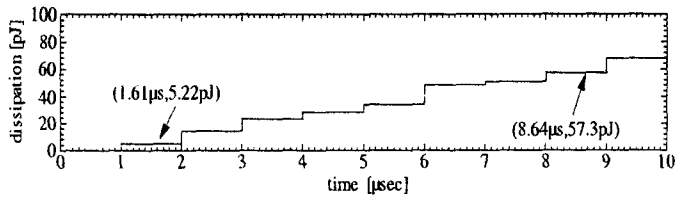


(b) Intermediate sum logic (Cell2).

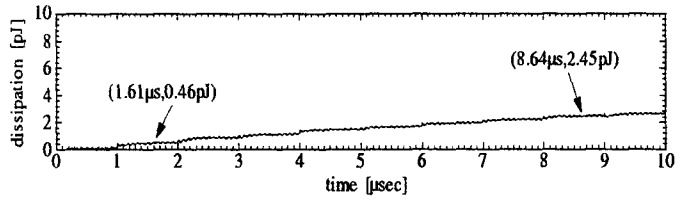


(c) 1bit CPFA/S.

Figure 2. CPFA/S building block.



(a) CMOS 1bit CPFA/S.



(b) ADCL 1bit CPFA/S.

Figure 3. Energy dissipation for PSPICE simulation.

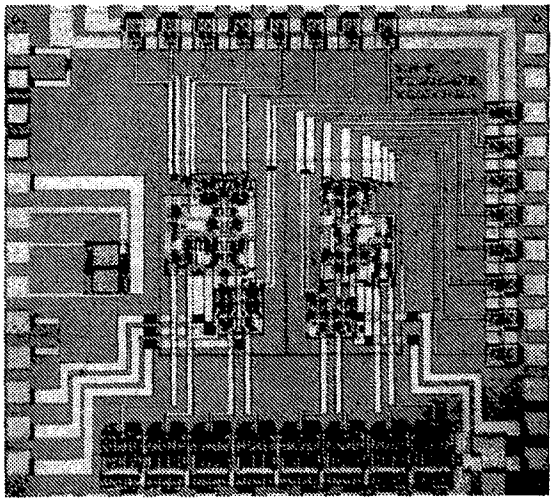


Figure 4. Photomicrograph of 1bit adder/subtracter chip.

signs of x_{i-1} and y_{i-1}. These two digits are part of the intermediate values combined with a guarantee of no ripple in the final stage. In this way, the final step of combining the intermediate carry with sum digits to form a final sum can be accomplished with a guarantee that no carry ripples will occur.

Figure 2 shows the 1bit CPFA/S building block. The Cell1 and Cell2 generate intermediate carry and intermediate sum, respectively. The adder/subtracter of arbitrary length can be realized by using parallel connection of the block diagram shown in Fig.2 (c). The CPFA/S always ensures constant propagation-delay time. In this case, maximum propagation-delay time of the CPFA/S using the ADCL circuits is less than $9\Delta_\phi$.

4. PSPICE simulation results

4.1. Energy dissipation of 1bit CPFA/S

Figure 3 shows the comparison of energy dissipation of the CMOS 1bit CPFA/S and the ADCL 1bit CPFA/S. The conditions of PSPICE simulator are following:

supply voltage V_{dd} : 5V, DC
supply voltage V_ϕ : 5V, 10MHz, sine wave
clock frequency f : 5V, 500kHz, square wave

From this result, we find that the energy dissipation of the ADCL 1bit CPFA/S is about $1/23$ as low as that of the CMOS 1bit CPFA/S.

Table 3. Comparision for 4bit CPA/S [7] and 4bit CPFA/S

	Transistors count	Maximum propagation -delay time	Energy dissipation
4bit CPA/S	684	$21\Delta_\phi$	119 pJ
4bit CPFA/S	636	$9\Delta_\phi$	25.7 pJ
Reduction %	**7.02%**	**57.1%**	**78.4%**

4.2. Comparison for 4bit CPA/S and 4bit CPFA/S

In [7], the ADCL 4bit CPA/S is designed to implement a 2's complement adder/subtracter. Since the ADCL 4bit CPA/S has long propagation-delay time, the clock speed is the main problem. On the other hand, the CPFA/S has a certain propagation-delay time. Table 3 summarizes transistors count, maximum propagation-delay time and energy dissipation of the 4bit CPA/S and the 4bit CPFA/S. From this table, it is found that CPFA/S is superior to CPA/S in all parameters. Therefore, it can be concluded that the "ADCL Adder/Subtracter" is suitable for realizing the "CPFA/S."

5. 1bit CPFA/S VLSI fabrication of ADCL technology

The 1bit CPFA/S VLSI using the ADCL circuit was fabricated using a $1.2\mu m$ CMOS process. This chip size is $2.3\text{mm} \times 2.3\text{mm}$. The transistor size W/L is $5.0\mu\text{m}/1.2\mu\text{m}$ for both of the p-channel and the n-channel transistors. The element value of the ADCL load capacitor to hold the output voltage is 0.05pF. In the input and the output interfaces, the conventional CMOS circuits are used in order to realize the CMOS interface compatibility. Therefore, these interface circuits are non-adiabatic. Figure 4 shows the photomicrograph of the ADCL 1bit CPFA/S chip. This ADCL 1bit CPFA/S area without the test vector part is $370\mu\text{m} \times 740\mu\text{m}$.

Figures 5 and 6 show the results of PSPICE simulation for 1+1 mode and the results of measurement for 1+1 mode, respectively. This measurement conditions are following:

supply voltage V_{dd} : 5V, DC
supply voltage V_ϕ : 5V, 10MHz, sine wave
clock frequency f : 5V, 1MHz, square wave

In Figs.5 and 6, we find that the 1bit ADCL CFPA/S is operating correctly with clock frequencies up to about 1MHz.

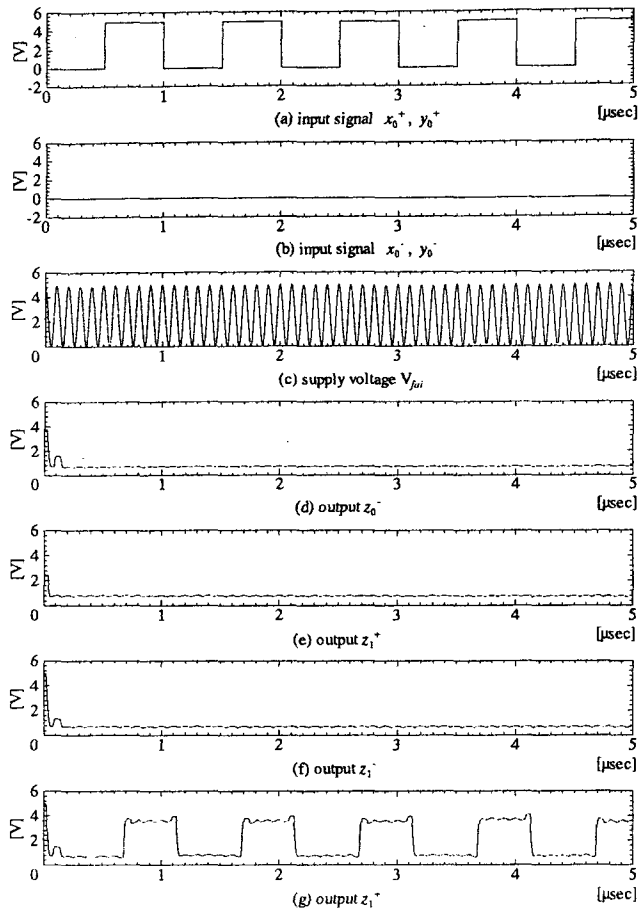


Figure 5. Results of PSPICE simulation (1 + 1 mode).

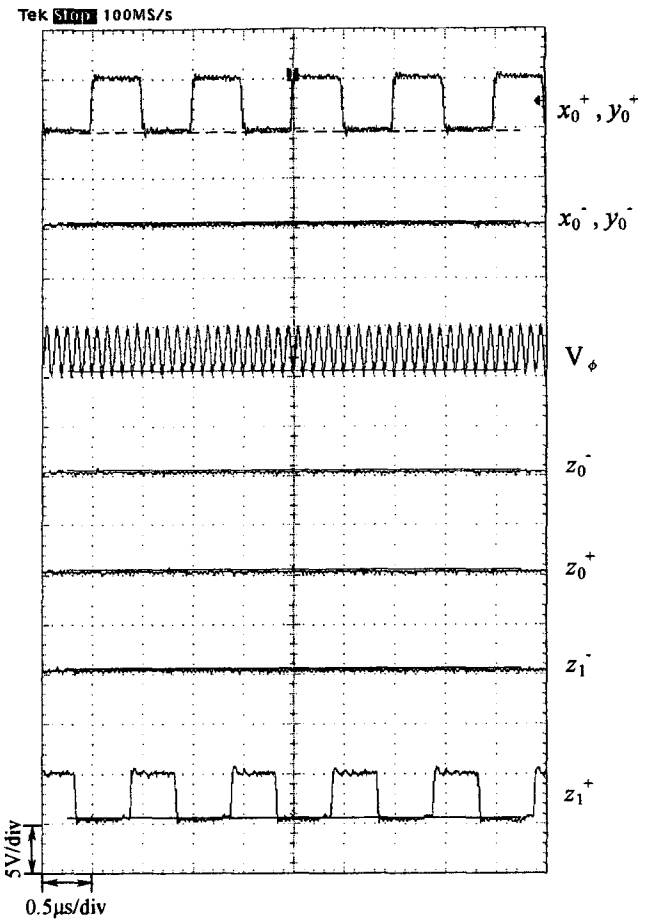


Figure 6. Results of measurement (1 + 1 mode).

6. Conclusion

In this paper, the Carry Propagate Free Adder/Subtracter (CPFA/S) scheme using ADCL technology is presented. The PSPICE simulation shows that energy dissipation of the ADCL 1bit CPFA/S is about 1/23 as low as that of the CMOS 1bit CPFA/S. And maximum propagation-delay time for the CPFA/S is found to be $9\Delta_\phi$. The ADCL 1bit CPFA/S is implemented by using a 1.2μm CMOS process technology with the area of $370\mu\text{m} \times 740\mu\text{m}$. The experimental results show that addition and subtraction are operated with clock frequencies up to about 1MHz.

Acknowledgment

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