

# Gain Controllable ADC using Two-Stage Resistor String for CMOS Image Sensor

\*Ju Young No, \*Jin Han Yoon, \*\*Soo Yang Park, \*\*Yong Park, \*\*\*Sang Hee Son

\*School of Information Communication Eng. Chong-ju University  
36 Naedok-dong, Sang Dang Gu, Chongju-shi, Republic of Korea  
E-mail : jyno@chongju.ac.kr

\*\*Cevit I.S.

305 East IT Venture Tower, 78 Garakbon-dong, Songpa-gu, Seoul, 138-803, Republic of Korea  
Tel. : +82-2-574-5781 Fax. : +82-2-571-3422

\*\*\*School of Information Communication Eng. Chong-ju University  
36 Naedok-dong, Sang Dang Gu, Chongju-shi, Republic of Korea  
Tel : +82-43-229-8464, Fax : +82-43-229-8461  
E-mail : shson@chongju.ac.kr

**Abstract** : This paper is proposed a 8-bit analog to digital converter for CMOS image sensor. A analog to digital converter for CMOS image sensor is required function to control gain. Frequency divider is used to control gain in this proposed analog to digital converter . At 3.3 Volt power supply, total static power dissipation is 8mW and programmable gain control range is 30dB. Newly suggested analog to digital converter is designed by 0.35um 2-poly 4-metal CMOS technology.

## 1. Introduction

Recently, growth in the market for multimedia systems has generated an increasing demand for image sensor systems that are able to directly import both video and photographic images into personal computers. Currently, such image sensor systems are usually implemented using charge-coupled device(CCD) technology [1][2]. However, as the products of multimedia system are recently required portability, low cost and low

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power, CCD technology is not adequate for system integration because of its specific technology. To overcome the limitations of CCD technology, it must be fabricated with standard CMOS technology to integrate circuits. By reason of the limitations of CCD technology, recently CMOS image sensor has been implemented for a number of applications [2]. Conventional CMOS image sensor (Fig. 1.) consists of pixel array, analog to digital converter, digital control circuit and timing controller interface etc.

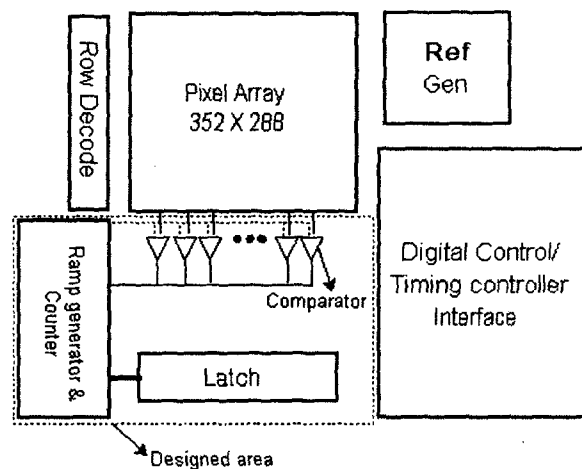


Fig. 1. Conventional CMOS image sensor scheme

At Fig. 1, line box area is analog to digital converter to be designed in this paper [3][4].

Color of images are appeared with light primary color (red, blue and green). To appear color in image, red, blue and green filter are covered on pixel array. Light to pass through the filters is characterized by a difference of amplitude (Fig. 2.). These amplitudes must be fixed. In dark place, image signals have small digital values. When small digital values are converted to analog values, such analog values are difficult to make a distinction. By reason of this, small analog values must be amplified. Because of such two reason, image signals are needed to control gain [5].

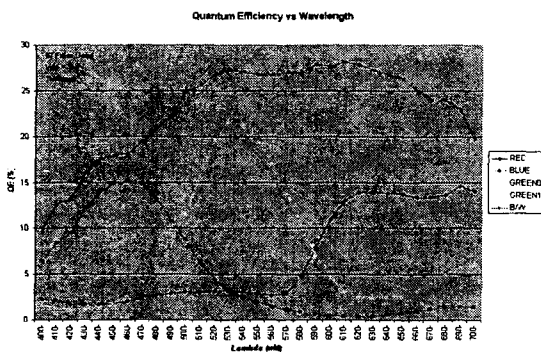


Fig. 2. Filters characterization of light

## 2. Proposed new gain control method

Previous gain control method is controlling the changing of slope (Fig. 3.).

For example, if the gain is increased two times, a slope is decreased a half of slope value. To change slope, if  $\Delta V$  decrease a half, slope is changed. So that, gain is increased two times. Like shown in Fig. 3, during  $\Delta V$ , master clock is counted one time, but if the slope is decreased a half, master clock is counted two times during  $\Delta V$ . Because of the reason, output digital values are increased.

Proposed gain control method in this paper is changing the slope, too. The difference is not  $\Delta V$  changing but  $\Delta t$  changing (Fig. 4.). For

example, if time interval is increased to  $2\Delta t$ , slope is changed to a half. During  $\Delta t$ , master clock is counted one time. But, during  $2\Delta t$ , master clock is counted two times and so gain is increased two times. In this paper, to change the time interval  $\Delta t$  to  $2\Delta t$ , frequency\_divider is used.

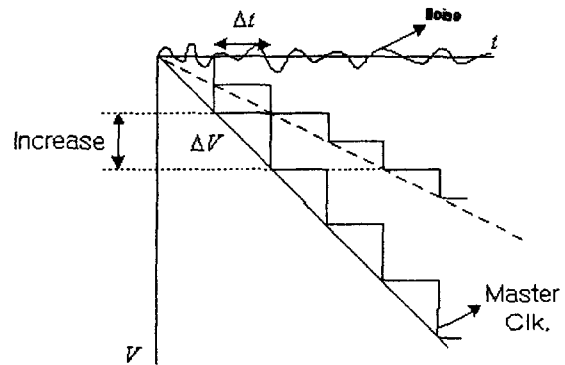


Fig. 3. Previous gain control method

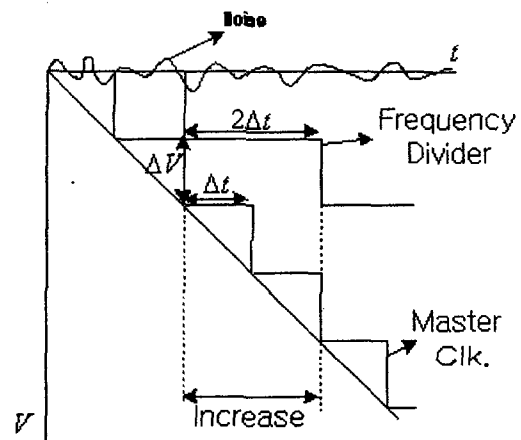


Fig. 4. Proposed gain control method

## 3. Proposed new ramp generator

For counting signal, ramp signal generator is needed. In this paper, ramp generator is made with resistor. Generally, ramp generator is consist of 256 resistors to achieve 8-bit digital code. However, to decrease a number of resistor, two-stage resistor string (Fig. 5.) are utilized. The architecture of two-stage resistor string is like to multistage resistor architecture of digital

to analog converter (DAC). Resistor strings consist of coarse-stage and fine-stage. Coarse-stage that widely generate ramp signal consists of 16 resistor. Fine-stage that narrowly divide coarse-stage ramp signal consists of 16 resistor, too. Therefore, it is gotten 16 ramp signals in fine-stage per 1 ramp signal in coarse-stage. Therefore, it is gotten 256 ramp signals of 8-bit. In ramp signal generator, the sum of resistor that is made of two-stage resistor string architecture is 32.

In this paper, proposed ADC scheme is shown in Fig. 6.

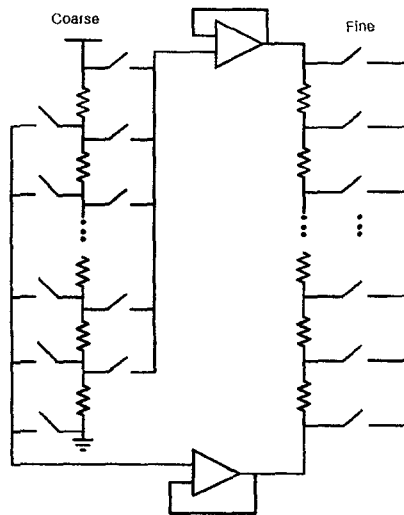


Fig. 5. Proposed two-stage resistor string RAMP generator

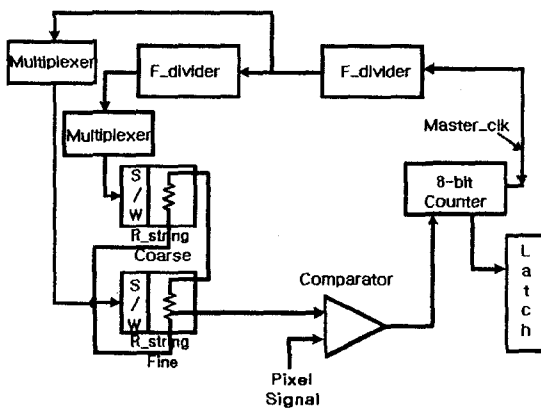


Fig. 6. Proposed ADC scheme

## 4. Simulation Results

Comparator output and ramp signal output, according to input signal, are shown in Fig. 7.

Let's count clock numbers in Fig. 7. So comparator output signal is passing the 7th coarse ramp (Fig. 7.) and passing the 1st fine ramp in the 7th coarse ramp (see Fig. 8., Fig.8 magnify the part of Fig. 7). So total numbers of fine ramp signal are  $97(6 \times 16 + 1)$ . Therefore, clock numbers are 97.

Counter output values are shown in Fig. 9. In Fig. 9., the most upper is LSB value and the most lower is comparator output. If this binary values are changed to decimal value, it is same as below ;  $2^0 + 2^5 + 2^6 = 1 + 32 + 64 = 97$ . We know that the counter output values are the same as ramp clock numbers.

Proposed gain controllable ADC using a  $0.35\mu\text{m}$  2-poly 4-metal CMOS technology was simulated using HSPICE.

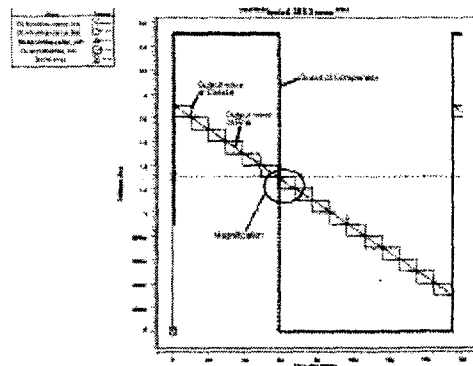


Fig. 7. Comparator & ramp generator output vs input signal

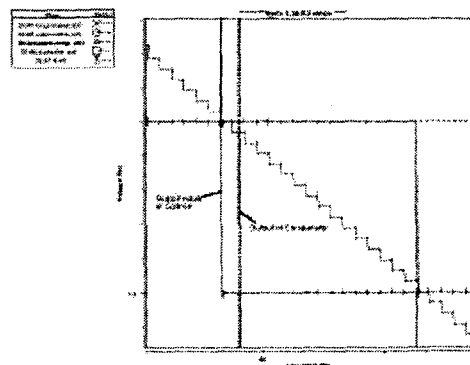


Fig. 8. Part magnification of Fig. 7.

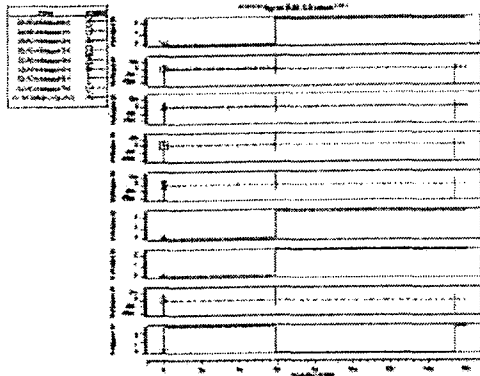


Fig. 9. Counter output results

### 5. Conclusion

The newly gain controllable 8-bit ADC using two-stage resistor string for CMOS image sensor is proposed and designed. At 3.3 Volt power supply, total static power dissipation is 8mW and programmable gain control range is 30dB. The gain control range can be easily increased with insertion of additional flip-flop at divided-by-N frequency divider. Using two-stage resistor string, resistor numbers are decreased.

Table 1. Simulation result

Power supply	3.3V
Power consumption	8mW
Operating Frequency	16MHz
Gain control range	30dB
Resolution	8-bit

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