A Phase Compensation for a Low Power Operational Trans-Conductance Amplifier

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Abstract: This paper describes a phase compensation technique for the low power consumption OTA. Power consumption of the low power OTA is lower than that of the conventional Wang's OTA. However, this circuit has an oscillation problem. The phase margin is -24deg. By using the phase compensation capacitor, the phase margin becomes 52deg. As a result, the low power consumption OTA circuit becomes to have an enough phase margin and to operate stably.

1. Introduction

With the development of the LSI technology, more improvement of the performance of analog circuits and higher integration of digital circuits have been required. It is expected that, in next generation of LSI, a large scale of analog circuit is integrated on the same digital LSI chip. In such flow, the following are required also in the analog circuit as well as digital circuit: Miniaturization, voltage lowering and little power consumerization. Operational Trans-conductance Amplifier (OTA) circuit is one of the most important analog circuits for analog LSI.

Though the conventional Wang's OTA[1] has the wide linear input voltage range, power consumption of this circuit becomes high. In Ref.[2], a low power consumption OTA circuit which overcomes this shortcoming has been proposed. In this paper, we call this OTA a low power OTA. In this circuit, power consumption is reduced by dynamically controlling the tail current using the minimum current selecting circuit without narrowing the linear input voltage range. The minimum current selecting circuit is realized by adopting a negative feedback. As described in the above, power consumption of the low power OTA is lower than that of the conventional Wang's OTA. However, this circuit has an oscillation problem which results from the negative feedback loop. Therefore, this paper proposes a technique which uses a small capacitance in order to obtain a sufficient phase margin of the low power OTA.

2. Wang's OTA Circuit

Figure 1 shows the Wang's OTA circuit. Let's assume that MOS transistors of the equal size are used for MN1 to MN4 and all of these transistors are in the saturation region. If channel length modulation effect is neglected, drain currents I_{D1}, I_{D2}, I_{D3} and I_{D4} are expressed as simple equations (1) to (4) by gradual channel approximation.

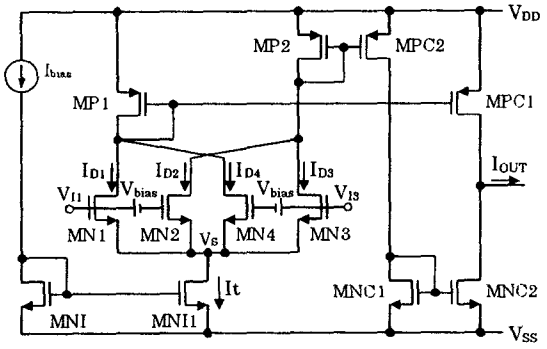


Fig.1. Wang's OTA circuit

$$I_{D1} = K\left(V_{IN1} - V_S - V_T\right)^2 \quad (1)$$

$$I_{D2} = K\left(V_{IN1} - V_{bias} - V_S - V_T\right)^2 \quad (2)$$

$$I_{D3} = K\left(V_{IN2} - V_S - V_T\right)^2 \quad (3)$$

$$I_{D4} = K\left(V_{IN2} - V_{bias} - V_S - V_T\right)^2 \quad (4)$$

Current $I_{D1}+I_{D2}$ which flows MP1 is copied to MPC2 by a current Miller circuit composed of MOS transistors of the equal size. Current $I_{D3}+I_{D4}$ which flows MP2 is also copied to MNC2. Finally it results in output current I_{out}. Thus, Eq.(5) is easily obtained, where $V_{IN} = V_{I1}+V_{I3}$.

$$\begin{aligned} I_{OUT} &= I_{D1} + I_{D4} - \left(I_{D2} + I_{D3}\right) \\ &= 2K \cdot V_{bias} \cdot V_{IN} \end{aligned} \quad (5)$$

From Eq.(5), trans-conductance g_m is obtained as

$$g_m = \frac{\partial I_{out1}}{\partial V_{IN}} = 2K \cdot V_{bias} \quad (6)$$

From Eq.(6), it is known that the trans-conductance g_m can be controlled by V_{bias}.

Next, the linear input voltage range of the Wang's OTA circuit is considered. It is necessary to satisfy next condition, because all transistors from MNI to MN4 must operate in the saturation region.

$$\begin{aligned} &V_{DSn} \geq V_{DSn} - V_T > 0 \\ &(n = 1 \text{ to } 4,\ V_T = V_{Tn}) \end{aligned} \quad (7)$$

The deviation from the linear operation range is on the transition point of either MN2 or MN4 to the cut off region as known from the circuit structure of Fig.1. Next equations are established on MN4 transition point to cutoff region.

$$V_S = V_{I3} - V_{bias} - V_T \quad (8)$$

$$I_{D4} = I_T - (I_{D1} + I_{D2} + I_{D3}) = 0 \quad (9)$$

From these equations, the following equation is obtained.

$$V_{IN} = \sqrt{\frac{It}{2K} - \frac{3}{4}V_{bias}^2} - \frac{V_{bias}}{2} \quad (10)$$

In the same way, the equation on MN2 is derived. However, the sign of V_{IN} is inverted this time. Therefore, linear input voltage operating range of the circuit can be expressed as the following equation.

$$|V_{IN}| \leqq \sqrt{\frac{It}{2K} - \frac{3}{4}V_{bias}^2} - \frac{V_{bias}}{2} \quad (11)$$

From Eq.(11), input voltage linear operating range depends on tail current I_t. It means that power consumption of the circuit also increases, if input voltage linear operating range is increased.

3 Tail current control circuit

In Fig.2, the proposed low power consumption OTA circuit is illustrated. This circuit contains a newly designed tail current control circuit surrounded by broken lines. The tail current control circuit consists of two current selection circuits ① and ②, and a current miller circuit ③ for summing output signals from the current selection circuits ① and ②.

In the circuit ①, I_{D1} and I_{D2} flow through MPM1 and MPM2, respectively. Moreover I_{bias} flows through MNM2. The size of all transistors is equal and all transistors operate in the saturation region. If $I_{D1} + I_{D2} < I_{bias}$, the current I_{MPM5} which flows through MPM5 is expressed by the following equation.

$$I_{MPM5} = I_{bias} - (I_{D1} + I_{D2}); (I_{D1} + I_{D2} < I_{bias}) \quad (12)$$

On the other hand, if $I_{D1} + I_{D2} > I_{bias}$,

$$I_{MPM5} = 0 \; ; (I_{D1} + I_{D2} > I_{bias}) \quad (13)$$

Another current selection circuit ② also similarly operates for input current $I_{D3}+I_{D4}$, because it bas the equal circuit structure. These currents are summed up in the ADDER circuit ③ and if I_{bias} is set at the intersection point of $I_{D1} + I_{D2}$ and $I_{D3} + I_{D4}$,

$$I_{bias} = I_{D1} + I_{D2} = I_{D3} + I_{D4} \quad (14)$$

The output current I_a of the tail current control circuit is expressed by Eqs. (15) and (16). Namely, the input currents $I_{D1} + I_{D2}$ and $I_{D3} + I_{D4}$ are compared to each other, and the smaller one is selected before the operation of I_{bias} minus the smaller one is executed.

If $I_{D1} + I_{D2} < I_{D3} + I_{D4}$,

$$I_a = I_{bias} - (I_{D1} + I_{D2}) \quad (15)$$

If $I_{D1} + I_{D2} > I_{D3} + I_{D4}$,

$$I_a = I_{bias} - (I_{D3} + I_{D4}) \quad (16)$$

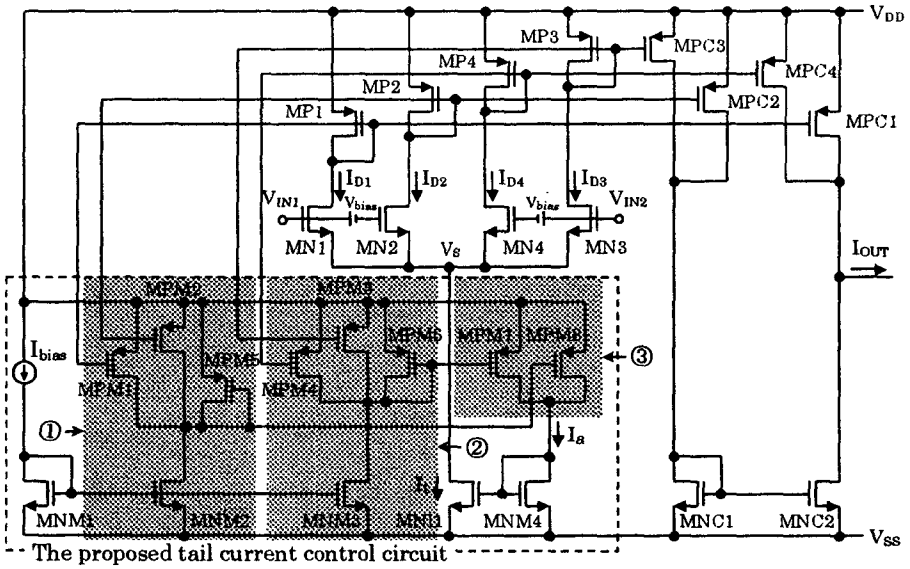


Fig.2. Low power consumption OTA circuit

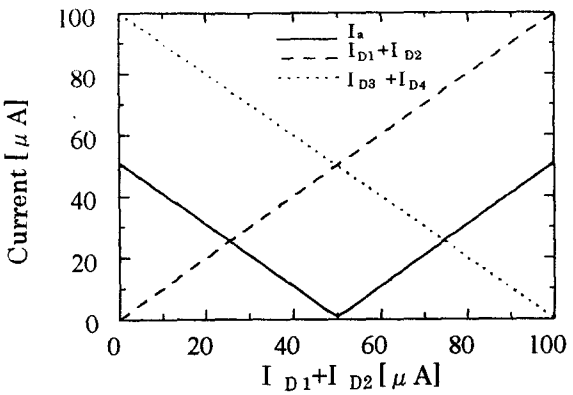


Fig.3. Input-Output current characteristic of the proposed tail current control circuit

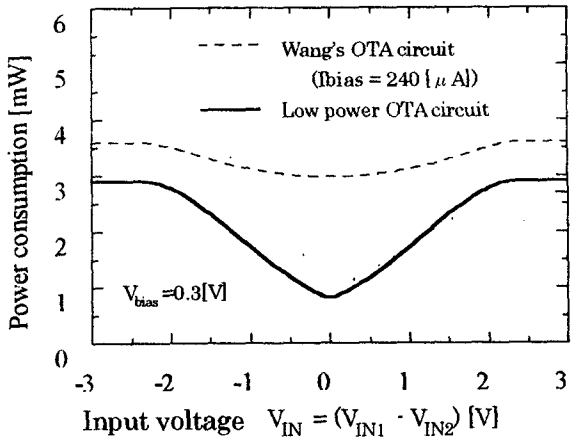
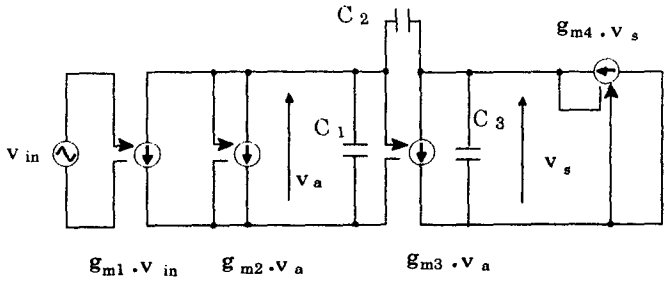


Fig.4. Power consumption

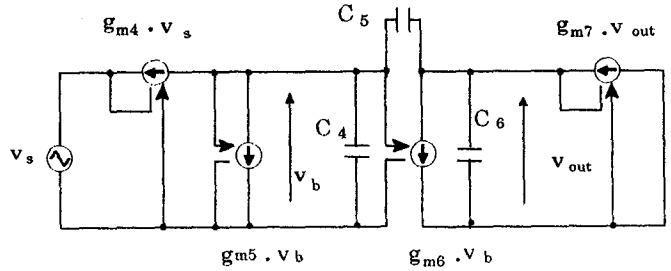
Figure 3 shows the above operation. In Fig.4, power comparison between 2 OTA circuits is shown. This result was obtained through computer simulation. From Fig.4, it is found that power consumption of the proposed OTA circuit is lower than the conventional one. At the stand-by mode, power consumption of the proposed circuit is 28% as low as the conventional one. The input voltage linear dynamic range is also confirmed to be from -2.8 volts to 2.8 volts by computer simulation, which is the same as the conventional OTA's.

4 Phase compensation of low power OTA

The minimum current selecting circuit is realized by adopting a negative feedback. As described in the above, power consumption of the low power OTA is lower than that of the conventional Wang's OTA. However, this circuit has the oscillation problem which results from the negative feedback loop. This problem is confirmed through both of computer simulation and experiment. In order to obtain a sufficient phase margin, we use a phase compensation capacitor. Generally, in the integrated circuits, it is undesirable to use large capacitance because of its large area. Therefore, this paper proposes a technique which uses a small capacitance in order to obtain a sufficient phase margin in the low power OTA.



(a) Equivalent circuit : from v_{in} to v_s



(b)Equivalent circuit : from v_s to v_{out}

Fig.5 A small signal equivalent circuit of the low power OTA

A small signal equivalent circuit of the low power OTA is analytically examined. Figure 5 shows the small signal equivalent circuit of the low power OTA. The device parameters included in the circuit are summarized in Tab.1. In this table, the parasitic capacitors are neglected except the gate-source capacitors and some of the gate-drain capacitors because the gate-source capacitor *Cgs* is the largest capacitor of all the parasitic capacitors when the transistor operates in the saturation region. The gate-source capacitor *Cgd* is a small value, but it cannot be neglected under the Miller effect. In the design step, we should consider the stability problem. Let's consider the open-loop transfer function of the low power OTA.

Table 1 Parameters of the circuit shown in Fig.2

	Transconductance [μA/V]	Cgs [pF]	Cgd[pF]
MPM7 MPM8	gm_1' : 7.0 *($gm_1=2 \cdot gm_1$')	C_6' : 0.045	
MNM4	gm_2 : 11. 5		
MN11	gm_3 : 240. 0	C_1 : 0.48	C_2 : 0.027
MN1 ~ MN4	gm_4 : 15.1	C_3' : 0.022 *($C_3 = 4 \cdot C3$')	
MP1 ~ MP4	gm_5 : 51.7	C_4' : 0.24 *($C_4 = C_4$'+C_4'')	
MPM1 ~ MPM4	gm_6 : 50. 0	C_4'' : 0.24	C_5 : 0.0135
MPM5 MPM6	gm_7 : 6.9	C_6'' : 0.045 *($C_6=C_6$'+C_6'')	

We can obtain transfer function of low power OTA as Eqs.(17), (18) and (19), because we can divide transfer function at *Vs*.

$$G1 = \frac{vs}{vin} \tag{17}$$

$$G2 = \frac{vout}{vs} \tag{18}$$

$$G = \frac{vout}{vin} = G1 \cdot G2 \tag{19}$$

From Fig.5, transfer function of *G1* and *G2* is expressed as

$$G1 = \frac{\frac{gm_1 \cdot gm_3}{gm_2 \cdot 4gm_4}\left(1 - jw\frac{C_2}{gm_3}\right)}{1 + jw\left(\frac{C_2 + 4C_3}{4gm_4} + \frac{C_1 + C_2}{gm_2} + \frac{C_2 \cdot gm_3}{gm_2 \cdot 4gm_4}\right) + (jw)^2 \frac{C_1C_2 + 4C_1C_3 + 4C_2C_3}{gm_2 \cdot 4gm_4}} \tag{20}$$

$$G2 = \frac{-2\frac{gm_4 \cdot gm_6}{gm_5 \cdot gm_7}\left(1 - jw\frac{C_5}{gm_6}\right)}{1 + jw\left(\frac{C_5 + C_6}{gm_7} + \frac{C_4 + C_5}{gm_5} + \frac{C_5 \cdot gm_6}{gm_5 \cdot gm_7}\right) + (jw)^2 \frac{C_4C_5 + C_4C_6 + C_5C_6}{gm_5 \cdot gm_7}} \tag{21}$$

Because $C_1 \gg C_2$, $C_1 \gg C_3$, $C_4 \gg C_5$ and $C_4 \gg C_6$, Eqs.(20) and (21) can be rewritten as

$$G1 \cong \frac{\frac{gm_1 \cdot gm_3}{gm_2 \cdot 4gm_4}\left(1 - jw\frac{C_2}{gm_3}\right)}{\left(1 + jw\frac{C_1}{gm_2}\right)\left(1 + jw\frac{C_3}{4gm_4}\right)} \tag{22}$$

$$G2 \cong \frac{-2 \cdot \frac{gm_4 \cdot gm_6}{gm_5 \cdot gm_7}\left(1 - jw\frac{C_5}{gm_6}\right)}{\left(1 + jw\frac{C_4}{gm_5}\right)\left(1 + jw\frac{C_6}{gm_7}\right)} \tag{23}$$

The low power OTA has four poles and two zeros. The phase margin indicated by the above equation is –24 degrees when we substitute the numerical values summarized in Tab.1 into Eqs.(19), (22) and (23). In this case, the first dominant pole is at 3.8 MHz and the second pole is at 17.1 MHz. Figure 6 shows a bode plot of this circuit. From this figure, we find that this circuit oscillates. In order to solve this problem, the transfer function which includes the phase compensation capacitor in the low power OTA is considered. The proposed technique is based on Miller effect compensation. The phase compensation capacitor 2.0pF is connected between the drain and the source terminals of MNI1. In this case, taking $C_2 \gg C_1$, $C_2 \gg C_3$, $C_4 \gg C_5$ and $C_4 \gg C_6$ into account, the transfer function is given by

$$G1 \cong \frac{\frac{gm_1 \cdot gm_3}{gm_2 \cdot 4gm_4}\left(1 - jw\frac{C_2}{gm_3}\right)}{\left(1 + jw\frac{C_1 + C_3}{gm_2 + gm_3 + 4gm_4}\right)\left(1 + jw\frac{C_2 \cdot gm_3}{gm_2 \cdot 4gm_4}\right)} \tag{24}$$

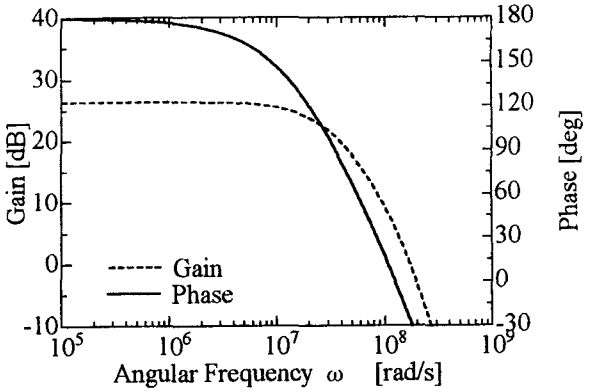


Fig.6 Bode plot : Low Power OTA

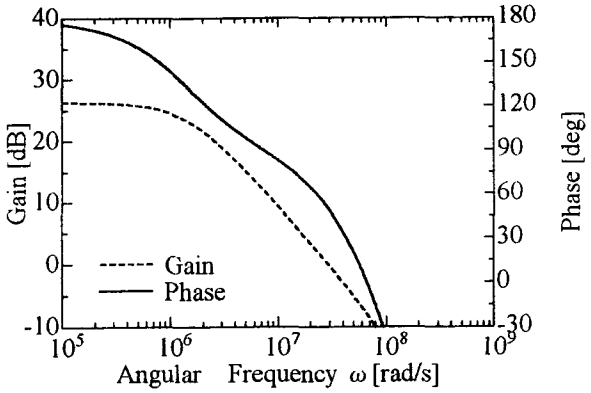


Fig.7 Bode plot : Miller effect compensation

Substituting the numerical values into Eqs.(19), (23) and (24), the phase margin achieved by using the phase compensation capacitor in the low power OTA becomes 52deg. In this case, the dominant pole is at 0.23 MHz and the second pole is at 17.1 MHz. Figure 6 shows a bode plot of this circuit. From this figure, we find that the oscillation problem is solved.

5. Conclusion

The phase compensation technique of the low power OTA is presented. The conventional low power OTA has the possibility of oscillation because stability is not taken into account. The proposed technique removes instability of the low power OTA and becomes useful in using the low power OTA.

References

[1] Z. Wang, "Novel Linearisation Technique For Implementing Large-Signal MOS Tunable Trans-conductor," Electron. Lett., Vol.26, pp.138-139, 1990.

[2] S. Sudo, T. Kitajima and K. Takahashi "A Novel Low Power OTA Circuit with a new Tail Current Control Circuit" Proc. of ITC-CSCC'01, pp.216-219, 2001