Constant-g_m Rail-to-Rail CMOS Multi-Output FTFN

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Abstract: An alternative CMOS implementation of a multi-output four-terminal floating nullor (FTFN) with constant-g_m rail-to-rail input stage is proposed. This presented circuit is based on the advantages of a complementary transconductance amplifier and class AB dual translinear cell circuit that comes up with wide bandwidth. The constant-g_m characteristic is controlled by the maximum-current selection circuits, maintaining the smooth response over the change of input common mode voltage. The circuit performances are confirmed through HSPICE simulations. A current-mode multifunction filter is used to exhibit the potentiality of this proposed scheme.

1. Introduction

Recently, there are many attempts to design a high performance four-terminal floating nullor (FTFN), which has been stood out as a more flexible and versatile than the other building blocks [1-4], especially, in current-mode circuits. This work shows the other choice to achieve an integrable multiple-output port FTFN in CMOS technology, which offers high bandwidth and low-voltage operation. This proposed circuit scheme is the combination of a low-voltage P-N complementary transconductance amplifier, a dual translinear cell and some of current mirrors. The sufferings from transconductance variation and degradation of common mode rejection ratio (CMRR) [5] have been reduced by using the current-selector circuit technique. In addition, the number of output ports can be expanded to support the designer applications. The characteristics of the FTFN are explained by mean of simulation results using HSPICE program. The current-mode multifunction filter is adopted to demonstrate the performance of this proposed circuit.

2. Multi-output FTFN

FTFN is an active device that equivalent to an ideal nullor, which can imply to be a high gain transconductance amplifier with floating characteristic at input and output terminals. Fig. 1(a) shows a nullor model of an FTFN that can be described by its port relation characteristics as:

$$v_Y = v_X \qquad i_Y = i_X = 0 \qquad i_Z = -i_W \qquad (1)$$

One of the most famous realisation techniques is built up from a basic type shown in Fig. 1 (b) [1, 2]. It is using one op-amp and supply current sensing technique, where the output impedance of port W is very low and the impedance of port Z is very high.

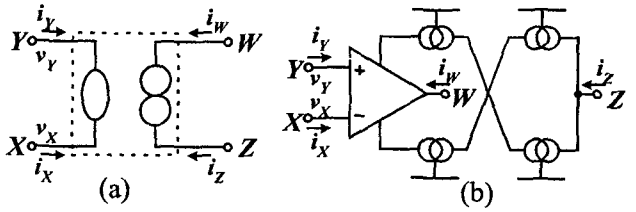


Fig. 1 (a) A nullor model (b) traditional implementation

A modification from the original FTFN to be a multi-output FTFN is done by adding the new output terminals as shown in Fig. 2, where its characteristics can be point out by the following port relations:

$$v_Y = v_X \ , \ i_Y = i_X = 0$$

$$i_{Z1} = i_{Z2} = \cdots = i_{Zn} = -i_{W1} = -i_{W2} = \cdots = -i_{Wn} \qquad (2)$$

where n is number of the output ports.

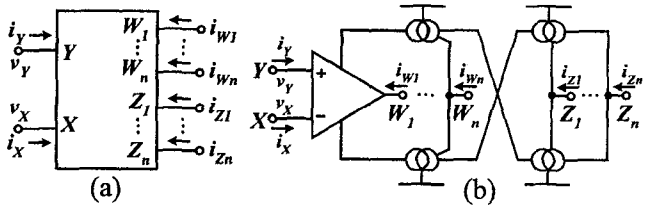


Fig.2 (a) Multi-output FTFN symbol (b) implementation

3. Circuit Description

The proposed circuit can be divided into 2 main sections, the constant-g_m low-voltage P-N complementary input stage and the dual translinear loop output stage, that will be described below.

3.1 Input stage

For lowering supply voltage in an amplifier, it is highly desirable to have a rail-to-rail input voltage swing. The P-N complementary differential pairs have been widely used in the input stage of low-voltage op-amp to achieve this requirement [6]. However, the P-N complementary structure is known to suffer from low common mode rejection ratio (CMRR) due to mismatch errors and the tail current switching between the P and N input stage [5]. Several techniques are invented to resolve this problem. Most of them are usually based on controlling the summation of the tail currents [5-6]. This work, in contrast, uses the maximum current selector circuits to choose only one current from P and N differential pairs, which has the highest magnitude at that time, preventing doubleo utput current when P and N pairs are both turned-on.

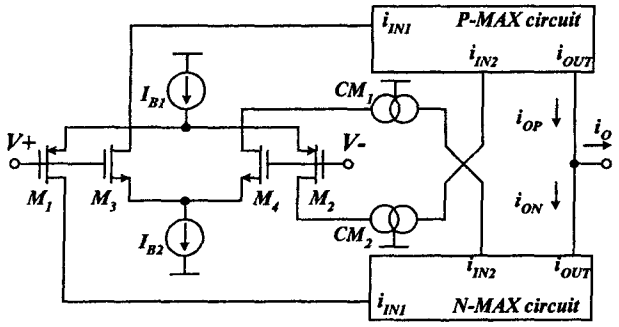


Fig.3 Rail-to-rail input stage using current selector circuit

The proposed structure is shown in Fig. 3. Transistors M_1 to M_4 and the bias current sources I_{B1}, I_{B2} perform the P-N complementary differential pairs. The output signal currents are sent to the maximum current selector P-MAX and N-MAX, where PMAX and NMAX are symbols of PMOS-type and NMOS-type circuit, respectively. CM_1 and CM_2 are replaced with the unity gain current mirrors. The maximum-current selector proposed by Huang and Lui has been chosen for our work and the NMOS-type circuit is redrawn in Fig. 4(a). This maximum circuit was developed based on the bounded difference equation analysis, which can diminish the accumulated errors in the old type binary tree structure [7]. It works like a Wilson current mirror, therefore, the accuracy of the selector circuit can be gained up by appending the additional diode in the same manner as improved Wilson current mirror. In this case, transistor M_{1A} and M_{3A} have been added to the circuit as shown in Fig. 4(b). From the basic analysis of the differential amp, the total output current i_O can be simply depicted as

$$i_O = \max(g_{mN}, g_{mP})(v_+ - v_-) \tag{3}$$

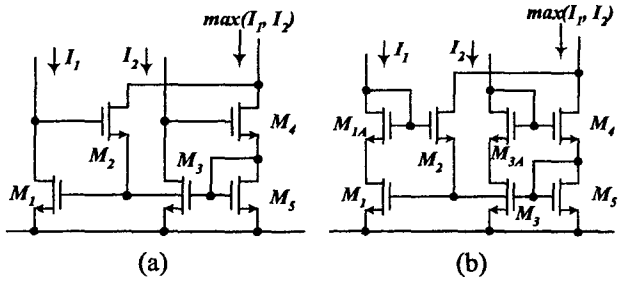


Fig.4 (a) maximum current selector (b) improved circuit

where g_{mN} and g_{mP} are transconductance gain of N and P pairs, respectively. Moreover, since this technique directly measures current from diff-amp using only current maximum selector circuit, it can work well independent of transistor process (bipolar or CMOS) and mode of operation (weak or strong inversion).

3.2 Output stage

The dual translinear loop output stage is shown in Fig. 5(a) which has been modified by injecting small signal current i_a along with DC current bias I_B. The small signal model for calculating current gain A_i of this stage appears in Fig. 5(b). Assume all transistors are identical, we can estimate the current gain as

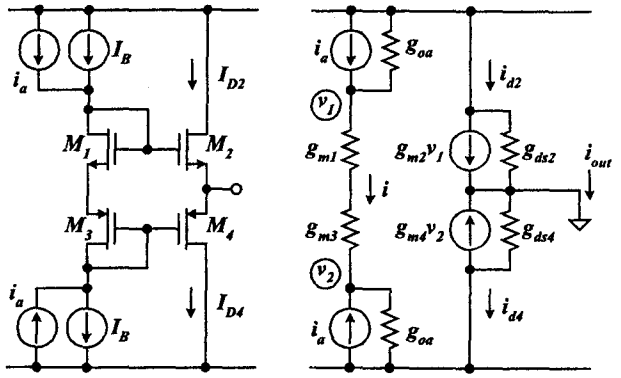


Fig.5 (a) translinear O/P stage (b) small signal model

$$A_i = \frac{i_{out}}{i_a} = \frac{g_{m(tran)}}{g_{oa} // g_{oa}} \tag{4}$$

where $g_{m(tran)}$ is the transconductance gain of MOS transistor in translinear loop and g_{oa} is the output conductance of current signal source i_a.

3.3 Overall amplifier

The simplified schematic of the constant-g_m rail-to-rail CMOS multi-output FTFN is illustrated in Fig. 6. It is designed with the building blocks introduced above, using a 0.7 μm CMOS process supplied by EUROPRACTICE. According to the complete circuit, the maximum selected current from the input stage will be sensed and enlarged by transistor M_{27}, M_{32} before injected to the translinear cell, M_{28} – M_{31}, and then summed to be output current at port W_1. This configuration provides high transconductance gain over a wide frequency range. Transistors M_{33} and M_{36} detect output current at port W_1an d then copy to the other ports. Ideally, it is required that the translinear loop transistors M_{28} – M_{31} are closely matched and all current mirrors have the exact unity gain. We can evaluate the total transconductance gain G_m of this FTFN from combining equation (3) and (4) and give

$$G_m = \frac{i_{W1}}{(v_Y - v_X)} = \frac{\max(g_{mN}, g_{mP}) g_{m(tran)} \dfrac{(W/L)_{27}}{(W/L)_{13}}}{g_{ds27} // g_{ds32}} \tag{5}$$

It should be noted that the transistor with a box at its gate imply to be the super transistor such as cascode or regulated cascode transistor. After using the FTFN in the network with a proper feedback, the translinear cell act as a current-follower that allows output current i_{W1} to sources and sinks at port W_1 and will be reflected and inverted to be current i_{Z1} at terminal Z_1, which keeps up $i_{Z1} \cong -i_{W1}$. The multi-output topology can be easily adapted by adding transistors to the output current mirror set. Transistors $M_{34\text{-}2}$ – $M_{34\text{-}n}$ and $M_{37\text{-}2}$ – $M_{37\text{-}n}$ are used to perform the output terminals W_2 to W_n, respectively. Similarly, transistors$M_{40\text{-}2}$ – $M_{40\text{-}n}$ and $M_{42\text{-}2}$ – $M_{42\text{-}n}$ are used to perform the output terminals Z_2 to Z_n.

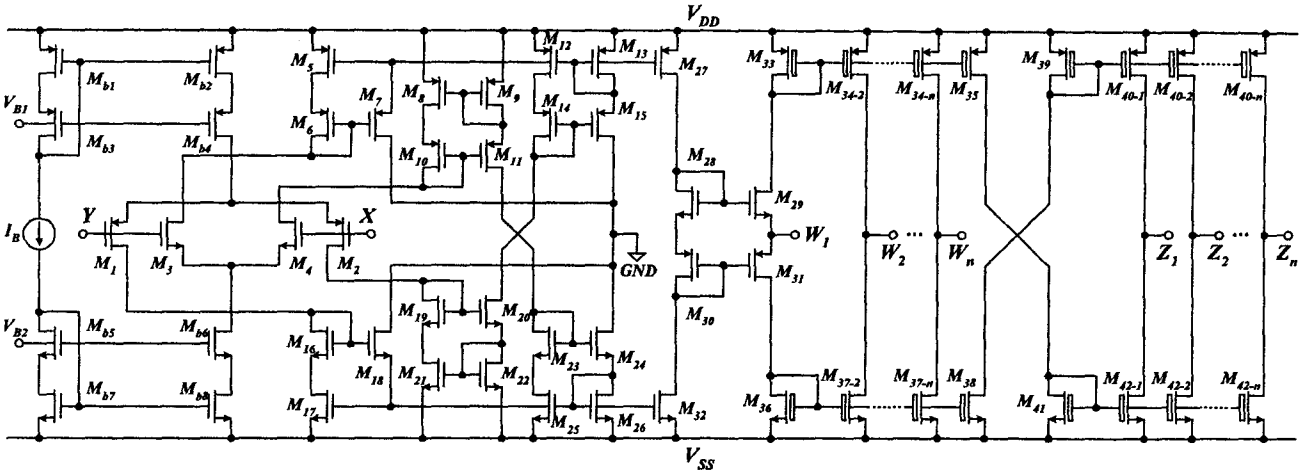


Fig.6 Complete circuit of constant-g_m rail-to-rail multi-output FTFN

3. Simulation Results

The performance of the proposed circuit is verified by HSPICE circuit simulation program based on 0.7-μm CMOS process level-49. All transistor dimensions are listed in Table 1, where W is channel width and L is channel length. The bias currents are set to I_B = 50 μA where the bias voltages are V_{B1} = +1.5V and V_{B2} = -1.5V. Supply voltages are taken as V_{DD} = +2.5V and V_{SS} = -2.5V. The characteristic of open loop transconductance gain is given in Fig. The –3 dB bandwidth can be estimated as about 7 MHz and the transconductance gain about 120 mA/V is obtained.

Table 1 Transistors dimension

Transistors	W/L
M_1, M_2	150μ/0.7μ
M_3, M_4	50μ/0.7μ
$M_5 - M_{15}$, M_{b1}, M_{b2}, M_{b5}, M_{b6}, M_{33}, $M_{34-2} - M_{34-n}$, M_{35}, M_{39}, $M_{40-1} - M_{40-n}$	15μ/0.7μ
M_{b3}, M_{b4}	45μ/0.7μ
$M_{16} - M_{26}$, M_{b7}, M_{b8}, M_{36}, M_{41}, $M_{37-2} - M_{37-n}$, $M_{42-1} - M_{42-n}$	5μ/0.7μ
M_{28}, M_{29}	100μ/0.7μ
M_{30}, M_{31}	300μ/0.7μ

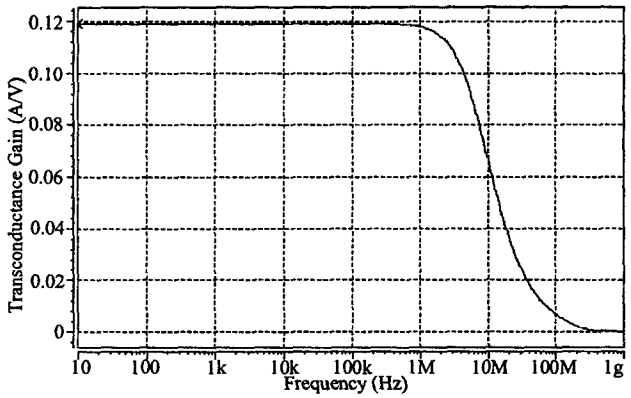
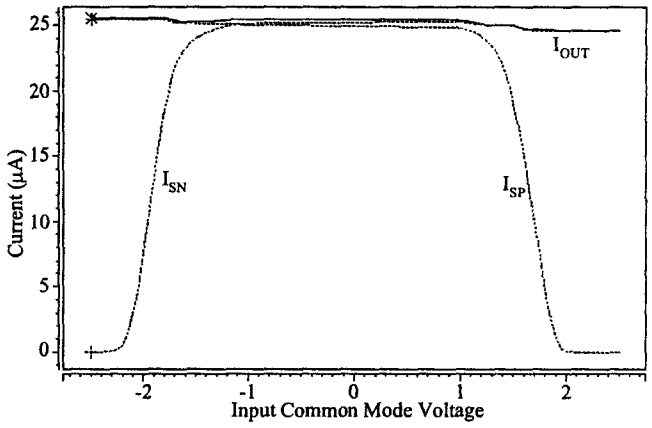
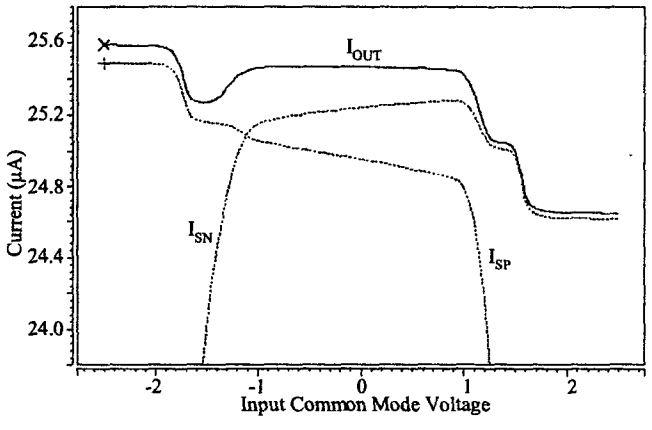


Fig.7 Open loop transconductance gain

This circuit consumeab out 3mW power dissipation. Fig. 8(a) shows the input constant-g_m feature where I_{SN} and I_{SP} are currents from N-differential pair and P-differentialp air, respectively. Fig.8 (b) shows the enlarged view of the maximum current selector operation that can notice a quite good in tracking of output current I_{OUT}. The CMRR of the amplifier is also simulated and shown in Fig. 9.



(a)



(b)

Fig.8 (a) Input stage current (b) enlarged view

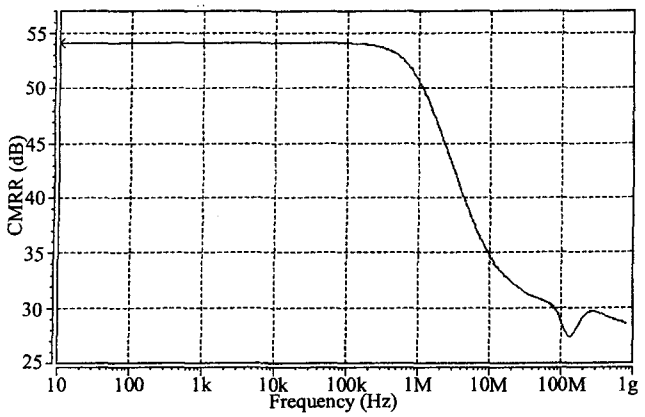


Fig.9 Simulated CMRR of the multi-output FTFN

The frequency response of the CMRR can keep in the same length both in magnitude and bandwidth with a bit better compared to the method mentioned in reference 5 while our proposed structure is simpler. Realisation of a current-mode multifunction filter from reference 2 is chosen as an illustrative example. Filter's structure is redrawn in Fig. 10. MFTFN symbol refers to our proposed multi-output FTFN. The simulation result of the current-mode filter using the proposed multi-output FTFN is given in Fig. 11. It can be observed that the current-mode multifunction filter cannot response correctly since the frequency up to about 100MHz. This is due to the parasitic elements inside the FTFN, which can also be noticed the deviation at the same point of the simulated CMRR result in Fig. 9. One of the major limitations is from current selector circuit itself, which cannot operate in high frequency. The improvement can be done by improving current selector circuit's characteristic.

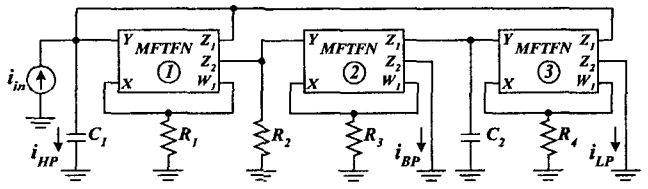


Fig.10 Current-mode multifunction filter

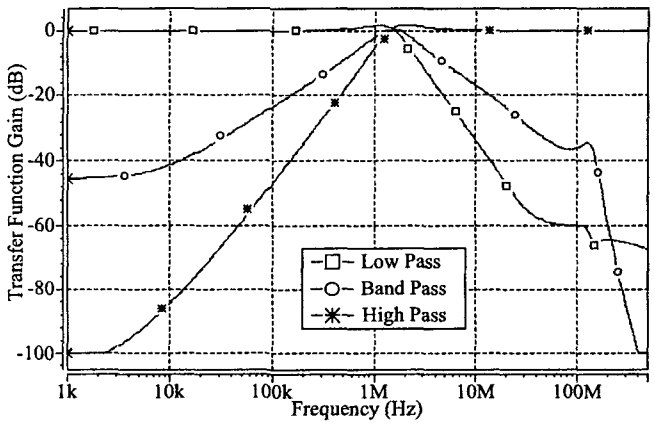


Fig.11 Simulated results of the current-mode multifunction filter

4. Summary

We have proposed a constant-g_m FTFN circuit with additional extended output port. The achievement has been realised through the use of a P-N complementary transconductance amplifier, a translinear cell and standard cascode current mirrors. The maximum current selectors are used to control the overall transconductance of the amplifier. Simulation results from HSPICE program confirm the high qualification of our presented circuit. A current-mode multifunction filter is an example to identify the feasibility of the circuit.

5. Acknowledgement

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