A floating resistor with positive and negative resistance operating at lower supply voltages

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Abstract: In this paper, we propose a floating resistor with positive and negative resistance operating at lower supply voltages. The circuit uses only two transistors between the supply voltages, which enable to operate it at low supply voltages. Moreover, the circuit uses fewer number of transistors compared to the reported work. The gate terminal is used in this circuit for the current addition/subtraction at the terminals of resistor. The characteristic of the proposed circuit is verified using HSPICE for the power supply +/-1.5V.

1 Introduction

In CMOS technology, different design- methods have been proposed for resistors. More often, the resistors were implemented as polysilicon strips or diffused strips, which were passive devices. When the need of programming the resistance value electrically was seen, floating resistors came into the picture. These floating resistors are characterized by having a control voltage for tuning and input/output nodes floating. The reported works designed these types of circuits with MOS transistors operating in either saturation [1], or in linear region [2]. To use floating resistors as synaptic weights in Analog Neural Network, we need wider resistance range and equivalent resistance with positive value as well as the negative value. As a result, we have proposed floating resistors having both positive as well as negative resistance values [5], [6]. Both of these circuits use more than two numbers of transistors between supply voltages that restrict these circuits, when power supply is reduced [7]. On the contrary, the proposed circuit uses only two transistors between the supply voltages, which enable it to operate at low supply voltages. Here, current subtraction is carried out at the gate terminal of the two end points of resistor. Moreover, the circuit uses non-linear cancellation technique proposed in [8]. The characteristic of the proposed circuit is verified using HSPICE for the power supply +/-1.5V.

2 Design method

Design method which is being used here, can be explained through a simple block diagram shown in Fig.1. Two endpoints in the block diagram represent two terminals of resistor where current and voltage are supplied. And current subtraction is carried out at the gate terminal of a MOSFET by wiring, wherein the same transistor is used for input/output voltage, because the current through the gate terminal of MOSFET is zero. Non-linear cancellation block will provide a linear V-I relation for the circuit.

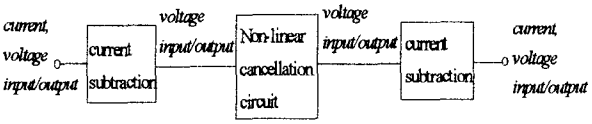

Fig. 1. Block diagram representing the design.

3 Circuit description

Fig. 2 shows the circuit diagram of floating resistor featuring positive resistance. The nodes V_X and V_Y are the two terminals of the resistor. All the transistors are being operated in the saturation region and it is assumed that, for all the transistors, bulks are connected to sources. The drain current for the N-channel MOSFET in the active region is given by

$$I_2 = K_1(V_{GS} - V_T)^2, \quad (1)$$

where $K = \frac{W}{2L}\mu_0 C_{OX}$, W/L is the aspect ratio, μ_0 the electron mobility, C_{OX} the gate oxide capacitance, V_T is the threshold voltage and V_{GS} is the gate-source voltage.

In this circuit, transistors M_1 to M_4 are the transistors for non-linear cancellation and remaining transistors are the current mirrors. The equivalent resistance of the circuit can be expressed by

$$R = \frac{V_X - V_Y}{I_{IN}} = \frac{V_X - V_Y}{I_{OUT}}. \quad (2)$$

The necessary condition for any resistor circuit is that, the input current is equal to the output current, namely,

$$I_{IN} = I_{OUT} = I_2 + I_4 - I_1 - I_3. \quad (3)$$

The currents flowing through M_1 to M_4 are given by

$$I_1 = K(V_X - V_{C2} - V_T)^2,$$

$$I_2 = K(V_X - V_{C1} - V_T)^2,$$

$$I_3 = K(V_Y - V_{C1} - V_T)^2,$$

$$I_4 = K(V_Y - V_{C2} - V_T)^2. \quad (4)$$

Where K is the transconductance value of transistor M_1 to M_4. Substitution of I_1, I_2, I_3 *and* I_4 in (3) results in the current at input/output terminal equal to

$$I_{IN} = I_{OUT} = 2K(V_X - V_Y)(V_{C2} - V_{C1}) \quad (5)$$

Substitution of (5) in (2) results in equivalent resistance equal to

$$R = \frac{1}{2K(V_{C2} - V_{C1})}. \quad (6)$$

From (6) it is clear that the resistance of this circuit is inversely proportional to the difference of control voltages V_{C1} *and* V_{C2}, where K is constant in this circuit. Whenever V_{C1} is greater than V_{C2}, the circuit is going to operate as a resistor circuit with positive resistance.

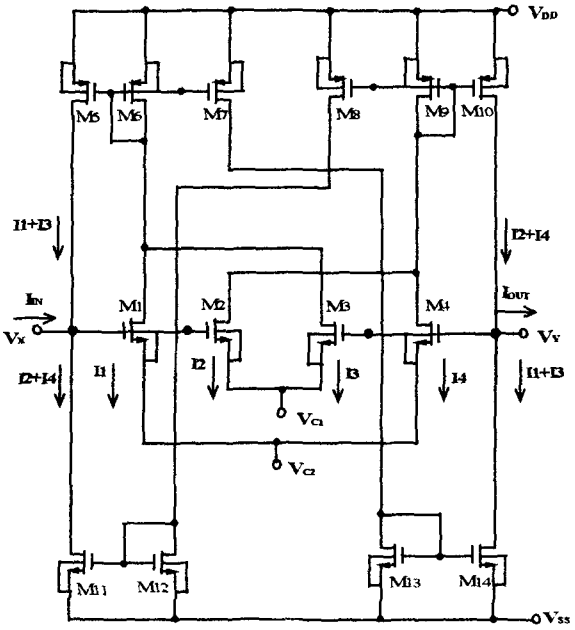

Fig.2. Circuit diagram of floating resistor.

Alternatively, when V_{C2} is greater than V_{C1}, the circuit is going to work as negative resistor. Because the numbers of transistors between the supply voltages are only two, this circuit is assumed to operate at low supply voltage as the voltages V_{C1} *and* V_{C2} are near V_{SS}.

4 Performance Analyses

So far we made calculations assuming that transistors were operated by square law current equations. It is necessary to calculate second order effects such as channel length modulation, mobility reduction to estimate the non-linearity of the proposed circuit.

4.1 Transistor Mismatch

Assume those Transconductance parameters of M_2 and M_4 equal to $K + \Delta K$ and that of M_1 and M_3 equal to $K - \Delta K$. Also, threshold voltage of M_1 and M_3 are assumed to be equal to $V_T + \Delta V_T$ and that of M_2 and M_4 equal to $V_T - \Delta V_T$. As a result, the current at the input/output terminals is,

$$I_{IN} = I_{OUT} = K(V_X - V_Y)(V_{C2} - V_{C1}) + \Delta K \begin{bmatrix} V_X^2 + V_Y^2 + V_{C1}^2 + V_{C2}^2 + 2V_T^2 \\ + 2\Delta V_T^2 + 2V_{C1}V_T + 2V_{C2}V_T \\ - 2\Delta K(V_X + V_Y)(V_{C1} + V_{C2} + 2V_T) \end{bmatrix} \quad (7)$$
$$- 2K\Delta V_T(V_{C1} + V_{C2} - 2V_X - 2V_Y)$$

4.2 Channel Length Modulation

When channel length modulation is considered, the drain current of MOSFET is given by,

$$I = K(V_{GS} - V_T)^2(1 + \lambda V_{DS}),$$

where λ is the channel length modulation coefficient and V is the drain source voltage. By considering the channel length modulation, the current at the input/output terminal is calculated as

$$I_{IN} = I_{OUT} = K(V_X - V_Y)(V_{C2} - V_{C1}) \left[(2 + \lambda(V_X + V_Y + 2V_D - 2V_{C1} - 2V_{C2} - 2V_T)\right] \quad (8)$$

where V_D is the drain voltage of M_1 to M_4.

4.3 Body Effect

Body effect is ignored here as the bulk of all the transistors are connected to the source.

Both the equations (7) and (8) contain non-linear terms which results in linearity error in our proposed resistor circuit.

5 Simulation results

HSPICE at level 28 is used for the circuit simulation and V_{DD} and V_{SS} are kept at 1.5V and –1.5V respectively. The simulation of circuit is carried out by varying the voltage V_{C1} from –1.3V to –1.5V while keeping the voltage V_{C2} at -1.4V. And the obtained resistance values are from 140Kohm to ∞ and –140Kohm to $-\infty$ as shown in Fig.3. Fig.4 shows the plot of conductance against the voltage across the resistor.

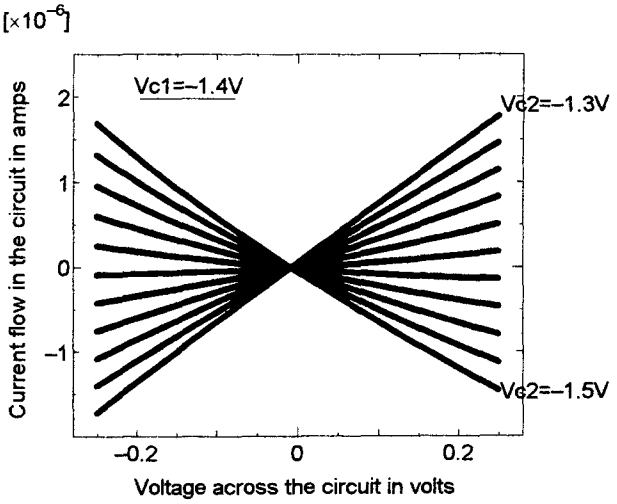

Fig.3. V-I characteristics of floating resistor.

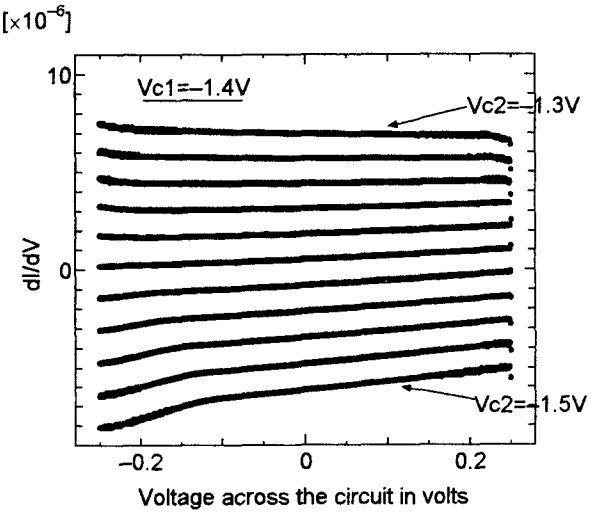

Fig.4. Plot of conductance verses voltage.

6 Conclusions

We have proposed a floating resistor with positive and negative resistance operating at lower supply voltages by using only two transistors between supply voltages. Our structure uses gate terminal for the current addition/subtraction. Simulation results from HSPICE at level 28 and supply voltage +/-1.5V confirms our proposal.

References

1. Sakurai, S., Ismail, M.:"A CMOS square law programmable floating resistor independent of the threshold voltage" IEEE Trans. on Circuits and System II, Vol.39, No.8, pp. 565-574, Aug. 1992.
2. Nagraj, K.,: "New floating voltage controlled resistor " Electronics Letters, Vol. 22, pp.667-668, 1986.
3. Surukampontorn, W., "CMOS floating voltage controlled negative resistor" Electronic Letters, Vol28, No.15, pp.1457-1458, 1992.
4. Tantry, S., Yoneyama, T. and Asai, H.: " Two Floating Resistor Circuits and Their Applications to Synaptic Weights in Analog Neural Networks ", Proc. ISCAS'01, May 2001.
5. Oura, T., Yoneyama, T. Tantry, S. and Asai, H.: "CMOS Floating Resistor Circuit Having Both Positive and Negative Resistance Values" IEICE Transactions on Fundamentals, Vol.E85-A, No.2, pp.399-402, Feb.2002.
6. Tantry, S., Oura, T., Yoneyama, T. and Asai, H.: "A Positive Negative Floating Resistor for synaptic weights" Papers on Technical Meeting on Electronic Circuits, ECT-02-38, pp.81-84, Jan-Feb 2002.
7. Takakubo, K., Takagi, S., Takakubo, H. and Fujii, N.: " An OTA consisting of pair-MOSFET's for Low Power Supply Voltage" 1997 European Conference on circuit Theory and Design, pp. 325-328, Aug-Sept. 1997
8. Zhenhua Wang. "A Four Transistor Four Quadrant Analog Multiplier Using MOS Transistors Operating in the Saturation Region" IEEE Trans. on Instruments and Measurements pp. 75-77, Feb. 1993.