A Behavioral Analysis of an Interpolation FIR filter and Sigma Delta DAC for ADSL Applications•

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Abstract: A transceiver for ADSL systems contains an interpolated combfilter, halfband filters, oversampling sigma delta modulator, a current steering DAC and an analog filter. The circuit complexity of the architecture makes it necessary to use behavioral models to determine the system features. For this reason, we need a specific behavioral simulation environment using the Matlab program. The Matlab is crucial for these circuits to be rapidly incorporated in larger systems, in particular in the context of mixed-signal-test schemes. Design trade-off among the blocks has also been discussed. The design methodology is based on behavioral design and CMOS process.

1. Introduction

The growing market for internet and mobile cellular is forcing the development of high operation speed and high resolution for DSL(Digital Subscriber Line) and communications. Asymmetric digital subscriber line (ADSL) can provide up to 8Mb/s connection from the central office(CO) to a customer premise(CP) and up to 700kb/s from CP to CO. The different techniques on the analog front-end(AFE) is due to the different modulation schemes for the use of echo cancellation(EC) or frequency-division multiplexing(FDM). In the FDM, the upstream transmits data from the remote terminal(RT) modem to CO in the frequency band from 25kHz to 138kHz. The downstream that frequency band is from within 138kHz to 1.1MHz happened in the opposite direction. Upstream and downstream channel separation is around 138kHz. This paper illustrates an approach to design of modeling a sigma delta DAC interface for DMT-ADSL systems. The standard of communications all show a trend toward increased signal bandwidth, thus driving the sampling rates at which baseband signals are encoded into the range of several megahertz. Digital subscriber line protocols are emerging as means of providing data communication rates of several megabits per second.[1][2][3] Also, CMOS VLSI technology continuously decreases the scaling of gate length. This trend serves to eliminate some of the accurate and expensive traditional analog building blocks. With these reasons, it is necessary to validate architecture with static and dynamic response of ADSL systems.[4] Fig.1 shows entire the block diagram flow for sigma delta DAC.

2. Sigma Delta ADC

2.1 The Interpolation Digital Filter

Interpolation filter increases the update frequency by padding zeros between each sample of its input signal. In the frequency domain, this operation gives rise to copies of the original frequency spectrum throughout the frequency range. The digital filter can be programmed to implement the three-stage 32 times interpolation filter for ADSL shown in Fig.1. (M1=2, M2=2, M3=8). A cascade of two stages increases the sampling rate by 4 times. The use of two halfband filters for this purpose provides increased efficiency as compared to a similar designs employing one halfband filter. They are characterized by the same stopband and passband ripple and symmetric cutoff frequency around $\pi/2$. Fig. 2 shows the frequency response of the interpolation halfband filter in the first and second stage.

In fig. 3, a comb filter provides the remaining factor of 8 increases in sampling rate and a multistage comb filters also called sinc filters. The advantage of the comb filter is a simple structure which does not need multiplier and coefficient storage as compared with the FIR filter. And also comb filter is realized with adders and delay units. Thus the chip area and cost can be reduced and easily implement with the cascade stages. The architecture is independent to the interpolation ratio.[5] Table 1 shows the expected process of interpolation for three stages. The transfer fuction of the comb filter is given by

$$H(z) = (1 - z^{L})^{K} \left(\frac{z^{-1}}{1 - z^{-1}} \right)^{K} \quad (1)$$

where L is oversampling ratio.

2.2 The Sigma Delta Modulator

In sigma delta DAC consisting of a digital noise-shaper followed by a core DAC. Mutibit quantization can be used to relax the oversampling requirement. Fig. 4 is the blocks diagram of fifth-order, 5-bit digital modulator used in the converter. The basic building block of the modulator are adders and delay elements.[6] The feedback loop of sigma delta modulator acts to attenuate the quantization noise at low frequencies while emphasizing the high-frequency noise.

In digital subscriber loop applications the attenuation of the noise power by greater than 80dB in relation to the in-band signal power is sufficient to avoid cross talk

between the lines. For the quantizer in a sigma delta modulator, the model uses the noise transfer function(NTF). The NTF can be estimated or calculated directly using a model of the sigma delta loop. The NTF can be represented by

$$H_{NTF}(z) = \frac{(z-1)(z^2-1.997z+1)(z^2-1.992z+1)}{(z-0.7477)(z^2-1.556z+0.6233)(z^2-1.756z+0.8336)} \quad (2)$$

A 5th order sigma delta modulator with 32 times oversampling was simulated. The fast Fourier transformed signal with 2^{13} point and the pole-zero configuration of NTF is shown in Fig. 5 and Fig. 6 respectively. The meaningful measure of the modulator performance is given by the maximum SNR. Fig. 7 shows the circuit's SNR versus the input level based on simulation result. The simulated dynamic range of the modulator is 88.62[dB] at L=32 and sampling frequency fs=8.8MHz.

2.3 The Current Steering DAC

The disadvantage of any switched-capacitor system is the requirement for a two-phase nonoverlapping clock scheme. During on clock-phase the charging of the capacitors has to be done and the second phase the charge transfer on a integration capacitor has to be performed. The unity-gain frequency has to be high. Although the matching of the active devices is worth less than that of the passive devices, a current steering architecture is compatible to switched-capacitor DAC.

The multibit DAC section can be designed using current-steering circuits, wherein transistor matching is essential to achieving high linearity, or charge-redistribution circuits A current mismatch in the DAC causes distortion in the signal band which reduces the obtained signal-to-noise-plus-distortion(SNDR).[6] These noise shaping DAC's use dynamic element matching(DEM) techniques, in addition to improvements in the design and the layout of the analog circuits, to cause the error resulting from step size mismatches to lie outside of the signal band. Most of the noise-shaping DAC architectures have the general form shown in Fig. 8.

Each consists of a digital encoder and $N=2^m$ current cell referred to as unit DAC-elements. Two's complement or binary-coded m-bit data words is processed by the encoder to derive the selection signals for the unit elements. The sum of the selected unit contributions gives the analog output value. Table 2 shows only for 3-bit decoder. The current steering DAC is still in discrete-time and has images centered at multiples of the ovesampling frequency. The output of the current steering DAC still contains images in the frequency domain due to the sample-and – hold element. With an analog continuous time lowpass filter, the images and noise at higher frequencies above the original wanted bandwidth are attenuated.

3. Simulation and Analysis

The simulation, capable of producing the outputs of the digital filter and the sigma delta modulator is programmed with the Matlab. It quickly carry out matrix operations, numerical analysis, signal processing and graphics. Simulations allow the user to assess whether a design is stable for a given input signal. For a specific test of the tool, a fifth order, thirty two times oversampling Interpolation FIR filter was simulated with the Matlab simulink The system of a 5th order sigma delta modulator shows the time domain Matlab output of that. This sigma delta modulator has a band width within 138kHz and 88.62[dB] SNR in 32 oversampling ratio.

4. Conclusion

In this paper, the ADSL front-end with an interpolation filter, an oversampling sigma delta modulator and a current steering DAC has been simulated using the Matlab. With a 5th order modulator and an oversampling ratio of 32, a sigma delta modulator has a bandwidth within 138kHz by optimizing the NTF zeros of modulator. A multistage FIR design for interpolation is more efficient than a single stage approach. The proposed method, the characteristic of the interpolation digital filter and sigma delta DAC can be analyzed before a circuit level design.

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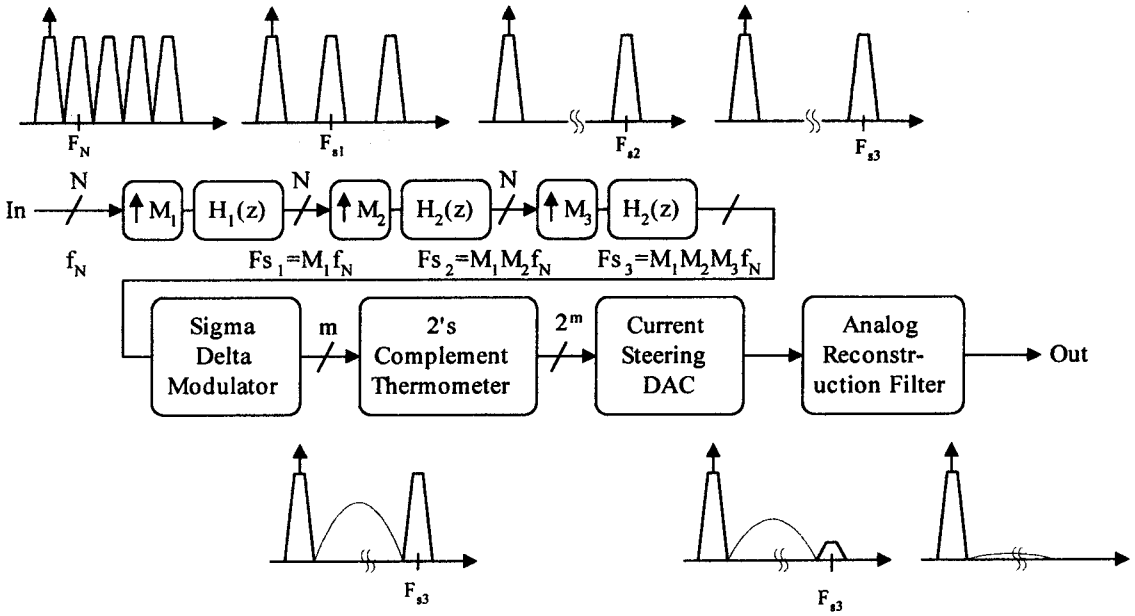


Fig. 1. Block diagram of the interpolation filter and sigma delta DAC.

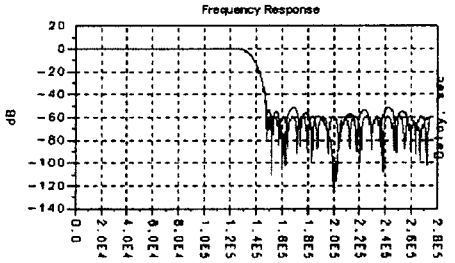
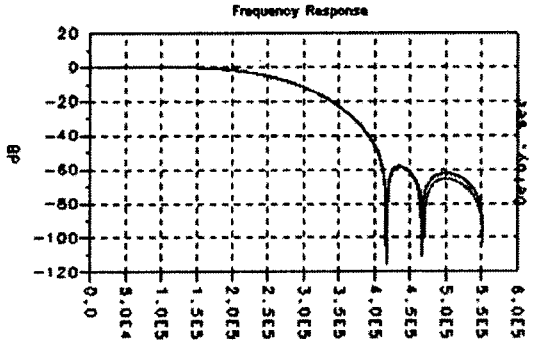


Fig. 2. (a) The first halfband filter $H_1(z)$



(b) The second halfband filter $H_2(z)$.

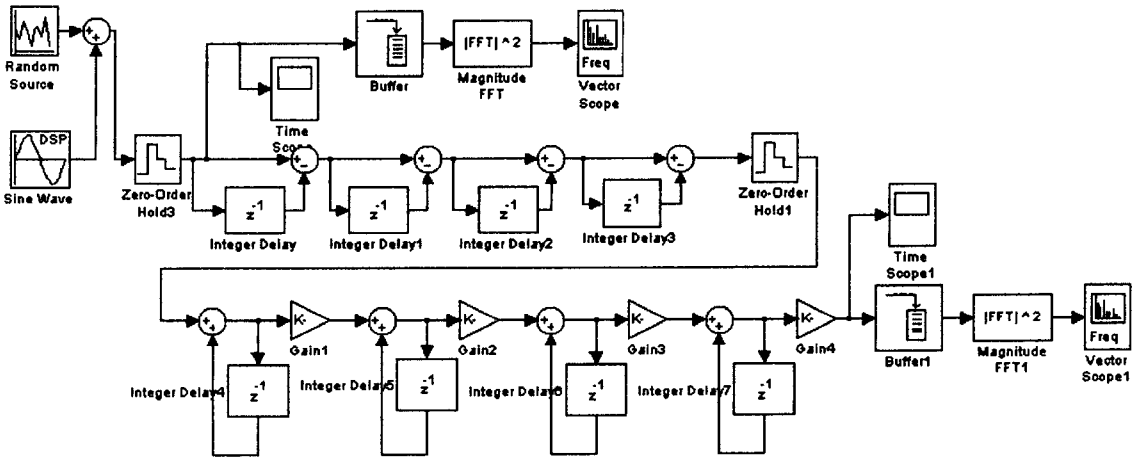


Fig. 3. Interpolation comb filter of 8 times.

Stage	Type of Filter	OSR	Passband Frequency	Sampling Frequency	Passband Ripple	Stopband Attenuation	Taps	Bit
1	Halfband	2	138kHz	552kHz	≤0.2dB	≥60dB	71	14
2	Halfband	2	138kHz	1104kHz	≤0.2dB	≥60dB	19	14
3	Comb	8	138kHz	8832kHz	≤0.2dB	≥60dB	.	14

Table. 1. Parameters for the three-stage cascade filter

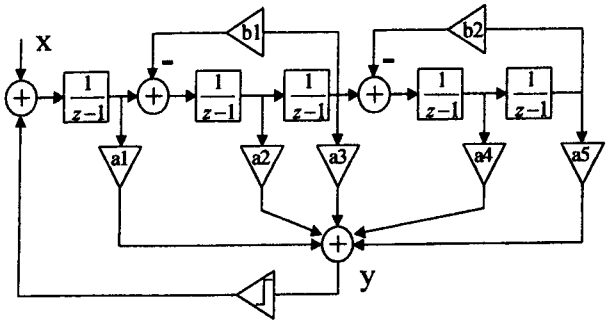


Fig. 4. Feedback structure of the fifth-order sigma delta modulator.

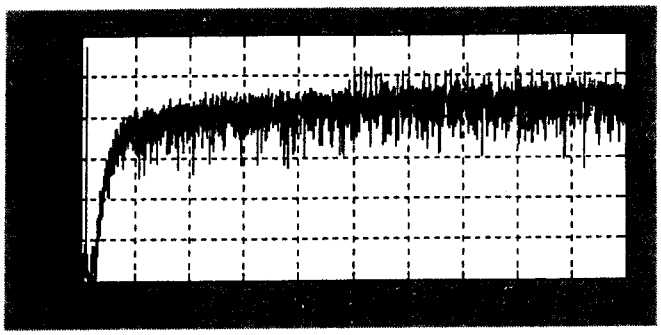


Fig. 5. Output FFT of 5th sigma digital modulator (1 = fs/2, sampling frequency).

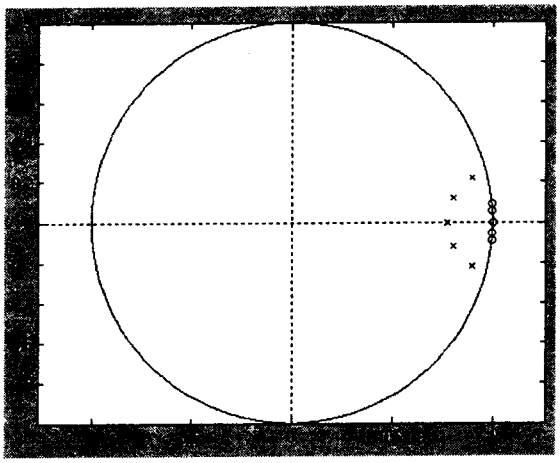


Fig. 6. Pole-zero diagram of the noise transfer function

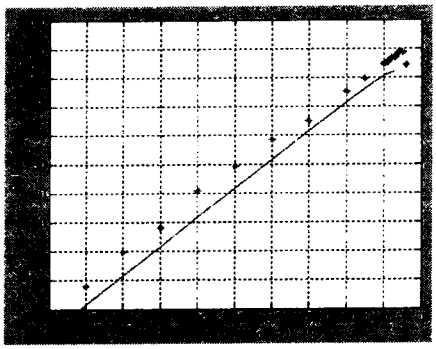


Fig. 7. Plot of SNR versus input amplitude for sigma delta modulator.

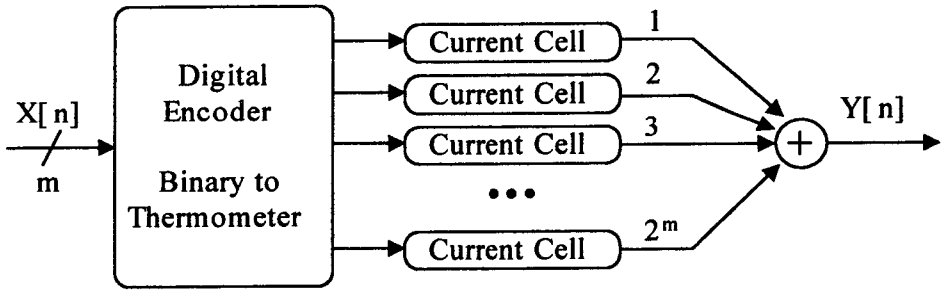


Fig. 8. Architecture of the current steering DAC with a digital encoder.

M2	M1	M0	T1	T2	T3	T4	T5	T6	T7
0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0
0	1	1	1	1	1	0	0	0	0
1	0	0	1	1	1	1	0	0	0
1	0	1	1	1	1	1	1	0	0
1	1	0	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

Table 2. Binary to thermometer decoding for 3-bit binary coding