Low power scan testing and efficient test data compression for System-On-a-Chip

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Abstract

We present a new low power scan testing and test data compression method for System-On-a-Chip (SOC). The don't cares in unspecified scan vectors are mapped to binary values for low power and encoded by adaptive encoding method for higher compression. Also, the scan-in direction of scan vectors is determined for low power. Experimental results for full-scanned versions of ISCAS 89 benchmark circuits show that the proposed method has both low power and higher compression.

1. Introduction

The System-on-a-chip (SOC) has a multiple pre-designed cores. This occurs a serious problem because of the cost and limitations of Automatic Test Equipment (ATE). Thus new techniques are needed for decreasing test data volume in order to reduce memory and testing time.

The method for reducing the test data volume of SOCs is based on the use of data compression techniques. The techniques in [1] exploited that successive test patterns in a test sequence often differ in only a small number of bits. An anther method was presented in [2] by using Golomb codes that map variable-length runs of 0s in difference vector to variable-length codeword. Also, The new class of variable-to-variable-length compression codes was presented [3], which was a frequency-directed run-length (FDR) code. Power consumption is another problem in SOC testing. The low power technique for unspecified test vectors was presented in [4]. However, the compressed test volume was larger than original test set.

In this paper, we present the new techniques reducing both The power consumption and test data volume for scan testing in

SOC. For low power consumption, the several techniques are proposed. First, the don't cares in scan vector is mapped to binary values for reducing the number of transitions in scan vectors. Also, the scan-in direction is determined to reduce the scan-in power. For higher compression of scan vectors mapped for low power, the scan vectors are encoded both by 0's run and 1's run.

2. Proposed strategy

2.1 Mapping unspecified input in scan vector for low power

The efficient mapping method for don't care in unspecified scan vector is described.

As in [5], we only consider the scan-in power and measure it in terms of the number of transitions in the scan vectors. We also use the weighted transitions metric introduced in [5] to estimate the scan-in power. Let the don't care value in partially-specified scan vectors be X, and the specified logic value in scan vectors be A $\in$ {0,1}, the inverted value of A be A'.

There are two cases that may occur. According to case1, case 2, we can map the Xs to binary logic vales.

Case 1. When the scan vector is "XXXA---" or "---AXXX" ;

In this case, the Xs needs to be mapped into A, because this mapping will reduce the number of transitions between A and X.

Case 2. When the scan vector is (the runs of m As)(the runs of p Xs)(the runs of n A's);

If the (m+p) is greater than or equal to the (p+n), the Xs needs to be A, otherwise when the (p+n) is greater than (m+p), the X needs to be A'.

2.2 Low power considering scan-in direction

The scan-in power of scan vectors is strongly correlated with the number of the transitions during the scanning of the scan vectors in the scan chain. The number of the transitions caused by the scan vectors depends on its transition position. To get the fewer transitions, therefore, the transition bit should come as close as the end of the scan-in string. This implies that if we can properly choose the direction of the scan-in, we can make difference in the number of the transitions and decrease the switching power of the scan-in.

2.3 Adaptive Encoding/Decoding using 0's run and 1's run

In this paper, we encode the scan vectors using both the 0's runs and 1's runs. Fig. 1 shows the adaptive codes based on FDR coding. The run-type prefix is added to codeword to classify the 0's run and 1's run. The run-type prefix 0 is added to represent the 0's run encoding, while the run-type prefix 1 is added to represent 1's run encoding.

Group	Run-Length	Type of pattern		run-type Prefix		Group Prefix	Tail	Codeword (run-type & group & tail)	
		0's run	1's run	0's run	1's run			0's run	1's run
A1	0	1	0	0	1	0	0	000	100
	1	01	10				1	001	101
A2	2	001	110			10	00	01000	11000
	3	0001	1110				01	01001	11001
	4	00001	11110				10	01010	11010
	5	000001	111110				11	01011	11011
A3	6	0000001	1111110			110	000	0110000	1110000
	7	00000001	11111110				001	0110001	1110001
	8	000000001	111111110				010	0110010	1110010
	9	0000000001	1111111110				011	0110011	1110011
	10	(10 0s)1	(10 1s)0				100	0110100	1110100
	11	(11 0s)1	(11 1s)0				101	0110101	1110101
	12	(12 0s)1	(12 1s)0				110	0110110	1110110
	13	(13 0s)1	(13 1s)0				111	0110111	1110111
---	---	---	---	0	1	---	---	---	---

Figure 1. Adaptive Encoding

3. Encoding /decoding of scan vectors by considering low power dissipation and high compression

The Fig. 2 shows the algorithm of the encoding and the following lists the encoding process.

(a) Mapping Xs for low power and high compression

(b) Grouping scan vectors into left_first and right_first

(c) Ordering the scan vectors in each group for higher compression

(d) Adaptive encoding using 0's/1's run

```
Encoding()
{ read(scan vectors);
  Num_sv = number of scan vectors
  Num_right = Num_left=1;
  for i=1 to Num_sv
  { X_map(SVi); /** Low power Mapping **/
    calculate left_first_power(SVi);     /*** Grouping ***/
    calculate right_first_power(SVi);
    if(left_first_power >= right_first_power)
      right_first_group[Num_right] = SVi ; Num_right++;
    else
      left_first_group[Num_left] = SVi ; Num_left++;
  }
  Ordering(right_first_group[]);
  Adaptive_encoding(right_first_group[]);
  insert escape codes;
  Ordering(left_first_group[]);
  Adaptive_encoding(left_first_group[]);
} End_encoding;
```

Figure 2. The proposed Algorithm

4. Experimental Results

In this section, we experimentally evaluated the proposed test-data compression/decompression method for the ISCAS 89 benchmark circuits. We used partially-specified scan vector sets generated by MINTEST ATPG program with dynamic compaction.

The table 1 shows the average power[P_{avg_0}] and peak power[P_{peak_0}] of the scan vectors by mapped the don't cares to 0, the average power[P_{avg_prv}] and peak power[P_{peak_prv}] of scan vectors by mapped the don't cares for low power[4] and the average power[$P_{avg\_proposed}$] and peak power[$P_{peak\_proposed}$] of scan vectors mapped by proposed method. The average reduction ratio is about 42% in case of mapped the don't cares to 0. In case of Pavg_prv, the average reduction ratio in this case is about 12%.

Table 2 shows the results of encoding the scan vectors (T_{map}) mapped don't cares for low power. The scan vectors mapped don't cares for low power in [4] were encoded by

[2] (T_{en_golomb}) and [10](T_{en_FDR}). Also, the scan vectors mapped the proposed method for low power was encoded by a proposed encoding procedure ($T_{en\_proposed}$). The size of proposed encoding is average 60% less than that of T_{map}. Therefore, the proposed method has both low power and higher compression.

Table 1. Experimental results on the average /peak power

Circuit	P_{avg_0}	P_{avg_prv}	Proposed		
			$P_{avg\_proposed}$	Reduction Ratio to P_{avg_0}(%)	Reduction Ratio to P_{avg_prv} (%)
S5378	4300	3433	2407	44.1	29.9
S9234	6705	3957	3434	48.7	13.2
S13207	12317	7734	7284	40.9	5.8
S15850	19448	13513	11749	39.6	13.0
S38417	201940	117541	109148	45.9	7.14
S38584	134037	85655	84163	37.2	1.74
Average				42.7	11.8

(a) Average Power

Circuit	$P_{peak\ 0}$	$P_{peak\ prv}$	Proposed		
			$P_{peak\ proposed}$	Reduction Ratio to $P_{peak\ 0}$ (%)	Reduction Ratioto $P_{peak\ prv}$(%)
S5378	12085	11519	11523	4.65	-
S9234	15395	14092	14116	8.30	-
S13207	110129	94879	94887	13.8	-
S15850	84360	70875	70919	15.9	-
S38417	501914	437884	437997	12.7	-
S38584	525417	481158	481190	8.4	-
Average				10.6	-

(b) Peak power

Table 2. Results of encoding the scan vectors mapped for low power

Circuit	Low power Mapped T_{map} (Bits)	Golomb Encoding		FDR Encoding		Proposed Encoding	
		$T_{en\ golomb}$ (Bits)	Compression (%)	$T_{en\ FDR}$ (Bits)	Compression (%)	$T_{en\ proposed}$ (Bits)	Compression (%)
S5378	23754	37240	-56.8	26668	-12.3	11922	49.8
S9234	39273	64297	-63.7	47398	-20.7	21784	44.5
S13207	165200	236075	-42.9	155074	6.12	31807	80.7
S15850	76986	130260	-69.2	90822	-17.9	26376	65.7
S38417	164736	284309	-72.6	198374	-20.4	67150	59.2
S38584	199104	308483	-54.9	216820	-8.9	78295	60.7
Average	—	—	-60	-	-12.3	-	60.1

5. Conclusion

We have presented the new encoding/decoding method for low power and higher compression during scan-in testing of SOC. The proposed methods were the efficient don't care mapping to get both low power and higher compression and adaptive encoding to achieve a higher compression of the scan vectors mapped don't cares for low power. Also, The scan-in direction of scan vectors was determined for low power.

References

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