Hardware design system with the voice communication

Akihito Honda, Hideo Araki, Katsumi Harashima, Toshiro Kutuwa
Osaka Institute of Technology
5-16-1,Omiya, Asahi-ku, Osaka, 535-8585 JAPAN
Phone: +81-6-6954-4304, Fax: +81-6-6957-2136
e-mail: honda@kesakoy.elc.oit.ac.jp, araki@kesakoy.elc.oit.ac.jp
harashima@elc.oit.ac.jp, kutuwa@elc.oit.ac.jp

Abstract: At present there is no hardware design system by using the voice. We try to use the voice communication to the hardware design and to communicate with the computer. This time,we make an application that introduces voice communication and we excute small-scale circuit description.

1. Introduction

Human has a desire for long years. It is that the computer makes something automatically, by talking to the computer. Bi-directional communication method of conversational hardware design has been enabled by the development of voice recognition and the hardware description language (HDL) in recent years. Therefore, we try to use the voice communication to the hardware design and to communicate with the computer. Our research aims to offer the good field of HDL design by the voice communication.

2. Background and Purpose

The hardware design of LSI circuits by schematic input has become very difficult because of complication and enlargement of the system. Therefore design and application by the HDL is widely used as the mainstream of this field now. The following conditions need to be satisfied for design by the description of HDL

(1) User needs to be trained sufficiently to the design method by the HDL.

(2) User is not a handicapped one. (His hand has not handicap.)

We propose the voice communication with computer and hardware engineer, to solve this problem. Our research is based on the purpose of the following point.

(1) Effect that uses the communication

- Improvement of design speed
- Improvement of the accuracy of design
- HDL description would be able to performed more easily than before.

(2) Effects of using the voice inputs as the media of communication

- Improvement of design speed
- Physically handicapped person would be able to attend the hardware design.

3.1 VoiceCommunication

3.1 Process of Voice Recognition

Process of Voice Recognition is shown in Fig.1.

We would research about application part .
(This application controls voice recognition and HDL description).

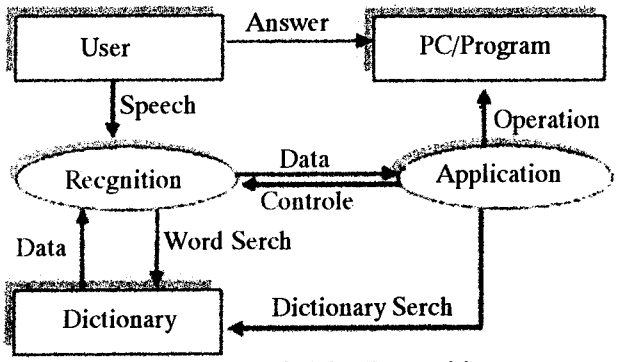

fig1. Process of Voice Recognition

3.2 Bi-directional and Voice Communication for the Hardware Design

Schematic of voice communication is shown in Fig.2.

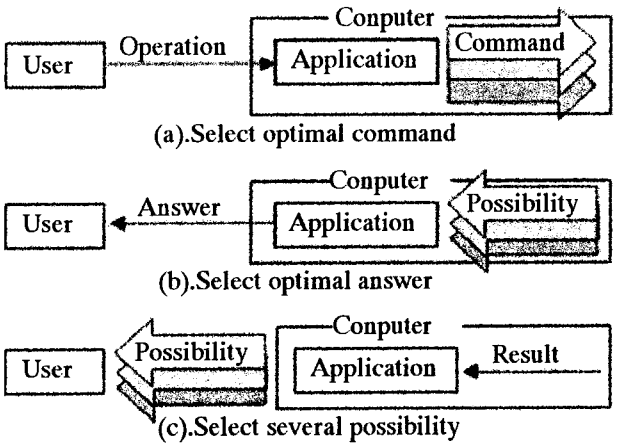

fig2. Schematic of VoiceCommunication

In fig.2(a) ,application selects a optimal command from possible action of expectation even if a user operates the same command . In fig.2 (b), application throttle possibility of action and presents the result to the user . In fig.2 (c), application searches the action which user is able to do , and present it. But the definition of the communication that is obtained from fig. 2 is abstract about use description of hardware design . The above communication for the hardware design is defined as follows:

(1) Voice recognition application program (VRAP) which we develop and show later, directs the next action for the user.

(2) VRAP presents the action that the user would be able to do next step.

(3) VRAP predicts the action of the user to backup the user .

(4) VRAP re-uses again the registered words if it is possible.

By introducing the above communication to the hardware design , the user will be able to design an intended circuit by several keywords

4. Voice Recognition Application Program

4.1 Process of Application Program

Process of application program is shown in Fig.3.

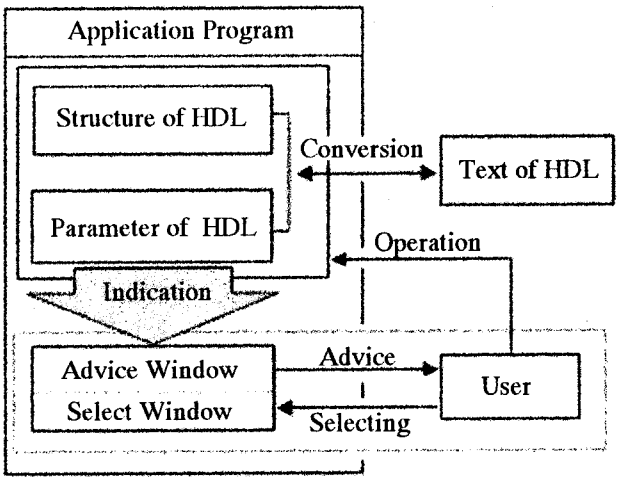

fig3. Voice recognition application program

The user operates two elements, which are a structure and a parameter of HDL. Yet, Structure Part and Parameter Part are not independence relation and be interdependence relation. VRAP has a select window and an advice window. The former shows the display the various choices and the later gives advices and indications to the user for performing this program.

4.2 Structure of HDL

Structure of HDL is shown in Fig.4.

Structure of HDL includes the constitution of grammar about HDL. Also, a part of the status that is used with original VHDL is included to structure part of VRAP. It comes from the following characteristic of structure part.

(1) Point which comes from block structure . : This time Structur Part that we proposed is block structure. Therefore, we can omit the declaration of the beginning of a sentence("LIBRARY","ENTITY ",etc...) in VHDL. Even end of a sentence("END") is similar.

(2) Conjecture from parameter inside the same ID . : IN the case the begining of sentence is "ARCHITECTURE **func** OF" , it will be able to conjecture that the end of sentence is "END **func**".

Therefore, the declaration of the end of a sentence is omitted by combining with the characteristic of (1).

(3) Conjecture from parent and child relation . : We explain parent and child relation by using fig. 4. we give 4 parameters to a block as follows:

(a) ID : The ID is the numerical value that distinguishes an individual block. ID=0 is assigned to project of itself. The ID is number that assigned in order from the top Layer block of ID=1 .

(b) Name : It shows the name that distinguishes the function of each block. In fact, Name is equal to Block_A1 or Block_A2 etc as "LIBRARY ", "ENTITY " etc. ID=0 is Project Name(Structure) .

(c) Depth : It shows the depth of a block . ID=1,5 is Depth=1 and ID=2,4 is Depth=2. Also ID=0 is Depth=0.

(d) Parameter : It shows several parameters of blocks . Parameter of ID=0 has Project Name(Structure) .

When parents X, child make Y, it is necessary that Parent and child relation met the condition as follows .

$$ID(X) < ID(Y) \quad (1)$$

$$Depth(X) = Depth(Y) - 1 \quad (2)$$

Furthermore, when hypothesizing other block (Block Z) , it is necessary the condition is not met simultaneously as follows .

$$ID(X) < ID(Z) < ID(Y) \quad (3)$$

$$Depth(X) \leqq Depth(z) \quad (4)$$

When this condition is met ,X is mother of Y.
Y can do reference of the X's parameter when X is mother of Y . Also ,Y can do reference of the Z's parameter when Z is mother of X . Accordingly, ID=1 is the mother of ID=2,4 and not the parents of ID=3,5. Also,ID=0 is the mother of ID=1. Example,ENTITY's parameter refers to Project's parameter when Name of ID=1 is "ENTITY". Therefore,Application conjectures that parameter is "ENTITY NAME = Structure".

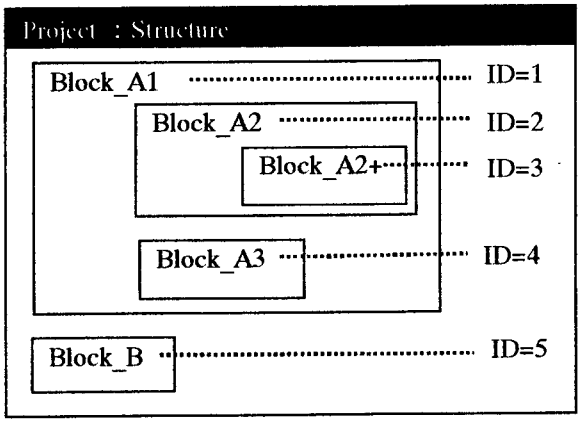

fig4. Structure of HDL

4.3 Parameter of HDL

Parameter of HDL is assigned to each declaration block that is shown in Fig.4.

The item of each parameter is decided with the following 2 items of blocks.

(1) Name of corresponding ID

(2) Number of Parameter : Parameter is stored in array in order from array number 0.

By combining these 2 items, The parameter of the block establishes the meaning . The input method of the parameter is shown below .

(1) Conjecture : Parameter that is inferred from the constitution of Structure of HDL. In this case , the user doesn't need operation. But, it is possible to rewrite forcibly.

(2) Selecting : Application gives possible choice of several action to the user. In this case, the user selects optimal actuation from the choice. The simplest choice is "Yes" or "No".

(3) Description : When the user can't excute the above 2 methods , user do this method. the user writes the number if it is a simple thing. However, it becomes the object word of the method of (1) after the user wrote once.

4.4 System of Conjecture

We express system of conjecture because it is an important element about Bi-directional voice communication .

This application perform the conjecture as follows.

(1) Conjecture of Structure

Insert possible Block Name is inferred from 2 pieces of relation of the block on Structure. These relation is parent and child relation, friend relation. Here, shown the condition of friend relation is shown as follows.

1. They have the same mother ID.
2. When expression is ID=X and ID=Y(Y > X) , application influences only ID=Y.

(2) Conjecture of Parameter

The conjecture of the parameter that comes from the structure of Structure Part. The conjecture of the proper noun that comes from the description of Parameter Part.

(3) Conjecture of Library

Conjecture that improves the problem of voice rcognition itself. Voice recognition has some problems as follows .

(a) Rejection : It's not recognized even if the user talks .

(b) Subjection : The recognition word that the user speaks is recognized as the different word .

(c) Insersion : Application recognition isn't the word of the user expect but the noise of surroundings and user's breath . We propose to reduce these problems as follows

1. Make Many Dictionaries .

Here , Dictionary is the minimum unit of the simple word group that recognizes voice.

2. Get Less Vocabulary

Vocabulary is the word group of voice recognition that combined several pieces of dictionary . Vocabulary is composed with minimum number of dictionaries . Dictionaries are integrated at the time of the operate ,after dividing a word group to the plural. Therefore , it is able to reduce the total number of words in the dictionary . Also , it can reduce the above problem.

5. Description of HDL

5.1 Problem of HDL description

There are several problems in case of HDL design by using voice communication as follows:

(1) There are a lot of words more than we need.

(2) Modification of constitution and parameter of the VHDL is difficult.

Then we conquest the above problems as follows:

(1) We construct the VHDL by the blocks of functional unit.

(2) We give the suitable parameters to the each block of the functional unit.

(3) We synthesize the constitution and parameter of VHDL and change to text.

The visual window displays the constitutions of VHDL and the select window displays selectable data as shown in fig5.

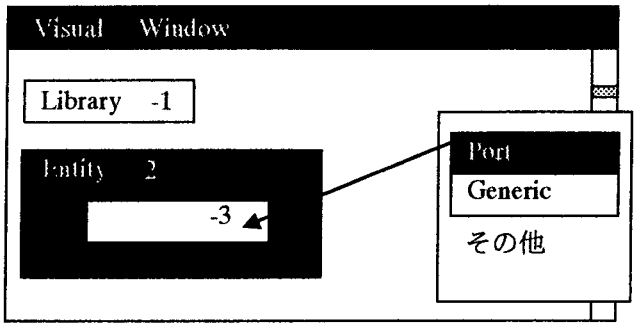

fig 5. Window of Visual Mode

The ID number and the name that indicates the attribute are given to the block of each VHDL constitution. Block ID is used to operate the block. The block's names such as Library, Entity and others denote the characteristics of block.

5.2 Circuit description of Full Adder

Description for FullAdder is shown in Fig.4

```
LIBRARY  ieee ;
USE  ieee.STD_LOGIC_1164.all ;
ENTITY  hadd  IS
     PORT( in1 , in2 , ci  :IN  STD_LOGIC ;
           out , co  :OUT  STD_LOGIC );
END  Fulladd ;
ARCHITECTURE  kinou  OF  Fulladd IS
BIGIN
     out <=(in1 XOR in2) XOR ci ;
     co <=(in1 AND in2)OR ((in1 XOR in2)AND ci) ;
END kinou ;
```

fig6. Description for FullAdder

We design a full adder circuit by using our VRAP. The block diagram is shown in fig.7, and Table 1 denotes the parameters of each block.

Table1. Parameter of Full Adder

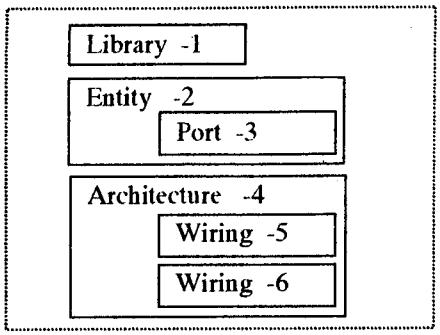

fig7. Structure of Full Adder

Table 1. Parameter of Full Adder

ID	Parameter
1	Default (ieee.std_logic_1164 = "Yes")
2	Fulladd (Project Name)
3	IN
	in1, in2, ci
	None (= STD_LOGIC)
	OUT
	out,co
	None (= STD_LOGIC)
4	Kinou
	Fulladd (Project Name)
5	out <=(in1 XOR in2) XOR ci
6	co <=(in1 AND in2)OR ((in1 XOR in2)AND ci)

In Table 1 , Conjecture of System could conjecture completely the parameter that has background of black.Or, parameter has the default values .

5.4 Comparison of Description

We measured speed of VHDL description for each ID as follows .

(1) Manually description of VHDL .

(2) Use only voice about description of VHDL .

(3) Use voice and manual operation about description of VHDL .

In Table 2 shows , the average results(Sec) that measured it 10 times.

Table 2 average result (Sec)

	ID 1	ID 2	ID 3	ID 4	ID 5	ID 6	計
(1)	26	20	43	38	20	32	179
(2)	0	2	35	15	39	71	162
(3)	0	2	20	8	26	38	94

ID1 is 0 second because the Library declaration can conjecture . From the results of Table.2 ,even if the user describes VHDL by using only voice , sufficient speed is obtained. However, the sufficient speed to the description of free word is not obtained from the result of ID5, ID6 . Also, the result of Table2 show the highspeed of the HDL description by voice and manual operation . Therefore, it shows the dominant that introduce the voice communication to HDL description .

5.5 Discussion on the Described Circuit

The full adder is made of only 6 blocks, and its constitution is easily understood by the user. The circuit configuration would be able to made more easily than before, and the number of parameters can be reduced because that the parameter of the full adder is settled for each block. Depending on this technique, the effects of voice input are denoted as follows:

(1) User can assemble the structure of the circuit just calling the name of each Block.

(2) User calls the identification of each Block and able to modify the structure of the circuit

(3) Application detects identification of Block and, the conversation that the user does predicts and improve the accuracy of speech recognition.

Also, we have subjects as follows.

(1) The consideration to the input to free word.

(2) Improvement of the conjecture system

6. Conclusion

We have developed the VRAP that aims design automation by the Bi-directional conversation with user and computer. By performing almost hardware description with VRAP, we can execute effecting HDL design without careless miss. Also, we think that physically handicapped person will be able to attend the hardware design. However, we must study effective design and HDL support by more conventional voice communication.

A part of this research depends on the cultivating funds of Japan Science and Technology Corporation and on the Party for the Academics Promotion of Japan

Reference

[1] Christopher Schmandt, "Voice Communicatino With Computers" ,Van Nostrand Reinhold.1993

[2] "Manual of the application development support tool for Mitubishi Speech Navi" ,MITUBISHI ELECTRIC CORPORATION.1996