A Compact Rail to Rail CMOS Voltage Follower

Patt Boonyaporn and Varakorn Kasemsuwan
Department of Electronics, Faculty of Engineering
King Mongkut's Institute of Technology Ladkrabang (KMITL)
Tel. +66-2-326-9968 Ext. 102, Fax.: +66-2-739-2398
e-mail: kkvarako@kmitl.ac.th

Abstract: A compact rail to rail CMOS voltage follower is presented. The circuit is based on the symmetrical class AB voltage follower and can operate under supply voltages of ± 1.5 V. The proposed circuit has power dissipation of 5.2mW under quiescent condition and can drive ±1.25 V to 250 Ω load with a total harmonic distortion of less than 0.5 percent and cut off frequency of 237 MHz. Although simple, the proposed circuit enables the output transistors to drive load efficiently.

1. Introduction

An integrated voltage follower is one of the indispensable blocks in many analog VLSI systems. At present, most system requirements make it necessary for the follower to be able to drive low-resistance loads while, at the same time, handle large output voltage swing and maintain low harmonic distortion. Several approaches have been proposed to achieve this goal [1-6]. One among the most popular approaches for realizing such follower is to employ a pseudo source follower which has a pair of complementary common-source MOS transistors. A pseudo source follower has a key advantage in that it offers small output impedance. Moreover, the pseudo source follower offers a larger output voltage swing compared to a simple common drain type source follower. However, this approach suffers from the difficulty in the control of the quiescent current as a result of the random threshold voltage and high transconductance of pullup and pulldown parts. Therefore, any practical circuit using such approach needs to incorporate an additional mechanism to control the quiescent current. In addition, compensation capacitors are required to improve the stability and the transient response and thus resulting in large chip area. Kadanka et al.[7] has proposed wild swing voltage follower without feedback. The circuit contains both BJTs and MOS transistors and is based on a double buffer implemented in the class AB emitter follower configuration. BJTs are employed as a core part and connected as an emitter follower due to two main reasons: 1) BJT has higher transconductance over MOS transistor, and 2) the mismatch in base-emitter voltage(ΔV_{BE}) of npn and pnp is much less than the mismatch in the gate-source voltage(ΔV_{GS}) of NMOS and PMOS. The circuit shows good dynamic performance, good stability and low power dissipation. The circuit implementation however requires BiCMOS process which has lower level of integration and higher power dissipation compared to the well known CMOS technology.

This paper presents a compact rail to rail CMOS voltage follower which is capable of handling large output voltage swing and maintaining low harmonic distortion. The circuit is based on the symmetrical voltage follower with additional circuit to enhance transconductance and, at the same time, reduce gate-source voltage mismatch. The circuit can operate under ±1.5V supplies and can drive ± 1.25V to 250 Ω load with a total harmonic distortion of less than 0.5 percent and cut off frequency of 237 MHz. The power dissipation under quiescent condition is 5.2mW.

2. Circuit Description

A conventional symmetrical voltage follower is shown in Fig. 1. The circuit consists of four transistors(M1-M4) connecting in the two stage common drain(double buffer) using class AB configuration. This configuration however has three main drawbacks: 1) a large offset voltage due to the mismatch between the gate-source voltage of NMOS and PMOS, 2) a high output impedance due to a reduced transconductance(g_m) of the MOS transistor compared to BJT's counterpart, and 3) a significant limitation in the linear output swing. All these problems can be alleviated using the proposed circuit shown in Fig. 2.

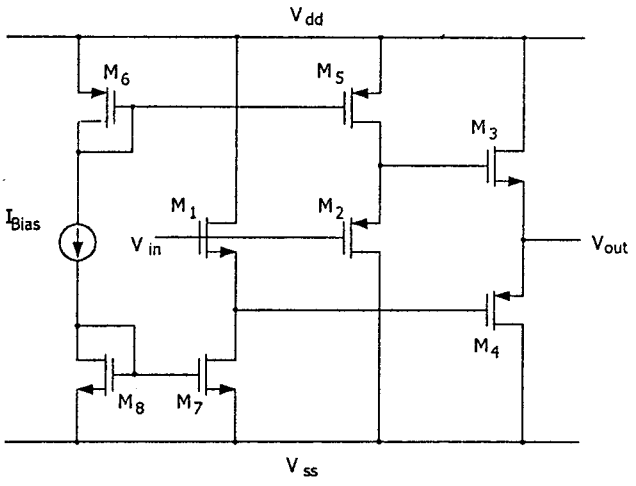

Figure 1. Conventional symmetrical voltage follower.

The proposed circuit in Fig. 2 is based on the symmetrical voltage follower described in Fig.1. The four transistors (M1, M3, M5 and M7) work as two stage common drain stage and are biased by current mirrors implemented by both NMOS and PMOS transistors (M2-M4 and M6-M8) with a transfer current ratio of α(see Fig.2). Since M1 has the same drain current as M2 and M3 has the same drain current as M4, the gate-source voltages of M1 and M3 are then nearly equal provided that all NMOS have the same dimensions and all PMOS have the

same dimensions. This gate-source voltage matching approach is also applied to the upper follower (M5-M8). As a result, the offset voltage of the voltage follower has been minimized[8].

The transconductance of the output MOS transistors can be increased by using two compound transistors as suggested in [8] consisting of M1-M4 and M5-M8. The transconductance of the lower follower (M1-M4) and upper follower (M5-M8) are given by Eqs.(1a) and (1b) as

$$g_{m(LOWER)} = \frac{g_{m1} \cdot g_{m3}}{g_{m1} - \alpha \cdot g_{m3}} \quad (1a)$$

$$g_{m(UPPER)} = \frac{g_{m5} \cdot g_{m7}}{g_{m5} - \alpha \cdot g_{m7}} \quad (1b)$$

respectively.

From Eqs.(1a) and (1b), the transconductance of output transistors can be adjusted through the transfer current ratio α. The simulation shows that proper value of α can result in very high transconductance.

For the input voltage with the amplitude in between V_{LOW} and V_{HIGH}, the circuit will operate as a conventional voltage follower with an enhanced transconductance and the reduced gate-source voltage

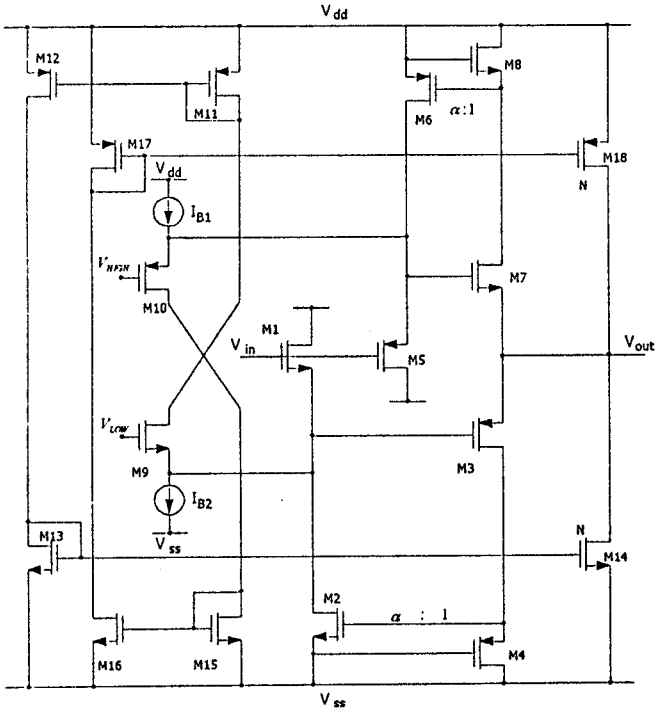

Figure 2. Proposed rail to rail voltage follower

mismatch. By using Eqs.(1a) and (1b), the output impedance of the circuit is given by

$$R_O = \left(\frac{1}{g_{m3}} - \frac{\alpha}{g_{m1}}\right) \Big\| \left(\frac{1}{g_{m7}} - \frac{\alpha}{g_{m5}}\right) \quad (2)$$

If the input voltage is lower than V_{LOW}, the bias current I_{B2} for both transistors M1 and M9, which are connected as a differential amplifier, mostly becomes the drain current of M9 and is mirrored by two current mirrors M11-M12 and M13-M14. M14, which has its width N-times that of M13, now acts as bias current for the upper voltage follower(M5-M8). The output is capable to swing within one overdrive (V_{DSATI4}) of the negative supply with the output impedance $R_{O(LOW)}$ given by $1/g_{m7} - \alpha/g_{m5}$. Similarly, if the input voltage is higher than V_{HIGH}, the bias current I_{B1} for transistors M5 and M10, which are connected as a differential amplifier, mostly becomes the drain current of M10 and is mirrored by two current mirrors M15-M16 and M17-M18. M18, which has its width N-times that of M17, now acts as bias current for the lower voltage follower (M1-M4). The output in this case is capable to swing within one overdrive (V_{DSAT18}) of the positive supply with the output impedance $R_{O(HIGH)}$ given by $1/g_{m3} - \alpha/g_{m1}$.

A low quiescent current of the circuit are obtained by properly selecting biasing currents I_{B1} and I_{B2} and two bias voltages V_{HIGH} and V_{LOW}. We have chosen the V_{HIGH} and V_{LOW} to be 0.5 V and -0.5 V and I_{B1} and I_{B2} to be 10 μA respectively. The quiescent current as a result is found to be 550 μA.

3. Experimental Results

To evaluate the performance of the proposed circuit, the simulation is performed using HSPICE with a standard twin well 0.6 μm CMOS technology. All *W/L* values of the transistors used in the circuit are summarized in Table I. It is noted that the mobility of the electron in this process is approximately four times that of hole and the transfer current ratio α used in this work is around 1/8. The simulations results show high performance characteristics, namely low output impedance, low harmonic distortion, large linear output voltage swing, wide bandwidth and low power dissipation. The proposed voltage follower is connected to drive ±1.25 V to 250 Ω load and the highest output impedance of the circuit is found to be less than 3.8 Ω while the harmonic distortion is less than 0.5 percent. Figure 3 shows DC transfer characteristics of the circuit with the same load. Dotted and solid lines represent input and output waveform respectively. As seen, the output can trace the input over a wide range linearly. Figure 4 shows output waveform of the circuit with the sinusoidal input signal of $1.5V_{PP}$, 1kHz. Figure 5 shows a frequency response of the circuit. The cut off frequency is found to be 237MHz. Figure 6 shows the output impedance of the proposed follower for the ±1.5V input signal. The maximum output impedance is found to be 3.8Ω. for the output signal in the range of ±1.25V. Figure 7 shows the total harmonic distortion (THD) for various input voltages of 1kHz. Lastly, the simulation shows the total power dissipation of 5.2mW under quiescent condition.

4. Conclusions

A compact rail to rail CMOS voltage follower is presented. The circuit is based on the symmetrical class AB voltage follower and can operate under supply voltages of ± 1.5 V. The proposed circuit has power dissipation of 5.2mW under quiescent condition and can drive ±1.25 V to 250 Ω load

with a total harmonic distortion of less than 0.5 percent for input voltage less than 1.25V and cut off frequency of 237 MHz. The maximum output impedance is less than 3.8 Ω for the output signal in the range of ±1.25V.

Table 1. Aspect ratio of transistors

Transistors	Aspect Ratios (*W/L*)
M1,M2,M9	55/1
M3,M4	750/0.6
M5,M6,M10	220/1
M7,M8	450/0.6
M11,M12,M17	4.6/1
M13,M15,M16	1.2/1
M14	380/0.6
M18	1305/0.6

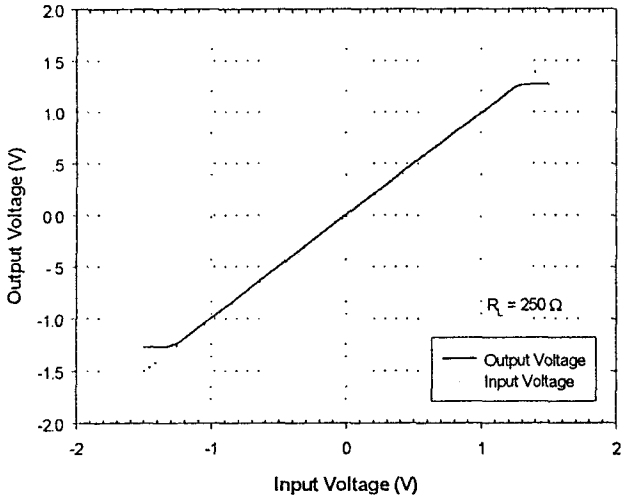

Figure 3. Dc transfer characteristics

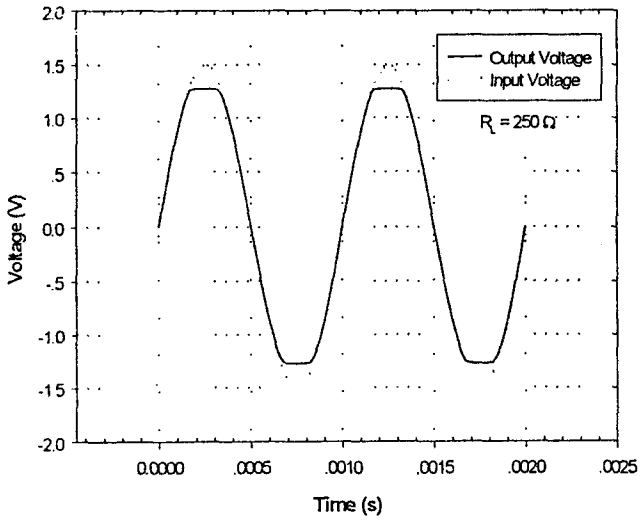

Figure 4. Output waveform

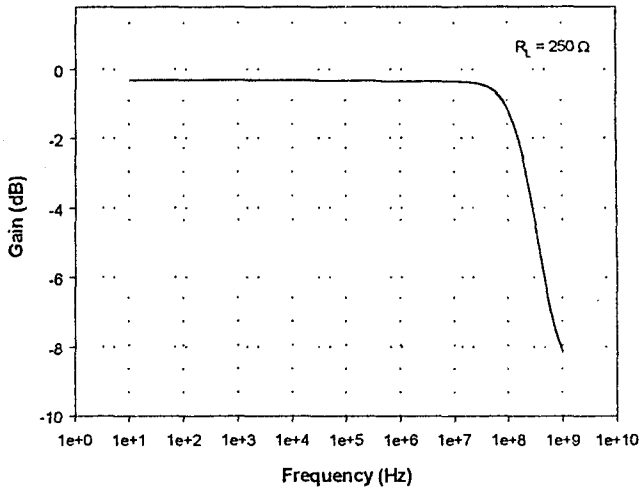

Figure 5. Frequency response of the proposed follower

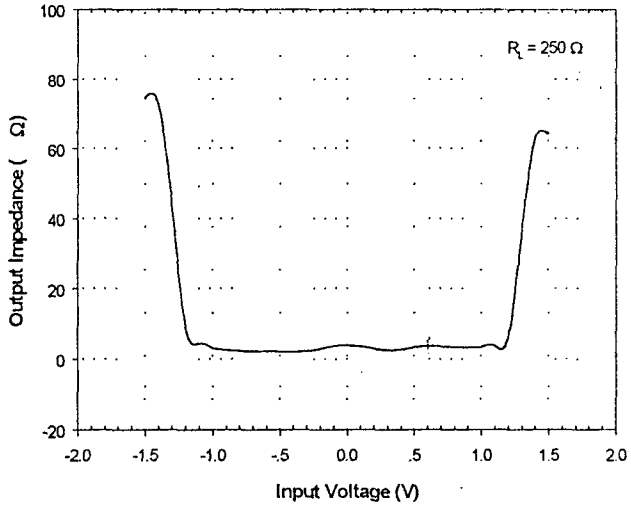

Figure 6. Output impedance

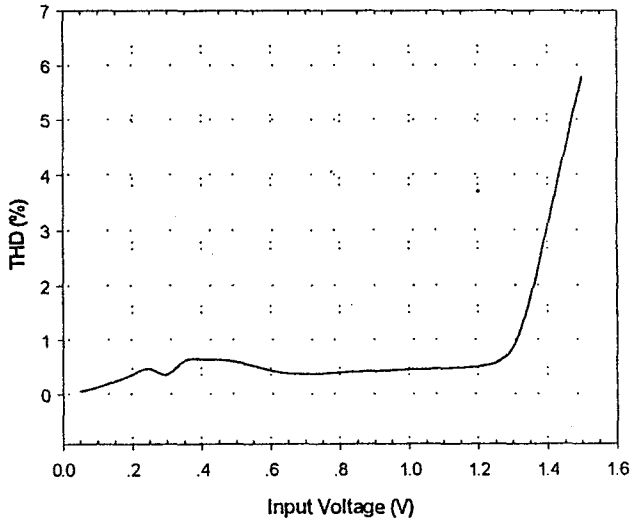

Figure 7. Total harmonic distortion (THD)

5. References

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