A Current-Mode Analog Programmable FIR Filter for SDR Terminals

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Abstract: We propose a current-mode analog programmable finite-impulse-response (FIR) filter with variable tap circuits. From the circuit simulation, the operation of the 7-tap FIR filter is comfirmed. We design and fabricate the 0.0625-step tap circuit using 0.8μm CMOS technology. The proposed FIR filter has a variable length of taps and variable coefficients, so it has a potential for being used to software defined radio (SDR) terminals.

1. Introduction

Software defined radio (SDR) is a promising solution for multi-mode and multi-band mobile communication system [1]. The ideal SDR system has the components of a digital signal processor and an analog-to-digital converter (ADC) directly connected to an antenna. The ideal SDR architecture can be comprised with only digital signal processor (DSP). Although the recent ADC and DSP operate at high frequency, it is difficult to implement ADC of more than 10GHz sampling frequency [2]. In addition, DSP with low power consumption of less than 100mW over 10GHz operation is difficult to implement [3]. Thus, programmable analog components, especially programmable filters such as the radio frequency (RF) /immediate frequency (IF) band-pass filter, the root-roll-off filter are required.

In mobile terminals, dielectric, surface-acoustic-wave and ceramic filters are used in RF and IF. However, these filters have fixed center frequency and fixed bandwidth characteristics. Filters designed for various communication systems are needed for SDR system. Using the filter with various center frequency and various bandwidth characteristics, mobile terminals can be designed with a small size.

We have already proposed and implemented the current-cut switched current matched filter (CC-SIMF) using current-mode analog circuit [4]. The power consumption of CC-SIMF can be remarkably reduced. The current-mode analog circuit has features such as (1) high-frequency operation, (2) low voltage operation, (3) constant power consumption and (4) simple circuit configuration without linear capacitors.

In this paper, we propose a programmable current-mode analog finite-impulse-response (FIR) filter with a variable tap circuit. A variable tap circuit structure is described. From the circuit simulation, programmable operation of the 7-tap FIR filter is confirmed. We design and implement the 0.0625-step tap circuit using 0.8μm CMOS technology. Programmable operation of the fabricated tap circuit is observed.

2. Current-Mode Analog Programmable FIR Filter

Figure 1 shows the block diagram of the FIR filter. The filter has components of a voltage-current (V-I) converter, a delay line using a current delay flip-flop (CDFF), a tap circuit, a current summation circuit and a current-voltage (I-V) converter. The input voltage signal is converted to the current signal using the V-I converter. The current signal is input to the CDFF. The output signal from the CDFF is input to the next CDFF and the tap circuit, delaying one clock period in each CDFF. For a certain tap coefficient, the input current to the tap circuit is weighted. The output current of the tap circuit is input to the summation circuit. Summation is performed by a *Wired-Or* structure. Finally, the output current signal is converted to the output voltage signal using the I-V converter.

Figure 2 shows the current memory (CM) circuit. The CM circuit is the basic circuit of the SI circuit. The CM has components of a current source, a memory MOSFET, an input switch, an output switch, a control switch and a dum-

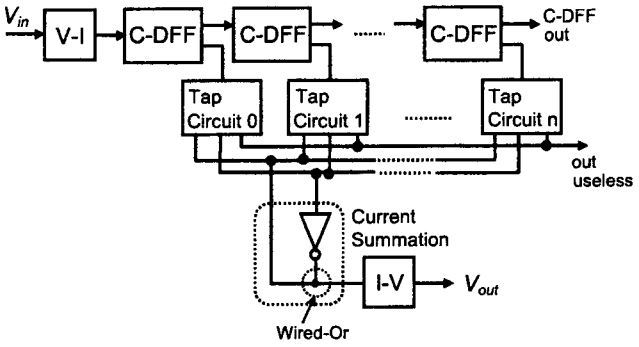


Fig. 1 Circuit block diagram of the FIR filter.

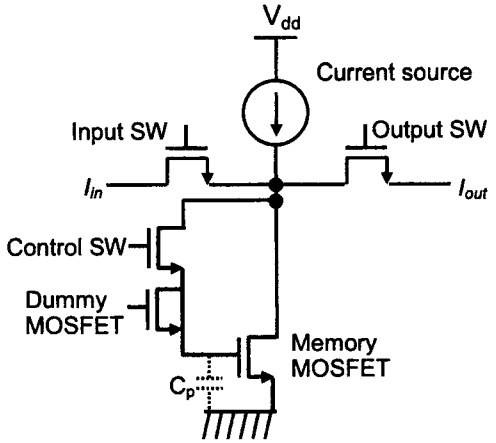


Fig. 2 The structure of Current Memory (CM).

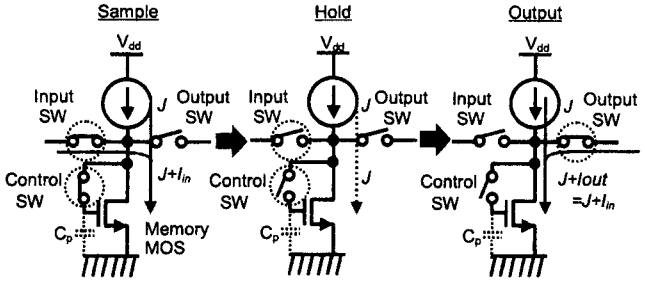


Fig. 3 Schematic diagram of CM operation.

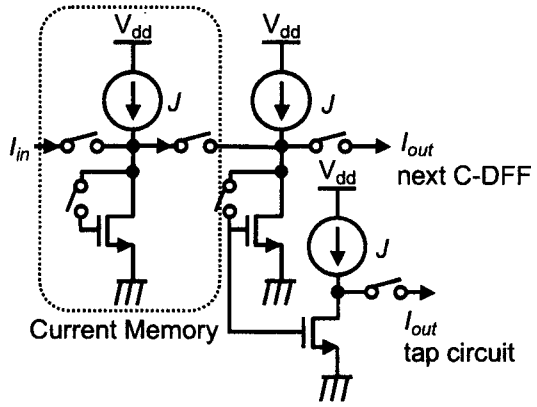


Fig. 4 The structure of Current Delay Flip-Flop (CDFF).

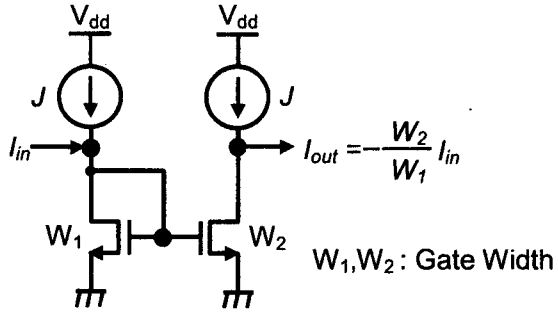


Fig. 5 The structure of Gate width-ratioed current mirror.

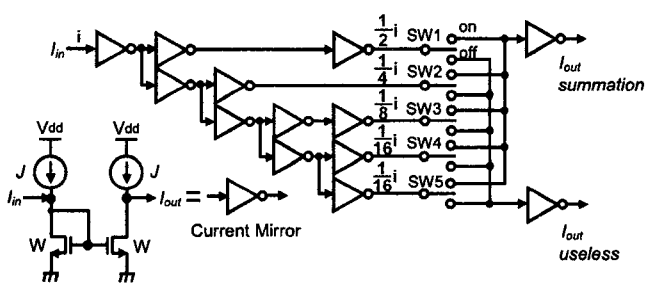


Fig. 6 The structure of 0.0625-step tap circuit.

my MOSFET [5]. The CM operation is performed using the charge memorized in the gate-source parasitic capacitance of the memory MOSFET. Figure 3 shows the schematic diagram of the CM operation. The operation is devided in the three periods, "sample", "hold" and "output". In the "sample" period, the input switch and the control switch is connected, and the output switch is disconnected. The current flow through the control switch is memorized by the charge at the paracitic capacitance of a gate of the memory MOSFET. In the "hold" period, all switches are disconnected and the input current is being memorized. In the "output" period, the output switch is connected and the input switch and the control switch are disconnected. The output current depending on the charge at the gate of the memory MOSFET can be obtained. The output current flow in the opposite direction to the input current. The CDFF is constructed using three CMs with one input node and two output nodes, as shown in Fig. 4. The input current is delayed and mirrored to the tap circuit.

Table.1 7-tap FIR filter coefficients.

Tap No.	0 and 6	1 and 5	2 and 4	3
Filter coeff.1	0.0625	0.3125	0.7500	1.0000
Filter coeff.2	-0.0625	0.0000	0.5625	1.0000

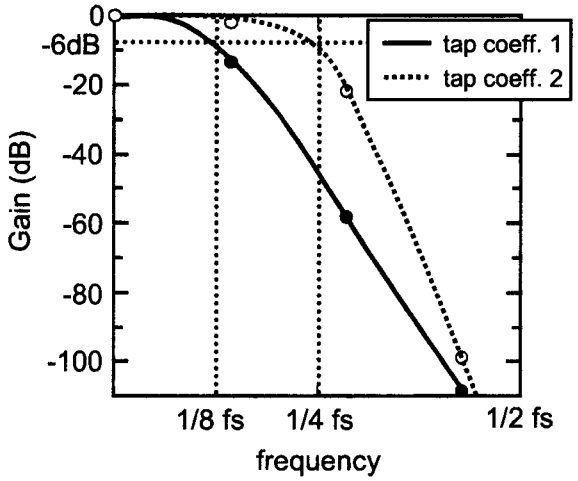
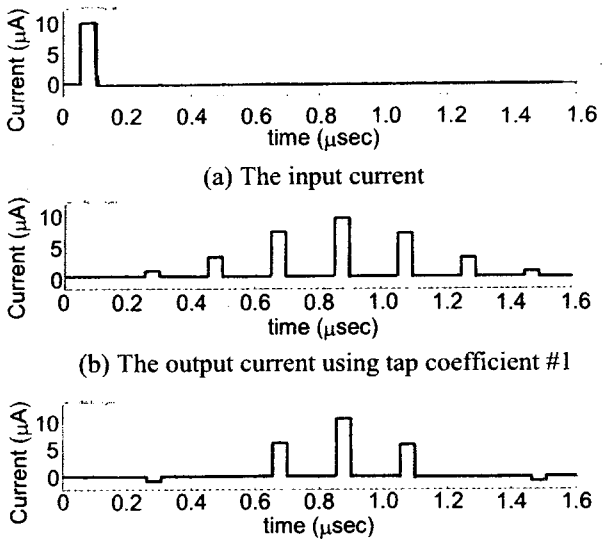


Fig. 7 Spectrum waveform of 7-tap FIR filter using tap coefficients in Table 1.

For programmable operation of the FIR filter, the tap circuit is required to operate programmably. The conventional tap circuit, as shown in Fig. 5, consists of the gate-width-ratioed current mirror circuit. Using the fixed tap circuit structure, programmability can not be obtained. Figure 6 shows a proposed tap circuit. The tap circuit consists of the same gate-width current mirrors and switches. When the SWx is on, the current flow into I_{out} *Summation* line, where x is 1,...,5. The current flow through SW1 is half of, SW2 is fourth part of, SW3 is eighth part of, SW4 and SW5 are sixteenth part of the input current. In Fig. 6, minimum output current step is 0.0625.

The 7-tap FIR filter has been simulated by programming with C language. Table 1 shows the tap coefficients. Figure 7 shows the spectrum waveforms of the 7-tap FIR filter using the tap coefficients in Table 1. The solid line is



(a) The input current

(b) The output current using tap coefficient #1

(c) The output current using tap coefficient #2

Fig.8 Time response waveforms of 7-tap FIR filter using Cadence SpectreS circuit simulator.

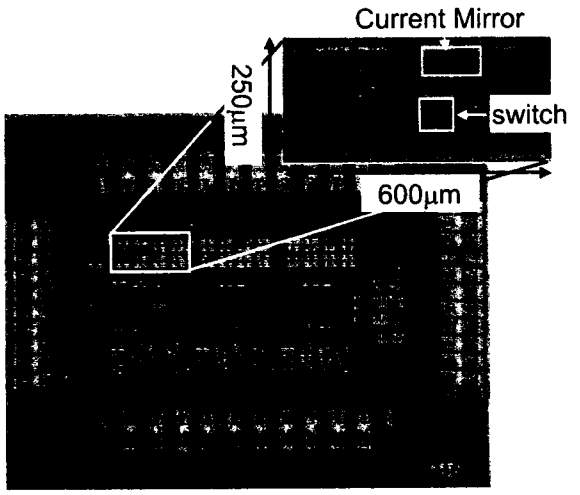


Fig. 9 Fabricated 0.0625-step tap circuit photograph.

the spectrum waveform using coefficient #1. The broken live is spectrum waveform using coefficient #2. Being used tap coefficient #1, the output current amplitude is as half as the input current at 1/8 fs, where fs is sampling frequency. Being used tap coefficient #2, the output current amplitude is as half as the input current at 1/4. Using the proposed tap circuit, programmable cut-off frequency can be obtained. The time response waveform of the 7-tap FIR filter using Cadence SpectreS circuit simulator are shown in Fig. 8, the input current in Fig. 8(a), the output current using tap coefficient #1 in Fig. 8(b) and the output current using tap coefficient #2 in Fig. 8(c). The input current is 10μA. The input current multiplied by the tap coefficient is the output current. In Fig. 8(b) and (c), the output current error between computer simulation and circuit simulation is almost zero. The 7-tap FIR filter can be operated with high accuracy.

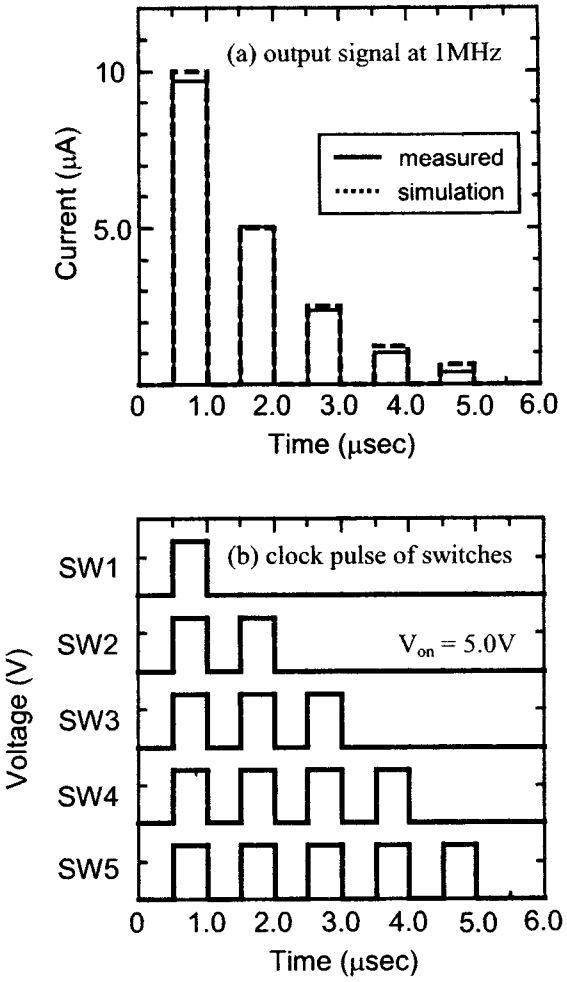


Fig. 10(a) Output signal at 1MHz of the fabricated 0.0625-step tap circuit and (b) clock pulse of switches.

3. Fabrication and evaluation

We have fabricated the 0.0625-step tap circuit using 0.8μm CMOS mixed signal technology. The foundary is AMS (Austria Mikro Systeme). The broker is CMP (Circuit Multi-Projets, France). The fabricated process is a 2-metal and 2-polysilicon process for a mixed signal design. We have used only 2-metal and 1-polysilicon layers. This means that the circuit can be fabricated using the same process as the conventional digital CMOS process.

Figure 9 shows the fabricated 0.0625-step tap circuit. Size of the tap circuit is 600μm×250μm.

Figure 10(a) shows the simulated and measured waveform at 1MHz with clock pulse of switches in Fig. 10(b). The input current is 10μA. The programmable operation of the tap circuit using digital clock is confirmed, although maximum error between measured and simulated output current is 26%. For the implementation of this work, we have not optimized layout of the tap circuit. This error can be reduced by optimizing of design with considering all paracitic capasitances in the tap circuit. The measured maximum operation frequency is 4MHz. This is because the maximum operation frequency is limited by the conversion speed of off-chip V-I/I-V converter using the

operational-amplifier. The settling time of this circuit with the Cadence SpectreS circuit simulation is less than 5nsec. With the on-chip V-I/I-V converter, operation of frequency higher than 100MHz can be obtained.

4. Conclusion

We have proposed a current-mode analog programmable finite-impulse-response (FIR) filter with the variable tap circuits. From the circuit simulation, the 7-tap FIR filter have been operated programmably. We have designed and fabricated the 0.0625-step tap circuit using 0.8μm CMOS mixed signal technoligy. Programmable operation of the proposed circuit have been confirmed. Error between measured and simulated output current can be small by optimizing the layout of the circuit. The current-mode analog FIR filter has a variable length of taps and variable tap coefficients. The proposed FIR filter has a potential for being used software defined radio terminals.

References

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