# Design and Implementation of the 16-QAM Modem for 26GHz FBWA system

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**Abstract:** This paper presents the design and implementation of 16-QAM modem that can be applied to fixed broadband wireless access system. It is implemented in the hardware prototype that consist of FPGA(Field Programmable Gate Array) for digital signal processing and analog front end module for analog signal processing. We provide 20.48Mbps data rate using implemented modem and test the modem in KOREA 26GHz broadband wireless local loop system including IFU(Intermediate Frequency Unit) and RFU(Radio Frequency Unit) via air interface.

## 1. Introduction

Internationally, there are actively proceeding in study for the Broadband Fixed wireless communication system including BWA(Broadband Wireless Access) of IEEE802.16 and FWA(Fixed Wireless Access) of Europe and Japan. In KOREA, there are two kinds of outstanding FBWA(Fixed Broadband Wireless Access) systems, called B-WLL(Broadband Wireless Local Loop) and BMWS(Broadband Multimedia Wireless Service). B-WLL is the broadband fixed wireless communication system using 26GHz radio frequency band. And, BMWS is the high density fixed system(HDFS) using 40GHz radio frequency band. In this paper, we describe the BWLL system overview and design and implementation of the 16QAM modem for the 26GHz B-WLL system. For the implementation of the 16QAM modem, we designed the prototype of modem hardware that can support 20.48Mbps data rate and control the IFU parameter such as power gain and frequency offset.

This paper is organized as follows. Section 2 presents the 26GHz B-WLL system overview. The design and implementation of modem hardware is presented section 3. And, we conclude in Section 4.

## 2. System Overview

B-WLL is a local point-to-multipoint wireless access system which delivers broadband multimedia services with FDD(Frequency Division Duplexing) full duplexing scheme between a BS transceiver and subscribers, such as individual houses and blocks of apartments within its cell or sector area.

In medium access methods, TDM and TDMA are used for downlink and uplink respectively. Modulation methods of the QPSK and 16QAM are used .

The cell radius is usually about 3~4Km for availability of 99.99% in the raining condition of 42mm/hour. Due to the propagation characteristics of millimeter-wave, the LOS(Line Of Sight) between the BS antenna and the subscriber antenna is required necessarily for reliable communication. We describe the system configuration in figure 1.

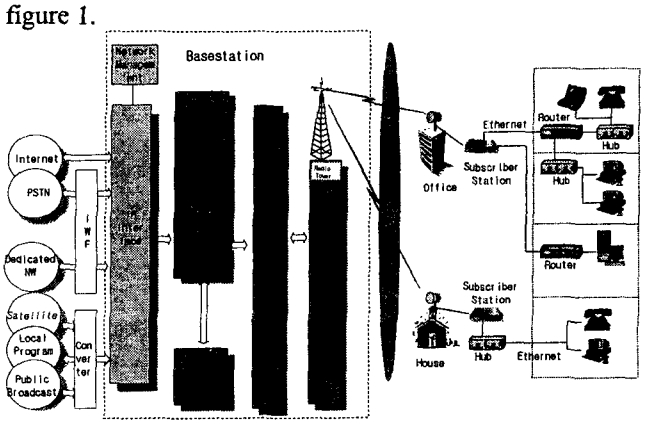


Figure1. B-WLL System Configuration

In KOREA, the frequency band for B-WLL is 24.25 ~26.7GHz which is divided into three blocks, 24.25 ~ 24.75 GHz for uplink, 25.5~ 26.7GHz for downlink, and 24.75 ~ 25.5GHz for guard band between uplink and downlink in the FDD scheme. In figure 2, we describe the frequency allocation according to operator such as Hanaro Telecom, Korea Telecom and Dacom. In table 1, we summarize the air interface specification for the B-WLL system according to KOREA telecommunication technology association.

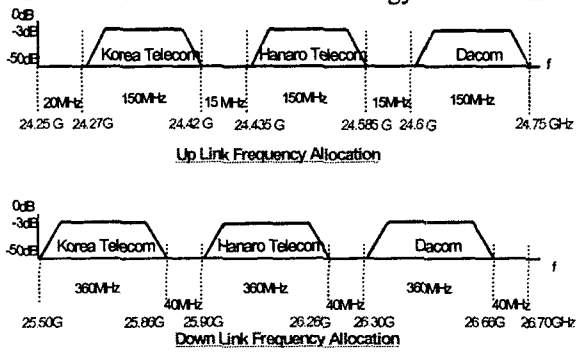


Figure 2. Frequency Allocation of the 26GHz B-WLL

Table 1. Air Interface Specification

| | Description | |
|---|---|---|
| | Down link | Up link |
| RF Frequency | 25.50~26.70GHz | 24.25~24.75GHz |
| IF Frequency | 950~1550 MHz | 450~750 MHz |
| Access Method | TDM | TDMA |
| Data Rate | 40~50Mbps | 10.24Mbps |
| Modulation | QPSK,16-QAM | QPSK |
| FEC | RS Code(204,188) | Variable RS Code |
| Transmission | Continuous MPEG-2 Stream | Variable Length burst Packet |

## 3. Design and Implementation of the 16-QAM modem for B-WLL down link

In this section, we describe the design and implementation of the 16-QAM modem for the B-WLL down link.

The down link is configured as follow. Base station transmit the continuous data to subscriber station. In base station, modem encode and modulate the data from MAC layer as follow. Modem perform the sync byte detection, data scrambling , Reed Solomon(204,188) encoding, convolutional interleaving, differential encoding, in phase and quadrature phase symbol mapping, baseband pulse shape filtering, and digitally up conversion to 40.96MHz carrier frequency. Digitally up converted signal is converted to analog signal via AFE and transmitted to air interface through IFU and RFU. In subscriber station, Received signal from IFU and RFU is digitized in AFE and digitally down converted to baseband signal in FPGA demodulator. Subscriber modem demodulate and decode the signal from AFE as follow. To demodulate, we implement the matched filter, AGC, symbol timing recovery, frequency offset remover, carrier phase recovery and equalizer. After we demodulate the signal, we decode the data using RS decoder, de-interleaver, de-scrambler and differential decoder. In figure 3, we describe the configuration of the implemented modem.

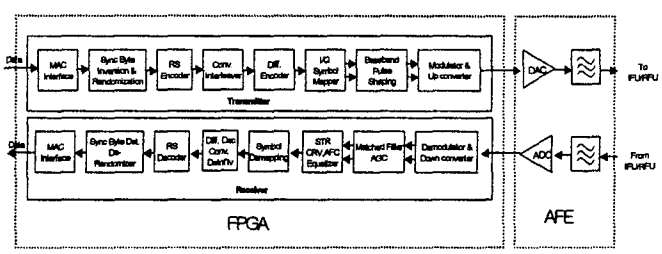


Figure 3. Configuration of the implemented modem

In table 2, we summarize the implemented modem parameters that are compatible with KOREA B-WLL Standard.

Table 2. Modem Parameter

| | |
|---|---|
| Randomization | $1 + X^{14} + X^{15}$ ,Initialization : 100101010000000 |
| Reed-Solomon encoding | (204,188) with T=8 byte errors corrected |
| Interleaving | Convolutional with depth I=12 |
| Modulation type | 16-QAM |
| Differential Encoding | Enabled/disabled |
| Spectral shaping filter | $\alpha = 0.35$ |
| Data Rate | Up to 20Mbps |
| Data Transmission | Continuous MPEG-2 stream |

And, we will describe the essential design algorithm to demodulate the signal such as matched filter, AGC, AFC, symbol timing recovery, carrier recovery .

### 3.1 Matched Filter

Matched filter is square root raised consine filter with roll-off factor equal to 0.35. We use 41-tap FIR filters with 7 bit coefficients. This matched filter operate at 4 times over sample clock relative in symbol rate.

### 3.2 Automatic Gain Controller

The automatic gain controller (AGC) control the amplitude of incoming signal to analog-to-digital converter so that it can be sampled in digital value in the linear region to minimize the quantization loss. It also adjust the output level of a demodulator in order to decide the samples into the soft-decided symbols accurately. The implemented AGC scheme is depicted in figure 4[5].

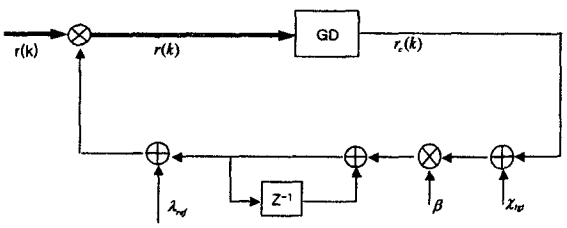


Figure 4. Automatic gain controller

The AGC circuit consists of a gain detector (GD), an integrator and two multipliers. We use the GD as

$$r_c(k) = \frac{1}{\sqrt{2}}\left(|r_r(k)| + |r_i(k)|\right). \quad (1)$$

### 3.3 Symbol Timing Recovery(STR)

The symbol timing recovery should work with frequency and phase uncertainties. Symbol timing recovery consist of interpolator, timing error estimator, loop filter and interpolator controller as shown figure 5. To estimate symbol timing error, we use Gardner algorithm which have good performance in the presence of the frequency offset up to 12.5% of symbol rate[6]. The Gardner algorithm is represented as

$$\begin{aligned} x_{GD}(n) = {} & z_i(nT - T/2 + \hat{\varepsilon}T)\left[z_i^*(nT + \hat{\varepsilon}T)\right] \\ & - \left[z_i^*((n-1)T + \hat{\varepsilon}T)\right] \\ & + z_q(nT - T/2 + \hat{\varepsilon}T)\left[z_q^*(nT + \hat{\varepsilon}T)\right] \\ & - \left[z_q^*((n-1)T + \hat{\varepsilon}T)\right] \end{aligned} \quad (2)$$

where, $\hat{\varepsilon}$ is a fractional timing error, T is a symbol period.

In a high speed digital modem, an interpolator is frequently used to get a sample at the recovered symbol timing. Even though samples at any time axis between inputs are calculated, we restrict the resolution of the interpolator to 4 discrete points between samples. As a result, our STR has a residual timing error less than or equal to $\pm 1/32$ of symbol period, which is considered to be small enough for commercial digital modem implementation [7,8]. As we use 4 sets of fixed coefficients, 4 interpolators calculate interpolation values in parallel. Thus a down sampler select one of them according to the timing error evaluated by eq.[2].

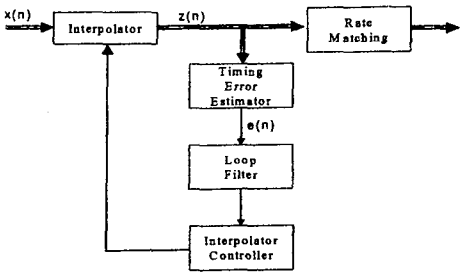


Figure 5. Symbol timing recovery scheme

### 3.4 Carrier Frequency Recovery

The carrier frequency recovery is essential to the MPSK modem. Even though, a state-of-the-art RF module has extremely high stability and accuracy, there still exist small amount of the frequency offset[9]. We assume the bound of frequency offset be tens of KHz. This will assure that a frequency offset never exceed 12.5% of the symbol rate. With this assumption, the STR using the Gardner algorithm will work without an AFC in front of it. Thus, we use the frequency recovery circuit after symbol timing is recovered, i.e. one sample per symbol is utilized for the frequency error estimation. The acquisition is acquired during the preamble period easily due to the preamble pattern. But in order to stay in the tracking mode during the data reception, the data modulation must be removed. Among the various nonlinear functions to remove the data modulation, we use the $\mathrm{mod}(x, 2\pi / M)$ algorithm. In the case of 16-QAM, M equals to 16 [9]. The maximum frequency offset which can be estimated will be $f_R / 8$. Figure 6 represents a block diagram of the carrier frequency recovery circuit.

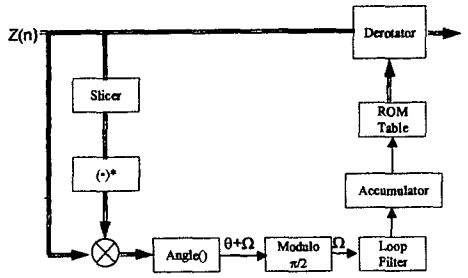


Figure 6. Carrier frequency recovery scheme

### 3.5 Carrier phase recovery

To compensate the carrier phase offset of received signal, carrier phase recovery which consist of phase error detector, 2nd loop filter and direct digital synthesizer is designed. To estimate the carrier phase error, decision directed(DD) phased error estimation algorithm is used.

$$\begin{aligned} \mathrm{Im}\left\{z_k \hat{d}_k^*\right\} / \left|\hat{d}_k\right|^2 &= \mathrm{Im}\left\{\alpha \hat{d}_k e^{j\theta} \hat{d}_k^*\right\} / \left|\hat{d}_k\right|^2 \\ &= \mathrm{Im}\left\{\alpha e^{j\theta} \left|\hat{d}_k\right|^2\right\} / \left|\hat{d}_k\right|^2 \\ &= \alpha\, \mathrm{Im}\left\{e^{j\theta}\right\} \cong \alpha\theta \end{aligned} \quad (3)$$

Figure 7 represents the DD carrier phase recovery circuit. We use 8 bits wide accumulator to express phase angle. Thus the resolution of the phase recovery should be $\pi / 128$, i.e. $1.4^o$.

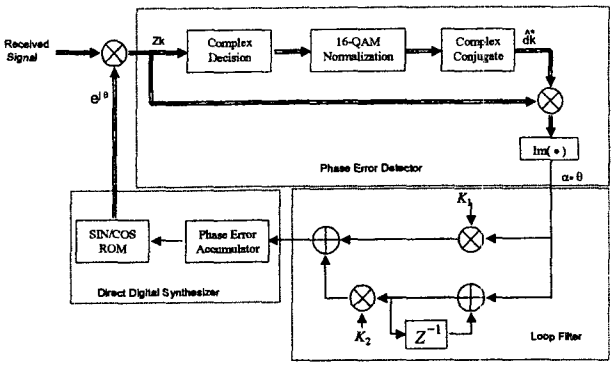


Figure 7. Carrier phase error recovery scheme

### 3.6 Modem implementation

We implement a 20.24Mbps 16-QAM modem prototype for B-WLL system. To implement the digital modem, we use FPGA chip of EP20K1000EBC652-1x[9]. In addition to FPGA chip , Analog Front End module which consist of D/A converter , A/D converter and filter is implemented. Table 3 shows the resource usage of modem configured in FPGA chips. The modem prototype is depicted in figure 8.

Table 3. Resource usage of modulator and demodulator

| | | Logic Elements(%) | Memory(ESB) |
|---|---|---|---|
| TX | RS Encoder | 230 (<1%) | |
| | Scrambler | 52 (<1%) | |
| | SQRC Filter | 1224 ( 5%) | |
| | Up Converter | 859 ( 3%) | 320(<1%) |
| | Others | 81 (<1%) | |
| | Total | 2446/24320 (10%) | 832/311296 (<1%) |
| RX | Down Converter | 472 ( 2%) | |
| | SQRC Filter and STR | 1492 ( 6%) | |
| | Freq. Recovery | 3422 (14%) | 20480 ( 7%) |
| | Phase Recovery | 1653 ( 7%) | 4096 ( 1%) |
| | RS Decoder | 8699 (36%) | 6144 ( 2%) |
| | Others | 1174 ( 5%) | 1056 (<1%) |
| | Total | 16912/24320 (70%) | 31776/311296 (10%) |

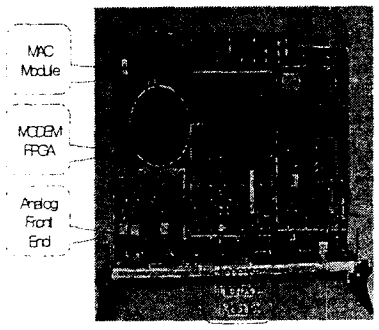


Figure 8. Presented prototype board for MODEM

### 3.7 Experiments and Performance Analysis

The functions of implemented modem are tested with IFU and RFU via air interface. Figure 9 show the configuration used for the functional test. As it is shown in figure 9, we analyze the modem performance at modem using some tet equipment such as logic analyzer, oscilloscope and spectrum analyzer. Figure 10 show the spectrum of modulated signal. The separation between in band and out band signal is over 50dB. Figure 11 show the demodulation performance. Scatter diagram of the demoludated signal is presented.

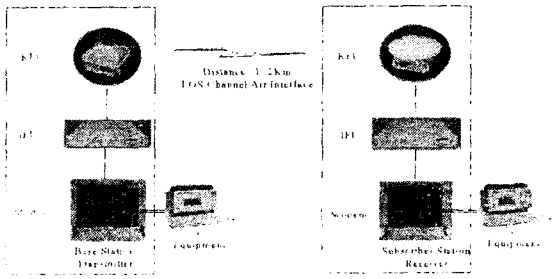

Figure 9. Test configuration of implemented 16-QAM modem

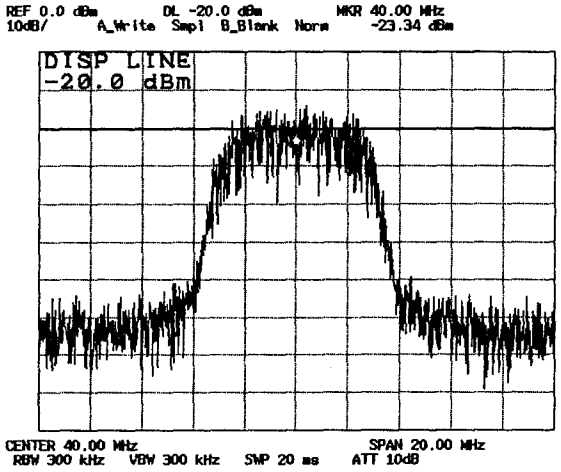


Figure 10. Modulator output signal

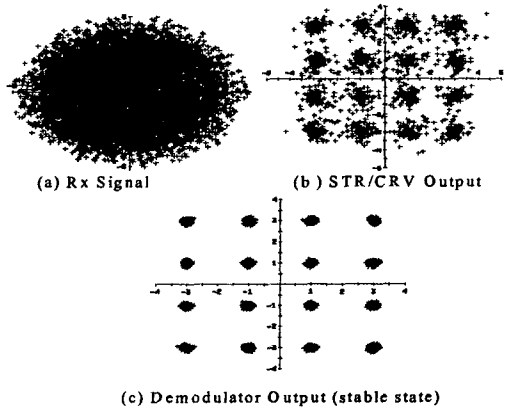


Figure 11. Implemented Modem chip output signal

## 4. Conclusion

So far, we described the overview of 26GHz BWA system in KOREA , design and implementation of the 16-QAM modem for FBWA system.

Implemented 16-QAM modem prototype include FPGA chip to digitally modulate and demodulate the signal and AFE to analog processing such as AD conversion, DA conversion and signal filtering. Modem is integrated in one FPGA chip including modulator/demodulator and FEC. The performance of Modem was tested in wireless channel using IFU and RFU via air interface. Implemented Modem have good porformance in wireless channel test. For the future work, we will integrate the MAC protocol chip with Modem chip.

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