A VLSI DESIGN OF CD SIGNAL PROCESSOR for High-Speed CD-ROM

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Abstract : We implemented a CD signal processor operated on a CAV 48-speed CD-ROM drive into a VLSI. The CD signal processor is a mixed mode monolithic IC including servo-processor, data recovery, data-processor, and 1-bit DAC. For servo signal processing, we included a DSP core, while, for CAV mode playback, we adopted a PLL with a wide recovery range. Data processor (DP) was designed to meet the yellow book specification.[2] So, the DP block consists of EFM demodulator, C1/C2 ECC block, audio processor and a block transferring data to an ATAPI chip. A modified Euclid's algorithm was used as a key equation solver for the ECC block. To achieve the high-speed decoding, the RS decoder is operated by a pipelined method. Audio playability is increased by playing a CD-DA disc at the speed of 12X or 16X. For this, subcode sync and data are processed in the same way as main data processing.

The overall performance of IC is verified by measuring a transfer rate from the innermost area of disc to the outermost area. At 48-speed, the operating frequency is 210 MHz, and this chip is fabricated by 0.35 um STD90 cell library of Samsung Electronics.

1. INTRODUCTION

The CD-DA has been one of the most widely used consumer products since it was announced in 1982 by Sony/Philips.[1] In 1984, the yellow book for CD-ROM was disclosed. Currently, the speed of a CD-ROM Drive is about 50X. Of late, the integration of chips in a CD-ROM drive is a major concern. So, we integrated the CD signal processor into a single chip for a high-speed CD-ROM.

2. THE INTRODUCTION OF CD SIGNAL PROCESSOR

A block diagram of a CD-ROM drive is shown in figure 1.

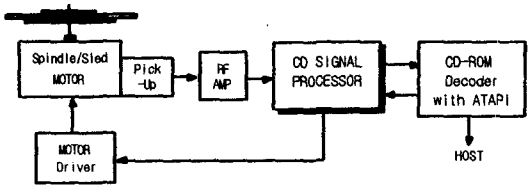

Figure 1. The Block Diagram of CD ROM Drive System

The signal read by pick-up is amplified by an RF AMP, and transferred to a CD signal processor. After processing, the signal is transferred to the host via ATAPI. In figure 2, a block diagram of a CD signal processor is illustrated.

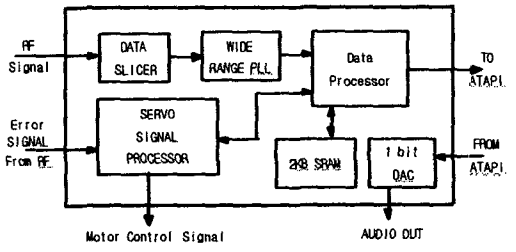

Figure 2. The block diagram of CD signal processor

In this paper, we focused on an implementation of the data processor. Digital servo block including DSP core functions as focusing, sled, tracking and spindle servo respectively. Data slicing block of a data recovery part employs a duty feedback method to shape an RF signal into a rectangular waveform. PLL block has a wide recovery range for CAV mode. The data and clock from data recovery are fed into EFM demodulator. After error correction, the signals

are transferred to CD-ROM decoder chip with ATAPI I/F.

3. THE HARDWARE IMPLEMENTATION OF DATA PROCESSOR

A block diagram of a data processor in the CD signal processor is illustrated in figure 3

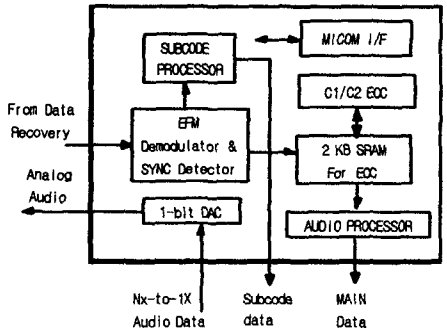

Figure 3. The block diagram of data processor in CD signal processor

3.1 EFM demodulator and sync signal processing block

The signal from data recovery is demodulated in EFM demodulator from 14 bits to 8 bits according to red book.[1] We used a translation table for EFM demodulation. In the sync signal processing block, by protection and insertion functions, data sync and subcode sync signals are correctly detected. The sync signals are used as reference signals for signal processing. The demodulated data is stored in 2 KB SRAM included in the chip

3.2 C1/C2 ECC block

The demodulated data stored in 2 KB SRAM is read by a deinterleaving method according to red book[1] for C1/C2 ECC. CD data is doubly encoded by C1 (28,24,5) and C2 (32,28,5). In this chip, we used a modified Euclid's algorithm for solving a key equation of a RS decoder. This algorithm simultaneously obtains errata locator polynomial $\sigma(x)$ and errata evaluator polynomial $\omega(x)$.[3] In figure 4, a block diagram of a RS decoder using in this chip is shown.[3]

The RS decoding method has been widely researched.[3-5] The decoding process is as follows : 1) syndrome calculation and erasure flag

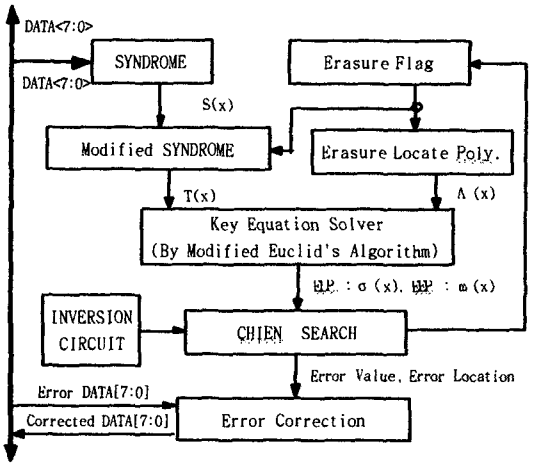

Figure 4. The C1/C2 ECC BLOCK Diagram

Power calculation 2) Forney syndrome and erasure locator polynomial calculation 3) ELP $\sigma(x)$ and EEP $\omega(x)$ calculation 4) error location calculation by Chien search and error value calculation by Forney algorithm 5) error correction.[3]

In C1 mode, the maximum error correction capability is 2, and in C2 mode, maximum 4 erasures can be corrected. In C2 erasure mode, erasure bits are a C1 codeword error flag which is generated when errors occur exceeding C1 codeword error correction capability. The C1 error flag is determined in Chien search block. When C2 codeword error exceeds its correction capability, the output error flag is copied from C1 error flag for audio interpolation.

The operation time of C1/C2 ECC stage is dependent on its syndrome calculation time and Chien search time determined by its codeword length. For a high-speed CD-ROM drive, we used a pipelined RS decoding method. The pipeline flow of ECC block is displayed in figure 5.

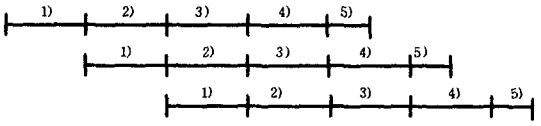

Figure 5. The pipeline flow of ECC BLOCK

3.3 Interpolation and data transfer block

In CD-ROM mode, the interpolation block is turned off, but in CD-DA mode, the interpolation operation is turned on to eliminate high frequency noise. The interpolation is executed by the output error flag of ECC block. The interpolated data is

formatted according to CD-DA or CD-ROM specification [1-2] and transferred to ATAPI chip together with error flag.

3.4 Subcode processor and Audio playback

The EFM data consists of 33 bytes. After EFM processing, the EFM data is divided into 32 bytes main data and 1 byte subcode data. The subcode data contains time information such as minute, second, frame and the subcode period is 98 EFM frame. The output of a data processor is 24 bytes/frame, so 98*24=2352 bytes is the same as 1 sector data in CD-ROM decoder. In CD-ROM format, the 1 sector data has a synchronization signal and header information, by which the data is processed. In CD-DA format, however, the 2352 bytes is a raw data which doesn't contain any sync and information data. So the data can be directly played via 1 bit DAC.

In CD-ROM Drive, CD-DA data is read at n-X speed and the read data is stored in the external DRAM of CD-ROM decoder. The stored data is played at 1-X speed. By this method, the CD-ROM drive can drastically improve audio playability in a defect disc. When track jump occurs, there should be data stream continuity between the previously stored data and the currently storing data. When the continuity breaks, the audio-output in 1 bit-DAC generates a high frequency noise. We call this noise as an audio buffering noise. In CD-DA mode, when data is buffered into CD-ROM decoder, we use a subcode sync signal as a reference signal for buffering start at each sector as the data doesn't have a sync signal. When track jump occurs, main data and subcode sync are not synchronized as the subcode signal is processed by WFCK. Main data is written by WFCK and read by RFCK in 2 KB SRAM. The waveform of this situation is shown in figure 6.

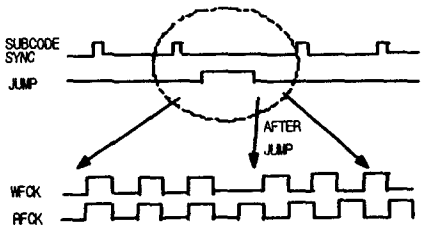

Figure 6. The waveform of Subcode Sync and Read/Write Clock

In this waveform, the WFCK and the RFCK have the same clock source made by channel clock and their period is a 1 EFM frame. But the WFCK has a phase discontinuity when jump occurs. As a result, the audio-output data has an audio buffering noise.

To eliminate this noise, we added a buffer for subcode data and sync signal. This buffer has the same clock system as a main data processing block. The block diagram of this buffer is displayed in figure 7.

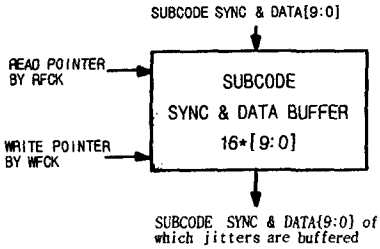

Figure 7. The block diagram of SUBCODE Data & Sync

By this, in CD-DA data buffering mode, the subcode sync and main data have a synchronized relation. So we achieved an elimination of audio buffering noise and a high audio playability in a defect disc.

4. Verification and Result

This chip was successfully operated at CAV 48X speed. The buffering method of subcode data and sync achieved a good audio playability at max 3.0 mm defect. In error correction capability as well, max 2.0 mm defect disc is corrected without any error flag signal. In figure 8, an error correction capability and an audio playability are verified by showing a relation between a defected RF signal and output audio signal of which errors are corrected.

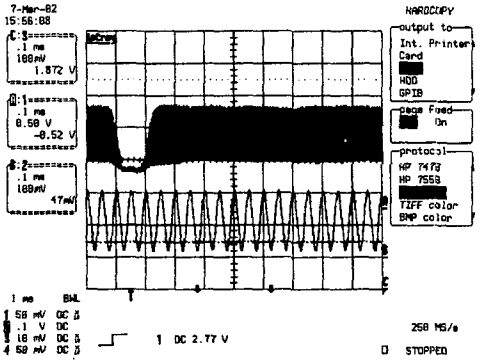

Figure 8. The defected RF signal and output audio signal of which errors are corrected

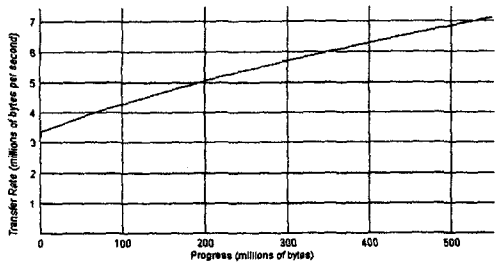

Figure 9. The Transfer rate of CD Signal Processor using winbench-99 DISC in CD-ROM drive from innermost area to outermost one of a disc

Figure 9. displays an overall performance of a CD signal processor. It is a transfer rate graph from innermost area to outermost one of a disc. At CAV 48X speed, we verified that data transfer rate has over 7200KB/sec.

5. Conclusion

This chip was successfully operated at CAV 48X speed and fabricated by 0.35 um process of Samsung Electronics, consisting of servo, data recovery, data processor. The CD data processor uses a modified Euclid's algorithm for solving a key equation for RS decoding. To improve audio playability, CD-DA disc is read at 12X or 16X speed. In subcode processing block, we adopted a subcode buffer for synchronizing main data with subcode sync. By this proposed method, we played a CD-DA disc without audio buffering noise and achieved a good audio playability. In this chip, the logic block is tested by scan and function vector, and the memory part is tested by bist method. The chip photograph is shown in figure 10.

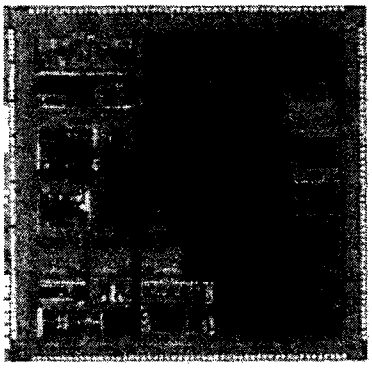

Figure 10. The chip photograph of a CD signal processor

REFERENCES

[1] SONY CORP, N.V. PHILIPS, "compact disc digital audio," SEPTEMBER, 1982

[2] SONY CORP, N.V. PHILIPS, "compact disc read only memory," JUNE, 1984

[3] Stephen B. Wicker, " Error Control Systems for digital communication and storage," Prentice hall, 1995

[4] Howard M. Shao, T.K. Truong, Leslie J. Deutsch, Joseph H. Yuen, and I.S. Reed, " A VLSI Design of a Pipeline Reed-Solomon Decoder," IEEE, Transaction on Computers, VOL C-34, NO. 5, MAY 1985.

[5] Howard M.Shao and Irving S. Reed, "On the VLSI Design of a Pipeline Reed-Solomon Decoder Using Systolic Arrays," IEEE Transaction on Computers, VOL. 37, NO. 10, October 1988.