A MPEG-4 Video Codec Chip with Low Power Scheme for Mobile Application

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Abstract

In this paper, we present a design of mpeg-4 video codec chip to reduce the power consumption using frame level clock gating and motion estimation skip scheme. It performs 30 frames/s of codec (encoding and decoding) mode with quarter-common intermediate format(QCIF) at 27MHz. A novel low-power techniques were implemented in architectural level, which is 35% of the power dissipation for a conventional CMOS design. This chip performs MPEG-4 Simple Profile Level 2(Simple@L2) and H.263 base mode. Its contains 388,885 gates, 662k bits memory, and the chip size was 9.7 mm x 9.7 mm which was fabricated using 0.35 micron 3-layers metal CMOS technology.

1. Introduction

Recently, the market for portable multimedia applications, such as MPEG video camera, wireless videophone, and portable wireless multimedia terminal, has been on the rise. Video/audio processors are essential to make this multimedia system high performance, low cost and low power consumption. These processors can be widely used to implement multimedia application such as JPEG (Joint Photographic Expert Group), H.261, H.263, MPEG, G.723, H.324, and other data compress standards. An MPEG-4 Simple Profile video codec core with extremely low power dissipation meets the growing demands for low-cost implementation of such terminals [1].

These applications requires low power consumption and to reduce memory bandwidth access. During compression, the largest portion of power is consumed in the motion estimation part, which requires a huge amount of computation. Most of these video compression standards are based on the DPCM method, which incorporates motion estimation (ME) and motion compensation (MC) techniques. Among all the methods required for a typical video coder, the ME module is the most power demanding it consumes almost 50% of the power needed for the entire system [3]. Several ME algorithm have been proposed [3-5]. But proposed algorithms are not adaptive architecture for implementation as VLSI.

we present a design of mpeg-4 video codec chip to reduce the power consumption using frame level clock gating and motion estimation skip scheme. The frame level clock gating scheme is to reduce power dissipation on architectural level and the others is to reduce the power consumption using motion estimation skip method. This method comprised first and second units. The first search is conducted with a motion estimation skip, which is motion vector prediction and motion compensation with previous parameters. In all test sequence performed, this reduced computation load to 32% that of conventional two-step methods with respect to that of a MPEG models.

This paper presents the MPEG-4 video codec with architecture and low-power techniques. Section II describes architecture of the MPEG-4 video codec. In Sections III and IV, low-power schemes employed in the MPEG4 video codec design are discussed. Verification and chip implementation are presented in Sections V and VI, respectively.

2. Architecture Overview of MPEG-4 Video Codec Chip

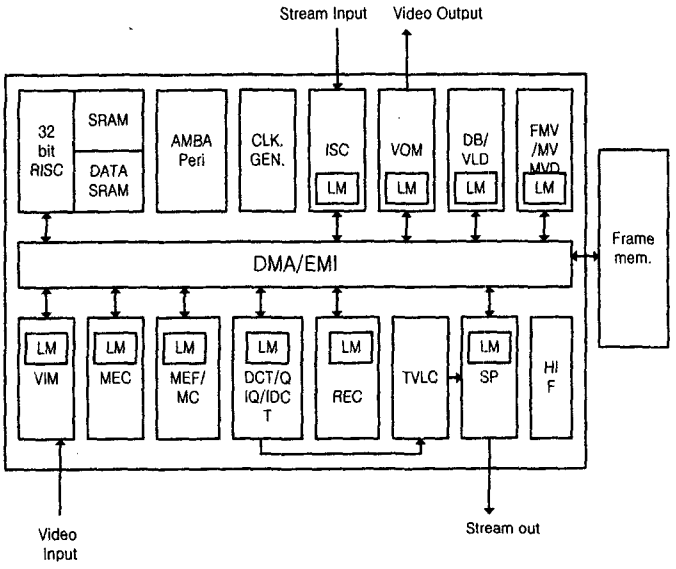


Fig. 1. Block diagram of the Chip

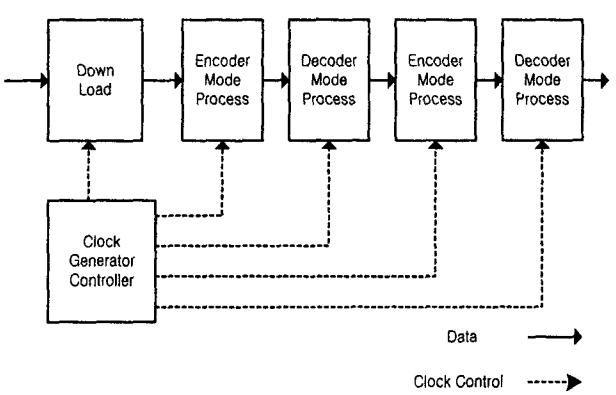
Fig. 1. shows a block diagram of the chip. An MPEG4 codec VLSI consist of 16Mb synchronous DRAM, to accumulate image data, and microprocessor to control video stream, host parameters. The chip is composed of 32-bit RISC processor and dedicated hardware engines. The dedicated engines are implemented for fixed functions in MPEG4, such as video input module(VIM), motion estimation coarse(MEC), motion estimation fine/motion compensation(MEF/MC), discrete cosine transform(DCT), inverse DCT(IDCT), reconstruction(REC), texture variable length coding(TVLC), stream producer(SP), host interface(HIF), clock generator(CLKGEN), input stream control(ISC), video output module(VOM), deblocking(DB), variable length decoding(VLD), four motion vector(FMV), and motion vector motion vector differential(MVMVD). The local memories(LM) reduce access to the external memory and power dissipation. The total size is 18 kbyte,

which has a small area and reduced power consumption. 16Mbits external frame memory is connected to the external memory interface(EMI) with direct memory access(DMA) controller. The DMA controller can transfer data among local memories and access external memory for one cycle.

RISC is a 32-bit ARM7TDMI processor with five-stage pilelining at encoding mode and four-stage pilelining at decoding mode. It access 48-kB instruction memory in which the whole firmware program is stored. The RISC processor executes scheduler, rate control, error concealment, syntax synthesis, and syntax parsing.

A motion-estimation module consist of a mixed mode coarse resolution and a motion-estimation module in fine resolution. A mixed mode motion estimation is hierarchical search and motion estimation skip. The search area of the motion estimation is +/-15.5, and support unrestricted mode. The DCT/IDCT module has 1-bit serial distributed arithmetic method with AC/DC prediction function. VLC module consists of TVLC, HVLC, and SP. TVLC performs texture coding processing. HVLC executes the header bit and motion vector synthesis. The VLD module has a LVLD and HVLD. The low variable length decoding (LVLD) is parsing of the texture bits of decoding input stream. The high variable length decoding (HVLD) is an analysis of header bits and motion vector streams. It is supports the reversible VLC, the data partition, and data re-sync processing. Error resilience can be improved for both random and burst errors, in particular in wireless communications. Hardware performance is designed such that both MPEG-4 codec with QCIF format at 30 frames/s can be carried out at 27 MHz.

3. Low Power Design of Frame Level Clock Gating



ig. 2. Data flow of codec mode operation.

gure 2 show data flow of codec mode operation at QCIF. ata flow is image down load, firstly, and then encoder and :coder operation, repeated. These operation is ntrolled by clock generator controller. This operation is a quence operation with clock gating control and does not nultaneous operation. Totally, it is roughly estimated the ime clock-gating achieves 20% power saving.

4. Mixed Mode Motion Estimation Coarse

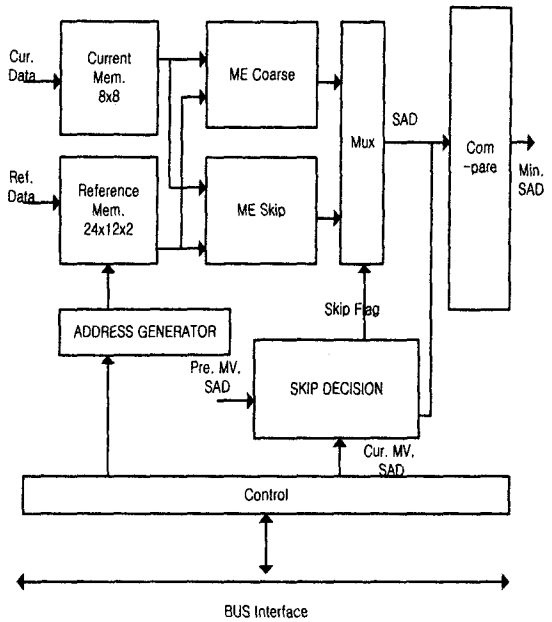


Fig. 3. Block Diagram Motion Estimation

Fig. 3. shows a block diagram of the motion estimation. To reduce the logic gate and local memory size, only 640 byte are used as ME coarse inputs. ME coarse computes summation of absolute differences (SAD) with 8 processing elements(PE). ME skip unit computes SAD with one PE. A mixed mode motion estimation for moving image encoding determines a motion vector by comparing a target block to sets of blocks selected according to the results of previous comparison. The mixed mode motion estimation indicated by previous comparison to be similar to the target block and thereby reduced the number of comparison and the search time required to find a motion vector. This method described here is on the motion estimation using motion estimation skip and hierarchical search(2:1 sampling) for image compression. We proposed a design method of motion estimation with motion estimation skip. The proposed hardware consists of reference data down sampling block, current data down sampling block, demultiplex, two reference memory, current memory, processing elements array, motion estimation skip, motion estimation skip processing block and comparator (fig. 3.).

The mixed mode motion estimation operated as follows.

First.

1. Three Motion Vectors (B,C, and A) inputs motion vectors for motion vector prediction.
1. To calculation for motion vectors gets median value among inputs vectors.
2. To run motion compensation with motion predictor value and current macro block.
3. To get SAD(Sum of Absolute Difference) for motion compensation predictor value.

Second.
1.Three SAD value take a previous macro block, top macro block, top right macro block.
2. To get a maximum SAD from inputs SADs

Third
1.From the first step and the second step.
2.Compare to SADmcp and SADmax
3. if SADmcp is less then SADmax, skip flag is on.

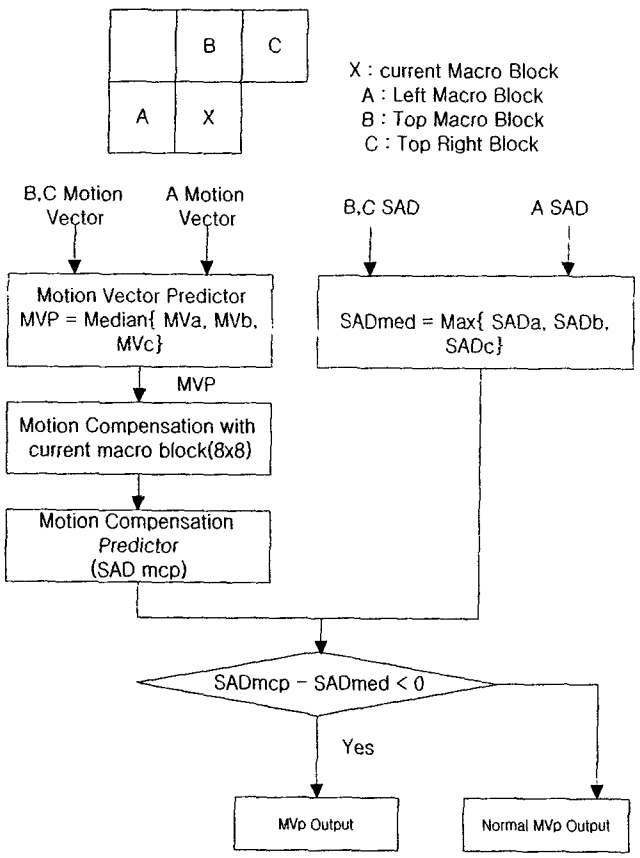


Fig. 4. Motion Estimation Skip Flow Chart

If skip flag is on, motion estimation is not normal operation. If skip flag is off, motion estimation is normal operation.

Motion estimation block diagram for video compression. The motion estimation architecture has a normal mode operation and skip mode operation according to skip decision. This block consists of current memory, reference memory, motion estimation coarse, motion estimation skip, and motion estimation skip decision. Search range is –8/+7 and processing elements are 8^{th}. This architecture has small size memory,(8x8 of current memory, the 576x8 of reference memory), and has low processing elements(8^{th}).

The MPEG-4 Test Sequences are used (QCIF resolution) which are called from class A, B and E of the MPEG-4 test suite to obtain the simulation results. Table 1. shows percentages of disabling calculating the actual operation.

Table 1. Percentage of disabling motion estimation skip

	Carphone	Foreman	Coast	Stefan
QCIF (176x144)	30 %	24.6%	36.7%	37.4%
PSNR	32.59 dB	31.67 dB	29.00 dB	23.94 dB

In all test sequences performed, this reduced computation load to 32% that of conventional two-step methods while maintaining average SNR < -0.1 dB with respect to that of an MPEG test model.

5. Verification Methodology

The top-down ASIC design begins with an ASIC requirement specification, followed by the behavioral verification of system/ASIC algorithms. Design verification and methodology was developed by us. We developed C models for major functional blocks of the MPEG-4 video codec and performed high level simulation. Also we modeled external environment using VHDL, which are ARM system, ARM Bridge, and synchronous dynamic access memory (SDRAM).

Simulation and testing for the result of the software and the hardware are carried using co-simulation environment. The test vectors for high-level simulation are used for verification from RTL-level VHDL simulation through gate-level simulation. We tested board level for function level verification as shown figure 5.

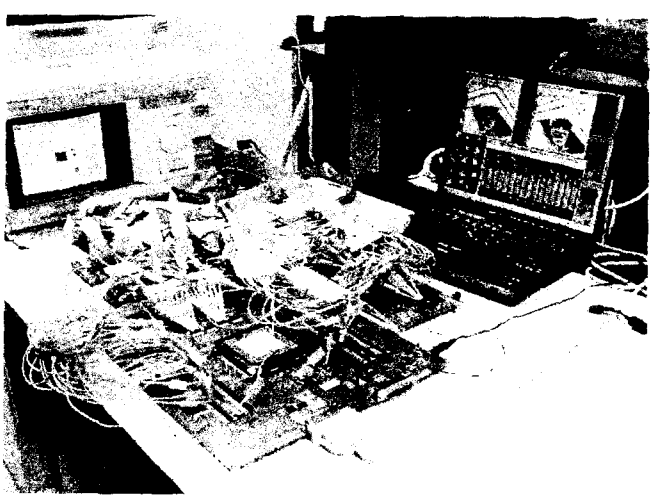


Fig. 5. Verification Board System

6. Conclusion

In this paper, we present a design of mpeg-4 video codec chip to reduce the power consumption using frame level clock gating and motion estimation skip scheme. It performs 30 frames/s of codec (encoding and decoding) mode with quarter-common intermediate format(QCIF) at 27MHz. Novel low-power techniques were implemented in architectural level, which is 35% of the power dissipation for a conventional CMOS design.

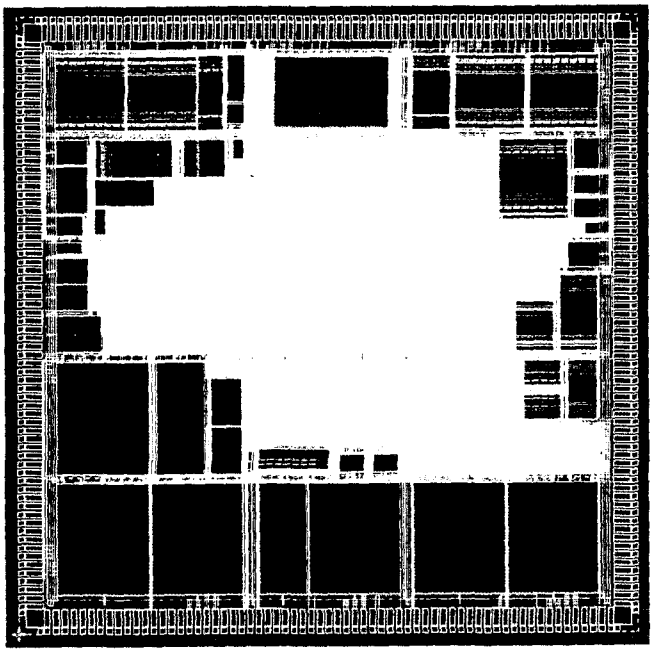


Fig. 6. MPEG-4 Chip layout photography

This chip performs MPEG-4 Simple Profile Level 2(Simple@L2) and H.263 base mode.

Its contains 388,885 gates, 662k bits memory, and the chip size was 9.7 mm x 9.7 mm which was fabricated using 0.35 micron 3-layers metal CMOS technology. Fig. 5 shows verification system and fig. 6 shows a microphotograph.

References

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