A High Gain V-band CPW Low Noise Amplifier

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Abstract: A V-band low-noise amplifiers (LNA) based on the Millimeter-wave monolithic integrated circuit (MIMIC) technology were fabricated using high performance 0.1 ㎛ Γ-shaped pseudomorphic high electron mobility transistors (PHEMT's), coplanar waveguide (CPW) structures and the integrated process for passive and active devices. The low-noise designs resulted in a two-stage MIMIC LNA with a high S_{21} gain of 14.9 dB and a good matching at 60 GHz. 20 dBm of IP3 and 3.9 dB of minimum noise figure were also obtained from the LNA. The 2-stage LNA was designed in a chip size of 2.3 × 1.4 mm^2 by using 70 ㎛ × 2 PHEMT's. These results demonstrate that a good low-noise performance and simultaneously with a high gain performance is achievable with GaAs PHEMT's in the 60 GHz band.

1. Introduction

Millimeter-waves are expected to be in high demand for wireless communication services because they can provide an extremely wide bandwidth with the frequency reuse characteristics [1-2]. A frequency band including 60 GHz, the V-band, is considered to be one of the strong candidates for wireless local area network (WLAN) applications both in household and office environments due to its unique feature of strong signal attenuation under oxygen ambient [3]. One of the keys to the successful implementation of the millimeter-wave technology for these applications is to demonstrate reliable and cost-competitive modules. For this goal, the millimeter-wave monolithic integrated circuit is believed to be a very promising solution. In this study, we have demonstrated a low-noise amplifier MIMIC in V-band.

2. Design

The LNA was implemented using CPW transmission lines. A CPW technology does not require the thinning of the substrate, via holes or backside metallization process, which can increase process yield and decrease chip costs compared with microstrip technology. For better accuracy of designed circuit simulations, we used Momentum simulations in conjunction with experimental test patterns to develop various models of co-planar structures such as bias lines, signal lines, coupled lines and so forth. We also modeled impedance lines of 35, 50, 70 Ω, and discontinuities. These developed models enabled us to successfully design the MIMIC's. The S-parameter data from the measurements and the modelings are compared in figure 1.

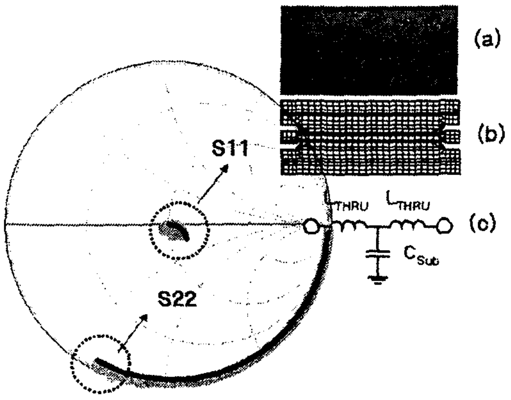

Figure 1. Comparison of measured (-) with modeled (O) S-parameters. (a) is fabricated 50 Ω CPW thru line, (b) is simulated 50 Ω CPW thru line and (c) is modeled 50 Ω CPW thru line.

Various coplanar stubs with passive components were also simulated for s-parameters. One of the simulated structures, the biasing network with bypass capacitors and resistors, is illustrated in figure 2.

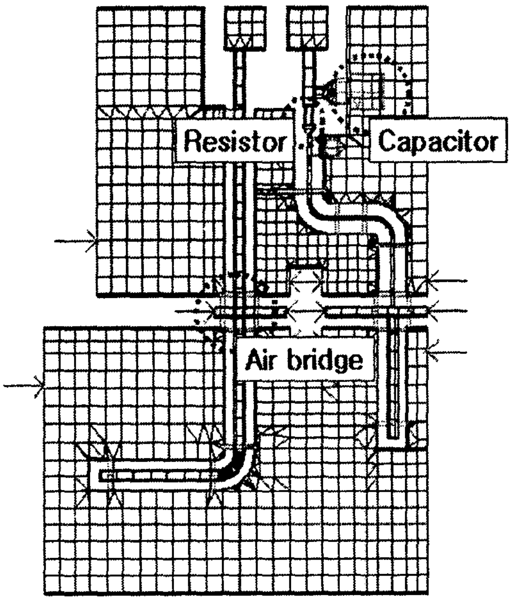

Figure 2. Example of momentum simulation for the CPW line and the passive component.

A 600 Å NiCr resistor and 1000 Å Si_3N_4 for MIM capacitors were used at the RF input and the output of the chip for dc block and bypass. Measured thin film resistors had 50.2 ~ 50.9 ohm/□ of resistance, and MIM capacitor 0.485 ~ 0.538 fF/㎛^{2} of capacitance [4-5].

A V-band MIMIC LNA was fabricated on a GaAs substrate employing a 0.1-㎛ Γ-gate PHEMT technology [6]. The device showed a good pinch-off voltage (V_p) of -1.75 V, a knee voltage (V_k) of 0.6 V and a drain-source saturation current (I_{dss}) of 63 mA (450 mA/mm), respectively. At a drain-source voltage (V_{ds}) of 1.5 V and a gate-source voltage (V_{gs}) of -0.7 V, a maximum transconductance (g_m) of 500 mS/mm was obtained. RF characteristics were measured in the frequency range of 1 ~ 50 GHz. At 50 GHz, an S_{21} gain of 3.9 dB was measured. A unit current-gain cut-off frequency (f_T) of 113 GHz and a maximum frequency of oscillation (f_{max}) of 180 GHz were estimated by extrapolating, the S-parameters. The small-signal HEMT parameters were extracted from the S-parameters measured up to 75 GHz. The parasitic components including gate resistance (R_g) were determined by cold-FET measurements [7-8]. Figure 3 shows the fabricated 0.1-㎛ Γ-gate PHEMT.

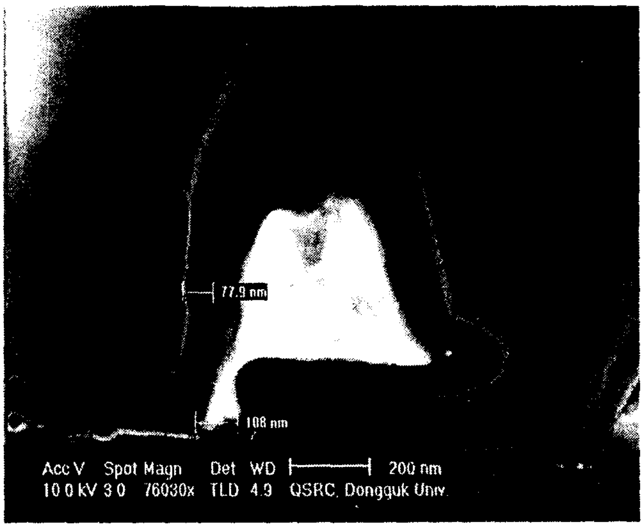

Figure 3. The fabricated 0.1-㎛ Γ-gate PHEMT.

Figure 4 shows the schematic of the 2-stage V-band LNA MIMIC. The input and the output ports were designed to have a good matching with 50 Ω loads to sustain a sufficient load power at high frequencies. Moreover, short-stub CPW's were added at the input ports to prevent a potential oscillation at low frequencies, and to enhance the matching characteristics. The length of the bias lines was set to one quarter of the wavelength of the 60 GHz electromagnetic waves to minimize the signal loss. Thin-film resistors were placed to enhance the circuit stability. To fabricate the V-band LNA MIMIC, a mask set of 7 layers was used. Figure 5 shows the fabricated MIMIC. The chip size was 2.3 × 1.4 mm^2.

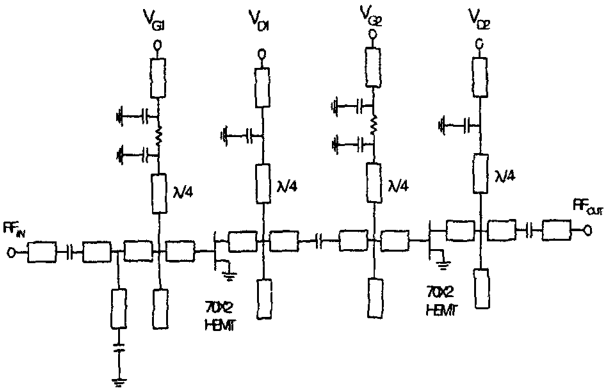

Figure 4. A schematic of the designed 2-stage V-band LNA MIMIC.

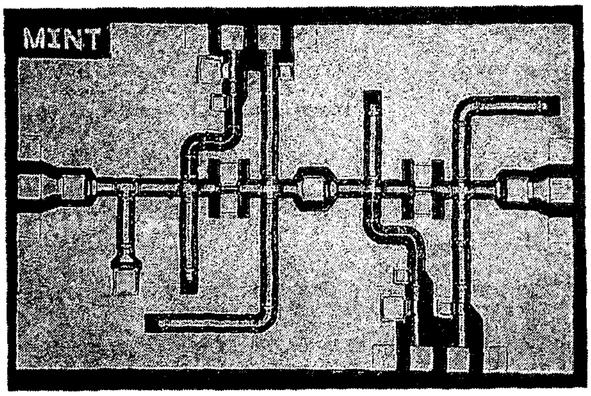

Figure 5. The fabricated V-band LNA MIMIC.

3. Performance

The performance of the V-band LNA was examined using the on-wafer probing and an Agilent V-band test set. Input and output matching characteristics were measured by an 8510C network analyzer. The S-parameters and the power measurement results are shown in figures 6 and 7, respectively. As shown in figure 6, S_{11} and S_{22} matching were slightly shifted by approximately 2 GHz from the target frequency, which is believed to be due to the variation of MIMIC process parameters. However, the LNA showed a high S_{21} gain of 14.9 dB at 60 GHz, which is attributed to the high performance of the PHEMT's and the optimized LNA design. P_{1dB} of the LNA was estimated from the measurements of the output power and the power gain at various input powers. As shown in figure 7, an output power of 1 dBm was obtained at an input power of -10 dBm.

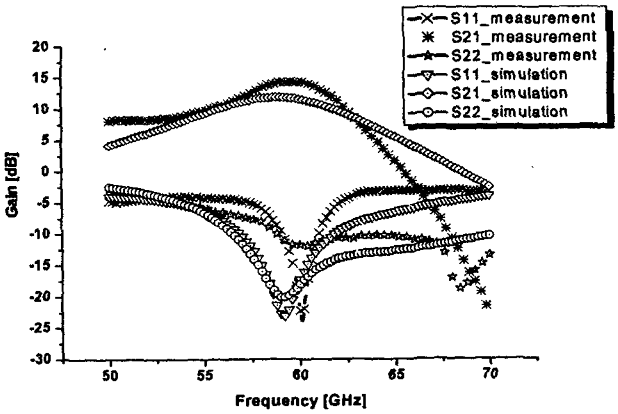

Figure 6. Comparison of measured (-) with simulated (O) S-parameters.

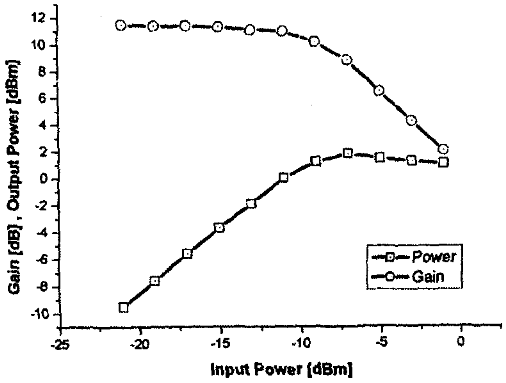

Figure 7. Results of the power measurement.

Figures 8 and 9 show that our typical LNA exhibits a 3rd order intercept point (IP3) of 20 dBm and a minimum noise figure (NF_{min}) of 3.9 dB at 52 GHz.

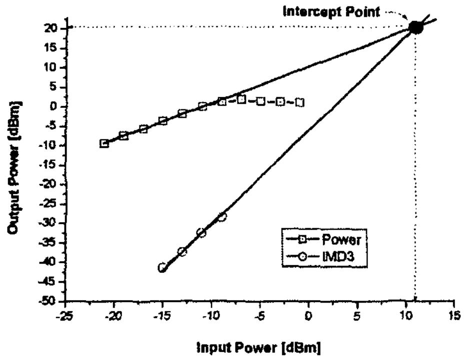

Figure 8. Results of the 3rd order intercept point (IP3) measurement.

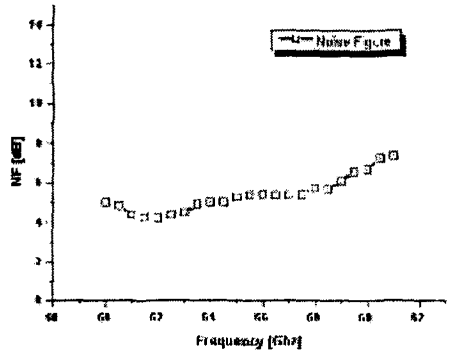

Figure 9. Results of the minimum noise figure (NF_{min}) measurement.

4. Conclusion

V-band MIMIC LNA's were designed and fabricated. The devices showed a high S_{21} gain of 14.9 dB at 60 GHz due to the high performance of the PHMET's and an optimized LNA design. The MIMIC circuit was fabricated in a 2.3 × 1.4 mm^2 chip size by integrating the 2-stage 0.1 ㎛ Γ-gate PHEMT's, the CPW structures and many other passive devices. The V-band MIMIC library was established based upon the measurement and modeling parameters of the active and passive device components. By using our established MIMIC library, the LNA was designed to have good matching and stability at 60 GHz. The fabricated LNA showed a good S_{21} matching and a maximum gain at 60 GHz. 20 dBm of IP3 and 3.9 dB of NF_{min} were also achieved from the LNA.

Acknowledgement

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REFERENCES

[1] H-L. A. Hung et al., "60-GHz GaAs MMIC low-noise amplifiers," in *Proc. IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp.*, May 1988, pp. 87-90.

[2] J. Brenz et al., "44-GHz monolithic low-noise amplifier," in *Proc. IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp.*, May 1987, pp. 15-18

[3] Skolnik, M.I., "Millimeter and Submillimeter Wave Application." *Proceedings of the Symposium on Submillimeter Waves,* Polytechnic Press of Poly. Institute of Brooklyn, New York, 1970, pp. 9-25

[4] J. W. Shin, Y. S. Yoon, S. D. Lee, H. C. Park, and J, K. Rhee, "Effect of He gas on hydrogen content and passivation of GaAs PHEMT with SiN film", *Asia-Pacific Workshop on Funddamental and Application of Advanced Semiconductor Devices*, pp. 121-124, 2000.

[5] Il-Hyeong Lee, Seong-Dae Lee, and Jin-Koo Rhee, "Studies on Air-Bridge Processes for mm-wave MMIC's Applications", *Journal of the Korean Physical Society,* 35(12), pp. S1043-S1046, 1999.

[6] W. S. Sul, D. H. Shin and J. K. Rhee, "Sub 0.1 μm asymmetric Γ-gate PHEMT process using electron beam lithography," *Materials Research Society*, 2002

[7] D. S. Park, H. C. Cho, Y. S. Chae, J. K. Rhee, "A New Cold PHEMT Equivalent Circuit for Extracting Extrinsic Resistance", *Asia-Pacific Workshop on Fundamental and Application of Advanced Semiconductor Devices*, pp. 115-119, 2000.

[8] G. Dambrine, A. cappy, F. Heliodore and E. Playez, "A New Method of Determining the FET Small-Signal Equivalent Circuit," *IEEE Trans. Microwave Theory & Technique,* Vol. 36, No. 7, pp. 1151-1159, 1988