A Study on the Hot Carrier Effect Improvement by HLDBD (High-temperature Low pressure Dielectric Buffered Deposition)

Lee Yong-Hui*, Kim Hyeon- Ho**,
Woo Kyong-Whan***, Kim Hyeon- Ki****, Yi Jae-Young*****, Yi Cheon-Hee******

Shinsung College, Division of Computer Application*, Chung-buck Provincial Univ. of Science & Technology. Dept of Electronic Information.**, Woosong Technical College. Dept of Internet Office***, Keukdong College, Dept of Electronic Telecommunication****, Technical University of Budapest, Dept of Control Engineering & Informatics*****, Chong-ju University , Dept of Electronic Engineering.

36 NAEDOK-DONG, SANGDANG-GU CHONGJU-SHI,
REPUBLIC OF KOREA(Zip code : 360-764)

Phone : +82-43-229-8448
Fax : +82-43-213-6392
E-mail : yicheon@chongju.ac.kr

Abstract

The scaling of device dimension and supply voltage with high performance and reliability has been the main subject in the evolution of VLSI technology. The MOSFET structures become susceptible to high field related reliability problems such as hot-electron induced device degradation and dielectric breakdown. HLDBD(HLD Buffered Deposition) is used to decrease junction electric field in this paper. Also we compared the hot carrier characteristics of HLDBD and conventional.[

1. Introduction

The scaling of device parameters such as channel length(Leff), oxide thickness(Tox), junction depth(Xj) and supply voltage(Vdd) results in the significant changes in performance and reliability characteristics of devices and circuits. Without scaling rules, it has been very difficult to satisfy complex requirement, hence, scaling theory has been introduced to guideline the design of device parameters. The first scaling theory maintains the electric field constant, i.e. both horizontal and vertical dimensions and supply voltage are scaled by a factor S(S>1) in order to maintain constant electric field within MOSFET[1].

The MOSFET structures become susceptible to high field related reliability problems such as hot-electron induced device degradation and dielectric breakdown. As a solution to reduce the hot carriers, new hot-carrier resistant structures such as the DDD(Double Diffused Drain)[2] and LDD(Lightly Doped Drain) structures[3] have been introduced. The LDD type structure has been successfully used in 4Mb, 16Mb, 64Mb, 256Mb DRAM devices with gate length 0.15~0.40um[4]. However, even using LDD, it is difficult to achieve high reliability and high performance at a 5volt power supply. For this reason, power supply voltage reduced to under 5volt, for example, to 3.3volt. Up to this time, the selection of optimal power supply voltage was based on optimizing the trade off between operation speed and reliability. An important

point is that most important parameter controlling power consumption is the supply voltage. The selection of optimal power supply voltage is now based on optimizing the trade off between operation speed and power consumption. In order not to lose operation speed by reducing power supply voltage, threshold voltage should be reduced. The increase of threshold voltage and capacitance limits the performance of circuit at low voltage operation, and the advantage in delay time due to reduction of channel length is diminished. To overcome this problems, it is very important to design a vertical doping profile of substrate structure, hence, the concept of substrate engineering was introduced[5].

HLDBD(HLD Buffered Deposition) is used to decrease junction electric field in this paper. HLDBD process is performed after first gate etch, deposit HLD layer and followed n-type minor ion implantation. To confirm this, we simulate the basic experimental items. For the comparison of junction profile after full process and concentration profile just after n-type minor implantation, process simulation corresponding to each splitting condition was performed. At the bias condition of fully charged state, the variation of electric field across the junction, according to each process scheme, was presented.

2. Fabrication.

HLDBD is used to decrease junction electric field. HLD process is performed after FG etch, and followed NM1 ion implantation. To confirm this, we simulate the basic experimental items.

For the comparison of junction profile after full process and concentration profile just after NM1 implantation, process simulation corresponding to each splitting condition was performed. At the bias condition of fully charged state, the variation of electric field across the junction, according to each process scheme, was presented. Figure 1 shows the comparison conventional structure and HLDBD structure. New HLDBD structure has HLD layer to decrease electric field.

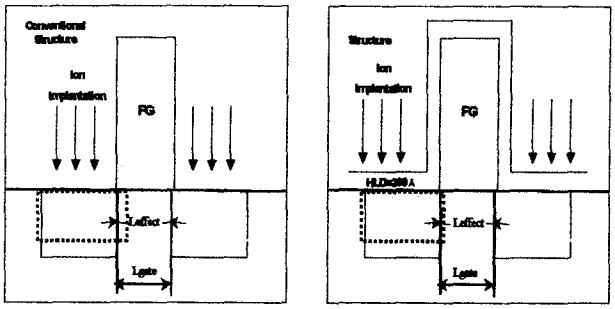


Figure 1. Comparison conventional structure

Buffer oxide and SiN layer were deposited and etched the field area for active area definition. Trench etching was performed(in depth=3000Å) after thin SiN layer was etched. Slight oxidation of trench sidewall was formed(1050℃, 100Å) to eliminate the defect which might be occurred during the trench etching step. Filling the trench gap with HDP(High Density Plasma) oxide, and densification at high temperature, then CMP was carried out for planarization. SiN and pad oxide were removed by 99HF 60"+Phorporic acid 75' and U10'+19HF 45", respectively. The gate electrode was patterned by the KrF lithography. The following nLDD ion implantation carried out with As+P nLDD with/without HLDBD layer. Then 65nm Si_3N_4 sidewall spacer was formed and then deep source /drain implantation(As) was carried out. The final process was RTA annealing at 1000℃ for 10seconds(to activate arsenic ions). And bit-line, capacitor, metalization, and annealing process performed.

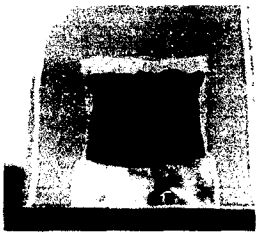


Figure 2. Conventional LDD structure

Figure2 and Figure3 represent the final fabrication image by TEM, respectively conventional and HLDBD

structure. In this figure we can observed HLDBD layer.

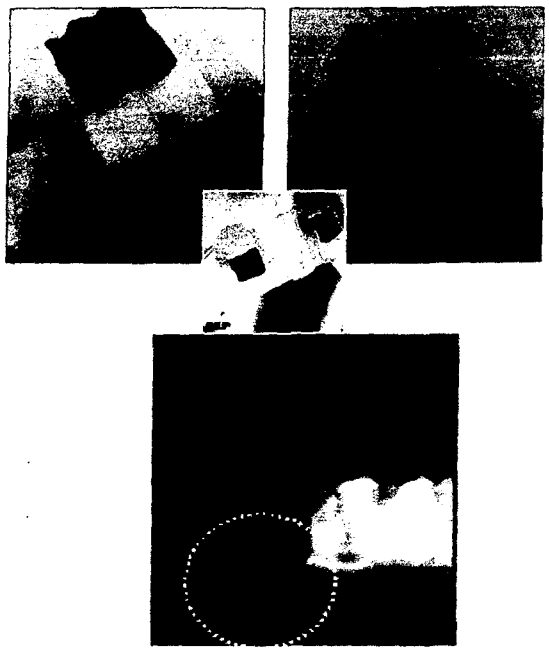


Figure 3. HLDBD structure

3. Experimental and Discussion.

In spite of the impressive advances in MOSFET device minimization during the last three decades, device optimization criteria for reliability are not still well established. The original equation for substrate current(I_{SUB}) based on lucky electron model can model the substrate current properly. However, the functional form of this formulation is inconvenient for device characterization and design. It is widely used a bell-shaped plot to characterize the substrate current by plotting I_{SUB} against gate voltage with drain voltage as a parameter. The initial rise is due to the increase of drain current and the fall is due to the decrease of channel electric field. The substrate current is result from holes generated by impact ionization, hence, it is a measure of hot electron currents in the channel. The original equations properly model the substrate currents and drain saturation voltage[6][7].

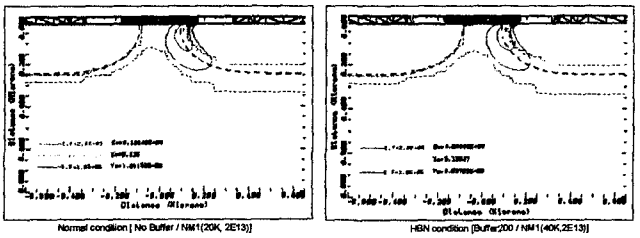
However, the functional form of these equations is inconvenient for design criteria. The minimization of substrate current and drain saturation voltage while maximizing drain saturation current is important in device design. Hot carrier induced interface state generation is a major reliability concern for modern short channel nMOSFET's. Since this is one of the major problems for device scaling, there have been numerous papers. However, the exact time dependence of the degradation is not still well understood. As far as the authors know, the following simple power-law dependence on both stress time and substrate current is perhaps the only model which used to fit the empirical behavior of degradation[8].

$$\Delta = C \quad (I_{SUB}/ID)m*(ID*t/W)n \quad \text{----------(1)}$$

Here Δrepresents the hot carrier induced degradation, which is the function of interface state density in the damaged region. In this equation, C is a proportional constant, W is the effective channel width, I_{SUB} and ID are the substrate and drain current, m and n are the empirical parameters representing the power-low dependence on substrate current and on stress time, respectively.

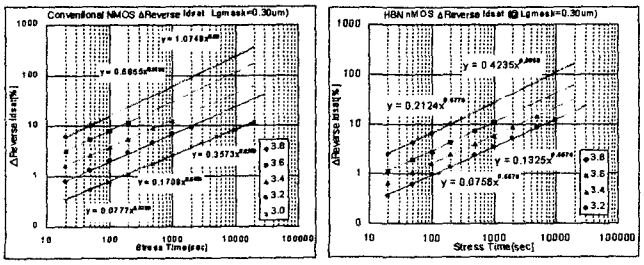
Ids vs. Vd curve used to extract 90% breakdown voltage in various drain voltage sweep. This condition is used to determine to evaluation transistor gate length. Next the gate voltage was determined to extract worst case stress condition. As above mentioned, Isub_max extract method is used to extract worst H.C.E measurement condition. Normally, Vg is 40~50% for Vd. Finally, extract lifetime(τ: 10% degradation time of Idsat) from 1/Vds and Isub/W. Figure 4 shows the simulation of H.C.E electric field. Bias condition is Vd=2.5V, Vgs=1.0V, Vs=0.0V, Vb=-1.0V. The gate length is 0.30um. As a result of simulation Normal Emax=3.18MV/cm and HLDBD Emax=3.07MV/cm. This result shows HLDBD Emax is located in inner channel than Normal condition. Figure5,6 is shows the stress time vs Reverse Idsat and comparison life time normal vs and

HLDBD structure. HLDBD structure lifetime is improved 15% than normal structure.



(a) Normal NMOS. (b) HLDBD NMOS.

Figure 4. Hot carrier simulation.



(a) Normal structure (b) HLDBD structure

Figure 5. Stress time vs Reverse Idsat (Normal and HLDBD structure)

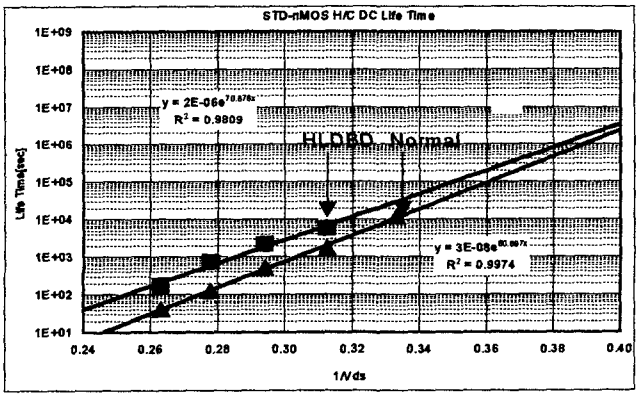


Figure 6. Comparison life time normal and HLDBD structure.

4. Conclusion

In this paper we proposed new HLDBD to overcome hot carrier effect. HLDBD is used to decrease junction electric field.. HLDBD process is performed after first gate etch, deposit HLD layer and followed n-type minor ion implantation. To confirm this, we simulate the basic experimental items. For the comparison of junction profile after full process and concentration profile just after n-type minor implantation. At the bias condition of fully charged state, the variation of electric field across the junction, according to each process scheme, was presented.

Reference

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