

A Multicast Switching Algorithm Based on iSLIP

Heyung Sub Lee^o, Sang Yeoun Lee, Hyeong Ho Lee, and Whan Woo Kim*

Router Technology Department, Electronics and Telecommunications Research Institute

* Department of Electronics Engineering, Chungnam National University

161 Kajong-Dong, Yusong-Gu, Taejon, 305-350, KOREA

Phone:+82-42-860-4863, Fax :+82-42-860-5213

E-mail: leehs@etri.re.kr

Abstract: This paper proposes a multicast packet-switching method which can less affect QoS degradation. The method includes a switch fabric with extra switching paths dedicated for multicast packets. Presented also are both a buffering structure and a scheduling algorithm for the proposed method. Simulation analysis for the method shows that the switching delay of unicast packets is decreased even though arrival rate of multicast packets is increased.

1. Introduction

Usually input buffering switch with crossbar fabric is used as a switch of high-speed network system. However, crossbar switch exists three types of blocking such as input port conflict, output port conflict and Head-Of-Line(HOL) blocking. These blocking problems in packet switch systems make difficult to provide QoS service of real time as circuit switching. Especially, multicast packet traffic increase due to the variety and integration of service and the switching of multicast packet causes more degradation of performance and service delay in network system. The research of switching mechanisms to reduce a blocking caused by multicast packet switching is necessary to get good switching performance for QoS service.[1][2]

A well known method to reduce the switch blocking problem of multicast packet is using the iSLIP scheduling algorithm on the VOQ(Virtual Output Queuing) structure. This paper reviews switching methods and scheduling algorithms of multicast packet on router system that is a symbol of packet switch. Also paper proposes a switch structure to improve the switching efficiency of multicast as well as unicast. The proposed switch structure has an extra switching path for multicast packets, and both type packets of multicast and unicast are switched at the same switching slot. To improve switching performance of the proposed switch structure, designed also proposed a buffering structure and a scheduling method based on iSLIP algorithm. In the paper, simulation analysis for not only delay and performance of proposed system is performed but also compare with other multicast scheduling algorithms. The simulation results show a possibility of application to the switch system through hardware implementation

2. Multicast Switching with Dedicated Path

2.1 Switch Structure for Multicast Packet Switching

As telecommunication traffic increases, network system using an efficient switching algorithm is required to QoS service. The traffic may be composed of unicast and multicast traffic. A popular way to handle the multicast traffic is to replicate it multiple times into the unicast queues in order to treat the multicast traffic as a unicast one. However, this approach has two disadvantages: increasing the required memory and reducing the bandwidth available to other traffic at the same input [3], [4]. To overcome the disadvantages, this paper proposes a switch structure using dedicated path that is combined VOQ buffering method and output port expansion method. The proposed switch structure has named EOPSF(Extended Output Port Switch Fabric) which extends an output port of crossbar switch from $N \times N$ to $N \times (N+Y)$. Since multicast packet have to switch at least two output ports, transmission to output ports use a shared method of bus type. The modified switch fabric of $N \times (N+Y)$ has $N \times N$ crossbar switch fabric for unicast traffic and Y buses for multicast traffic as shown in Fig. 1. [5]

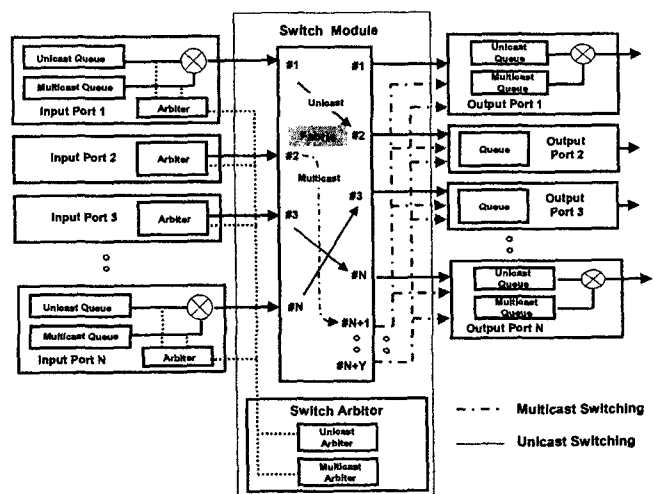


Figure 1. Bus and memory buffer of the forwarding function block

2.2 Buffering Structure of EOPSF Switch System

The effective buffering structure is required to get the maximum throughput through simultaneous switching of multicast and unicast. The designed buffering structure has each separated logical buffers of unicast packet and multicast packet at both input port and output port. Since switching of unicast packet depends on destination of packet, unicast buffer of each input port has N VOQs (Virtual Output Queue) to remove HOL blocking. Otherwise, multicast buffer is single queue in input ports because multicast packet is switched to output ports through the shared bus. The buffering structure of each output port is separated to multicast and unicast with respectively single queue. The multicast traffic can be transmitted along one of the Y multicast buses if the connection does not lead to input or output conflict (blocking). Each output port performs a filtering function that decides discard or not for received packet. The filtering function is performed by compare with setting bits that are coincident the output ports and set at input port. The service order between multicast and unicast is decided by scheduling algorithm such as WRR(Weighted Round Robin) in output port. Generally, above switching operation for output port is possible to implement on the outside of switch fabric as well as inside.

5.3 Scheduling Method of EOPSF Switch System

The most practical scheduling algorithm for VOQ is iSLIP algorithm that is modified round robin scheduling. Therefore, paper proposes a scheduling algorithm using iSLIP to obtain the maximum switching throughput of multicast and unicast. In the designed scheduler, scheduling of multicast and unicast packet is performed on the same time slot at all iterations. It is named PSLIP(Parallel iSLIP) and architecture of designed scheduler is shown in Fig.2[6][7]

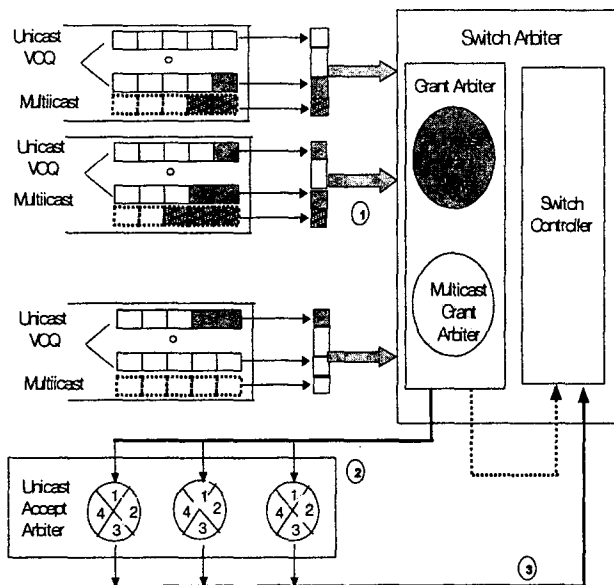


Figure 2. PSLIP scheduler for EOPSF switch system

The scheduler is designed as two parts of SA(Switch Arbitrer) and UAA(Unicast Acceptor Arbitrer). The SA is located in switch module and decides a switch connection to each output port. The UAA is placed in input module and selects a packet for switching from VOQ packets to output port. The SA arbiter consist of GA(Grant Arbitrer) and SC (Switch Controller) function blocks. The GA determines grant packets to switch from the multicast and unicast VOQs to each output ports. The SC controls the priority pointer of UGA(Unicast Grant Arbitrer) and MGA(Multicast Grant Arbitrer) in order to determine switching order of scheduling packets.

When SA arbiter selects a grant packet, multicast packet has higher priority than every unicast packets. In case both packets of multicast and unicast request switching to the same output port, SA arbiter selects the multicast packet. The unicast packets granted by SA arbiter inform to the UAA of each input ports, UAA finally selects the switching packet in according to service priority among the granted unicast packets. And then, UAA requests switch connection to switch arbiter and SC controls a connection of the switching path between input port and output port. The Fig. 3 shows the state diagram representing operation procedure of proposed PSLIP scheduler.

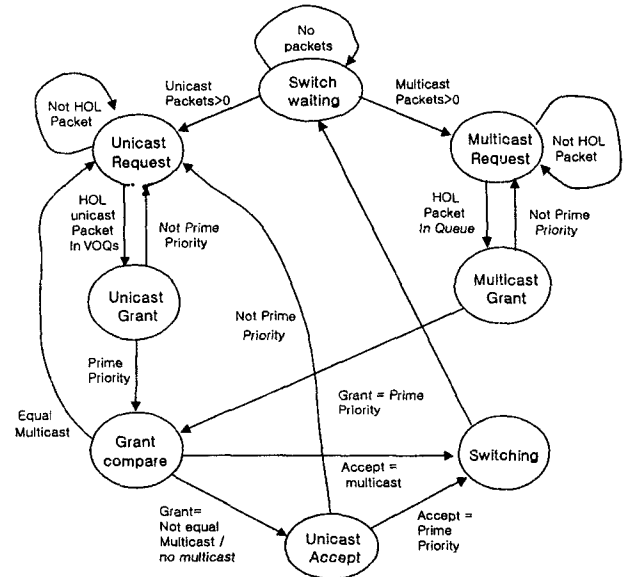


Figure 3. State diagram of PSLIP scheduler

3. Simulation Model of EOPSF Switch System

Simulation is performed three aspects of service delay, fairness and throughput of unicast and multicast packets. The simulation results of PSLIP compare with other two algorithms, iSLIP and ESLIP. In the iSLIP algorithm, multicast packet is replicated all VOQs of unicast and switched as unicast. The ESLIP is one of the modified algorithms of iSLIP and has a separated scheduling method for multicast and unicast. The arrived packets into input port is assumed the Poisson distribution. The queuing model is used deterministic M/D/1 as service packet of switch is one per every switching time slot. In

analysis, all VOQs of each input ports exist at least one packet and it are switched to output ports according to random value. It is supposed that HOL packets of all VOQs request a switching on every time slot and performed 2 iterations in one slot time. The interval of scheduling slot is 0.1 sec and period of total simulation time is 1000 slot times. The switch structure on simulation uses 8x9 (N=8, Y=1) switch fabric and uses Awesim software toolkit on Pentium-III PC.

Table 1. Simulation variable and condition

Simulation Variable	Condition and Value
Simulation Algorithms	PSLIP, ESLIP, iSLIP
Input/Output Ports	8 x 9 (N=8, Y=1), 6 x 7, 4x 5
Simulation Software	Awesim II (SLAM upgrade version)
Scheduling iteration times	2 times
Queuing Model	M/D/1
Arrival Packet Distribution	Poisson Distribution
Switch Destination Ports	Random Variable
Unit Slot time	0.1 sec
Total Simulation Period	1,000 Slots

4 Simulation Results

4.1 Service Delay depend on Multicast Packet Rate

Under simulation condition, arrival rate of packet service at each input ports is the same at all input ports. The multicast percentage (packet rate) indicates the multicast packet out of total arrived packets of input ports. Multicast group represents the number of output ports that needs a replication to switch from one input port to several output ports. The service delay, time interval from the point that packet is stored in input buffer to the point that packet is transmitted to output port, is simulated in condition of the multicast packet rate. The simulation is performed at 10% ~ 40% range of multicast packet rate and simulation results show in Fig.4.

The simulation results of service delay (BUS(unicast), BUS(multicast)) in PSLIP algorithm with EOPSF switch show that unicast packet decreased according as multicast packet rate of input port increase. Otherwise, multicast packet increased according as multicast packet rate of input port increase. In review results, service delay of multicast packet rapidly increased in more than 10% multicast packet rate. When multicast packet rate go to over 20%, service delay of multicast packet with PSLIP algorithm shows longer than it with iSLIP algorithm. The reason of this result is considered a output confliction that all multicast packets are switched just one multicast switch port(Y=1) even though multicast packets of each input ports are increased.

The service delay of unicast packet using PSLIP

algorithm shows a different result on compare with other algorithms. The service delay of PSLIP algorithm is not increased according to increase of multicast packet rate but other algorithms increased. As simulation results, we know that PSLIP algorithm with EOPSF switch is an effective multicast packet switching method on to support QoS service at 20% below of multicast packet rate.

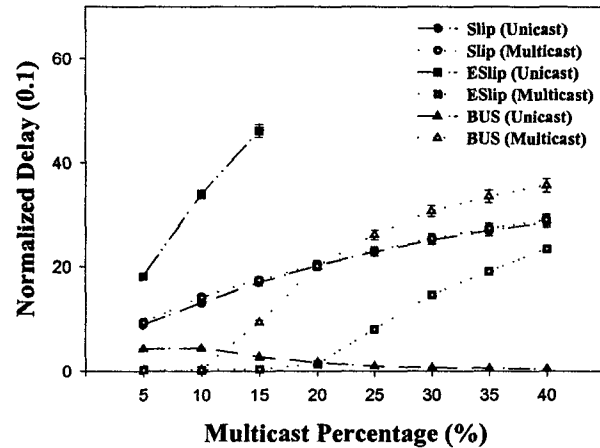


Fig.4. Simulation results of service delay depend on multicast packet percentage

4.2 Service Delay depend on Multicast Packet Size

When arrival rate of packets at all input ports is the same and multicast packet rate is 10%, simulation for service delay of multicast packet is performed depend on multicast packet size. The result of simulation shows that service delay is not affected according to multicast packet size as shown in Fig.5.

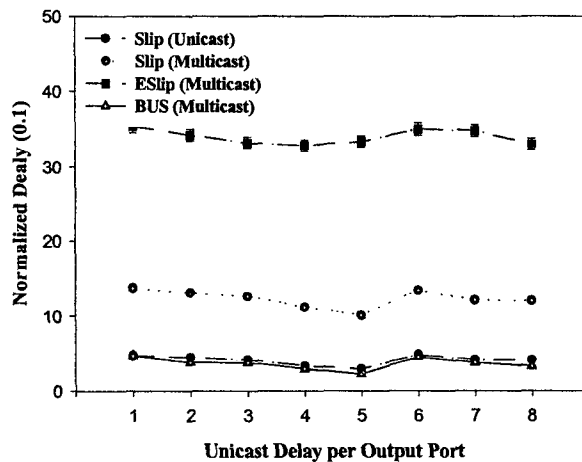


Fig.5. Simulation results of service delay depend on multicast packet size

In the simulation results (BUS(unicast), BUS(multicast)) of proposed algorithm and switch architecture, service delay of both type packets is constant regardless to multicast packet size. The reason can be deduced that input confliction occurs only an input port which multicast packet is serviced. Therefore, we can recognize that service delay is not affected by multicast switching size but affected by multicast packet percentage of arriving packet in input port.

4.2 Simulation for Service Fairness

The service delay of unicast packet in NxN switch fabric is simulated to find fairness effect due to multicast packet. The average service delay of unicast packet on each output ports is shown in Fig.6. As the result of simulation, unicast service delay of ESLIP (ESlip(multicast)) has the longest value in case multicast packet exists in arrival packets. However, service delay deviation of ESLIP on output ports is smaller than other algorithm.

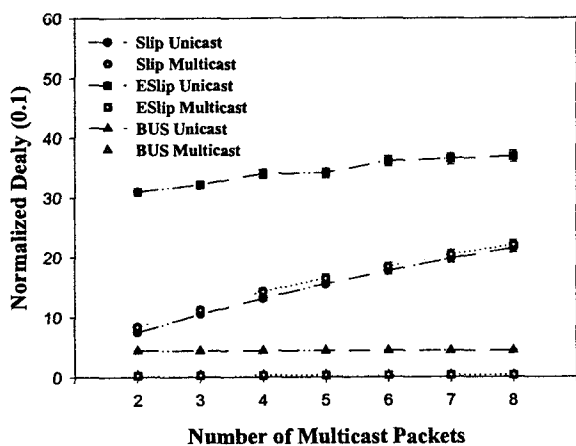


Fig.6. Simulation results of service fairness depend on multicast packet percentage

The service delay deviation of proposed algorithm in this paper is very similar to the Slip(Unicast) result which only exist the unicast packet in arrived packets without multicast packet. From the simulation results, we know that service delay and service deviation (Jitter) of unicast packet in the proposed switch structure and PSLIP algorithm maintain most likely values without multicast packet, in case multicast packet rate is less than 20%.

5. Conclusion

This paper proposes a multicast packet-switching method that includes a switch fabric with extra switching paths dedicated for multicast packets to provide QoS service. Also, paper designed a buffering structure related in proposed switch structure and a scheduling algorithm (PSLIP) based on iSLIP algorithm. The simulation results of proposed PSLIP algorithm show that service delay of

multicast and unicast packets can be effectively reduce in case multicast packet rate is less than 20%.

However, proposed PSLIP algorithm has a defect that service delay of multicast packet rapidly increases in which multicast packet rate of arrived packets on each input ports is more than 20%. The other hand, the service delay and fairness of unicast packet have most likely values as iSLIP scheduling regardless multicast packet rate of input ports. In the proposed switch structure and scheduling algorithm maintain same values as without multicast packet in which multicast packet rate is less than 20%.

The proposed method may require the further study for burst packet input, but characteristics of service delay and fairness are superior to other methods. Therefore, the proposed method can be implemented in simple hardware in order to support QoS service for network system as router.

References

- [1] Dye-Jyun Ma, "Performance analysis of A Nonblocking Space-division PacketSwitch with Window Policy", ICICS'97, Singapore, 3F1.2, September, 1997.
- [2] H. Jonathan Chao et.al., "Design of Packet-Fair Queuing Schedulers using a RAM-Based searching Engine" IEEE JSAC Trans. Vol.17, No.6, June 1999.
- [3] Ali, M., Youssefi, M, "Performance analysis of a random packet selection policy for multicast switching", IEEE Trans. Commun, Vol.44, No.3, Mar 1996.
- [4] N. H. Liu and Kwan L. Yeung, "New Packet Scheduling Algorithm for Input-buffered Multicast Packet Switches" GLOBECOM'97, Part vol.3, 1997, pp.1695-9.
- [5] Heyung Sub Lee et.al., "Deign of the Packet Forwarding Chipset with Feedback Blocking" ITC-CSCC, July 1999.
- [6] B. Prabhakar, "Multicast Scheduling for Input-Queued Switches" IEEE JSAC, June 1977.
- [7] N. McKeown, "iSLIP: A Scheduling Algorithm for Input - Queued Switches," IEEE/ACM Trans. Vol7, No.2, April. 1999.