A CMOS Rail-to-Rail Current Conveyer and Its Applications to Current-Mode Filters

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Abstract: This paper presents a second-generation CMOS current conveyor (CCII) consisting of a rail-to-rail complementary N- and P-channel differential input stage for the voltage input, a class AB push-pull stage for the current input, and current mirrors for the current outputs. The CCII was implemented using a double-poly triple-metal 0.6 μm n-well CMOS process, to confirm its operation experimentally. A prototype chip achieves a rail-to-rail swing ±2.4 V under ±2.5 V power supplies and shows the exact voltage and current following performances up to 100 MHz. Because of its high performances, the CCII proposed herein is quite useful for a building block of current-mode circuits. The applications of the proposed CCII to current-mode filters are also described.

1. Introduction

To meet a requirement for the wide dynamic range and the wide bandwidth operations under the low supply voltage, current-mode analog signal processing is receiving much attention as a voltage-mode alternative. An op-amp equivalent in current-mode circuits is the second-generation current conveyor (CCII), and its CMOS realization is highly requested to facilitate the analog circuit design in a mixed analog and digital CMOS ASIC [1], [2].

The CCII is characterized in terms of the voltage- and current-following performances [3]. An excellent voltage-following performance can be realized by the op-amp with unity-gain configuration. The rail-to-rail input and output capabilities are also provided with the op-amp under class AB operation [4-8]. A high performance CCII can thus be realized by combining such an op-amp and current mirrors. Based on this idea, a CMOS rail-to-rail CCII is developed. Its circuit configuration, simulated performances, and a prototype chip fabricated using 0.6 μm CMOS process will be described in the followings.

2. Circuit Description

The circuit configuration of the CMOS rail-to-rail CCII is shown in Fig. 1, where Y is the voltage input terminal, X is the voltage output/ current input terminal, and ±Z are the current output terminals. It comprises four blocks; the rail-to-rail input stage consisting of the complementary N- and P-channel differential pairs (M_{n1}~M_{n4}, M_{p1}~M_{p4}) for the voltage input v_Y, the rail-to-rail class AB push-pull stage (M_{n5}, M_{p5}) for the voltage output/ current input i_X, the current mirrors (M_{n6}~M_{n9}, M_{p6}~M_{p9}) for the current outputs $i_{\pm Z}$, and the bias stage.

The complementary input stage consists of the N- and P-channel differential pairs connected in parallel. The operation can be divided into three regions: The positive rail region where only NMOS pair is active, the mid-rail region where both NMOS and PMOS pairs are active, and the negative rail region where only PMOS pair is active. The transconductance g_m of the input stage therefore depends on the input voltage. The dependence may cause the harmonic distortion, but the common-mode feedback to make g_m independent of the input voltage is not incorporated because the harmonic distortion can be greatly suppressed by the fully feedback configuration.

The differential stages and the current outputs stage form the active current mirror [9], [10]. The active current mirror achieves the exact mirror operation by reducing the input impedance effectively by the differential stage gain.

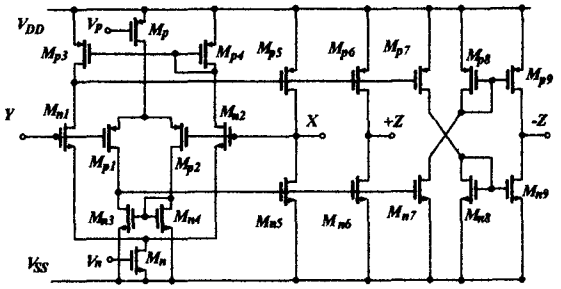


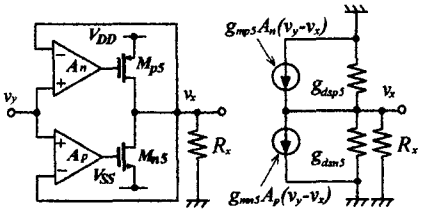
Fig. 1. The circuit diagram of the proposed rail-to-rail CCII.

2.1 Voltage Following Operation

Regarding the voltage and current input stages as the input and output stages of an op-amp, respectively, one can model the input stage as shown in Fig. 2(a). Figure 2(b) shows the small-signal equivalent circuit. Referring to this model, one obtains the voltage transfer gain A_v from the node Y to the node X:

$$A_v = \frac{v_x}{v_y} = \frac{g_{mn5}A_p + g_{mp5}A_n}{g_{mn5}A_p + g_{mp5}A_n + g_{dsn5} + g_{dsp5} + 1/R_x}, \quad (1)$$

where A_n and A_p are the gains of the differential stages, g_m and g_{ds} are the transconductance and drain-source conductance of MOS transistor, respectively. A_v is very close to 1 since $1/R_x$, $g_{ds} \ll g_m$ holds. Therefore, v_x exactly follows v_y.



(a) (b)

Fig. 2. The input stage model of the CCII (a) and its small-signal equivalent circuit (b).

2.2 Input/Output Impedance at Node X

Referring to Fig. 3, the impedance r_{xn} presented by M_{n5} is given by

$$r_{xn} = \frac{1}{g_{dsn5} + g_{mn5}A_p}. \quad (2)$$

Similarly, the impedance r_{xp} is presented by M_{p5}. The impedance r_x at the node X is the parallel connection of r_{xn} and r_{xp}, and thus

$$r_x = r_{xp} // r_{xn} \approx \frac{1}{g_{mn5}A_p + g_{mp5}A_n}. \quad (3)$$

In deriving the last expression, $g_{ds} \ll g_m$ is assumed.

Equation (3) indicates that the impedance at the node X of a basic CCII is reduced by the open loop gain of the differential stage. With the simple configuration shown in Fig. 1, the gain higher than 40 dB can be realized. It follows therefore that the node X in Fig. 1 is virtually grounded when the node Y is grounded.

2.3 Rail-to-rail Class AB Output Stage

Referring again to Figs. 1 and 3, one obtains the following expressions for the current flowing through M_{n5} and M_{p5}:

$$i_{dn5} = J + g_{dsn5}v_{dn5} - g_{mn5}A_p(v_y - v_x), \quad (4)$$

$$i_{dp5} = J + g_{dsp5}v_{dp5} + g_{mp5}A_n(v_y - v_x), \quad (5)$$

where $v_{dn5}=v_x-V_{SS}$, $v_{dp5}= V_{DD}-v_x$. In (4) and (5), the same quiescent current J is assumed flowing through M_{p5} and M_{n5}. Because of the exact voltage-following action $v_y=v_x$ and $g_{ds} \ll 1$, the ac components in (4) and (5) are much smaller than the quiescent current . Then

$$v_{gsn5} + v_{gsp5} = \sqrt{\frac{i_{dp5}}{K_{p5}}} + V_{thp5} + \sqrt{\frac{i_{dn5}}{K_{n5}}} + V_{thn5}$$

$$\approx \sqrt{\frac{J}{K}}\left(2 + \frac{g_{ds}(V_{DD} - V_{SS})}{2J}\right) + V_{thn5} + V_{thp5} = const. \quad (6)$$

where K_{p5} and K_{n5} are the transconductance parameters of M_{p5} and M_{n5}, respectively, and $K_{p5}=K_{n5}=K$ and $g_{dsp5}=g_{dsn5}$ are assumed to derive the last expression. Equation (6) indicates that M_{p5} and M_{n5} operate under the push-pull mode.

The current i_x applied to the node X is shared between M_{p5} and M_{n5}. Taking the push-pull condition (6) into account, one can derive the following expressions for i_{dp5} and i_{dn5}:

$$i_{dn5} = J - i_x/2 + i_x^2/16J, \quad (7)$$

$$i_{dp5} = J + i_x/2 + i_x^2/16J. \quad (8)$$

Equations (7) and (8) indicate that the push-pull operation continues until i_x reaches ±4J and the single-ended operation starts, as shown in Fig. 3. The maximum current is limited by the voltage headroom in the push-pull stage.

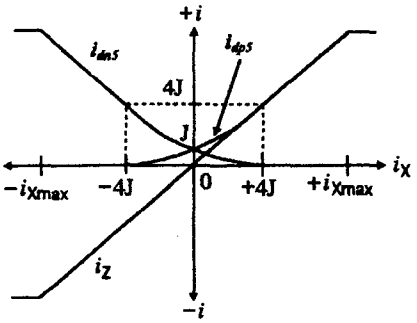


Fig. 3. The current transfer characteristics.

3. Performance

3.1 Simulations

Performances of the CCII shown in Fig. 1 are simulated using HSPICE. Transistor dimensions are listed in Table 1. The parameters used for the simulations assume 0.6 μm CMOS process. Supply voltages are $V_{DD} = -V_{SS} = 2.5$ V and J is set to 50 μA. Simulated performances are shown by solid and dotted lines in the following figures.

The total harmonic distortion (THD) in the voltage follower when 1 V_{p-p} sinusoidal signal is applied to the node Y and the node X is terminated by R_X = 1 kΩ is lower than –80 dB in the low-frequency region.

The Bode diagram of the differential stage shows that the dc gain when the output node X is terminated by 1 kΩ is 43 dB, the unity gain frequency is 64 MHz and the phase margin is 65 °.

Table 1. Transistor dimensions.

Transistor	W (μm)	L (μm)
M_{n1}- M_{n4}	36	2.4
M_{p1}- M_{p4}	72	2.4
M_{n5}- M_{n9}	48	1.2
M_{p5}- M_{p9}	120	1.2

Figure 4 shows the input characteristics at the node X. The positive sign in the current indicates the current flowing into the node and the minus sign the current flowing out of the node. The impedance r_x is 4.22 Ω in the push-pull region and decreases slightly in the single-ended region.

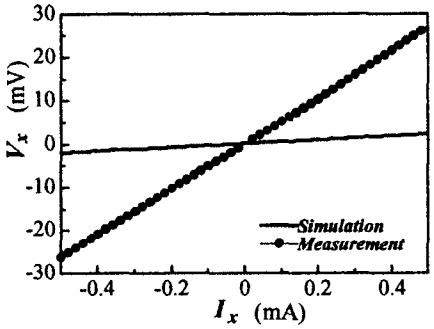


Fig. 4. The V_x versus I_x characteristics.

Figure 5 shows the voltage transfer characteristics from the node Y to the node X when the node Z is short-circuited to ground. The exact voltage-following performance and the rail-to-rail input and output capabilities are demonstrated. The offset voltage at the node X when the node Y is grounded is less than 60 μV.

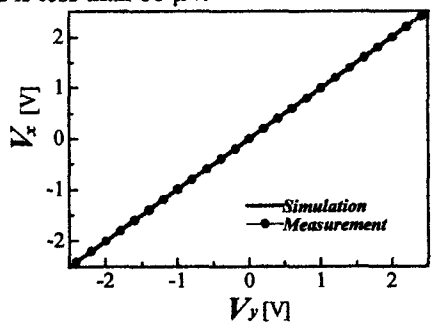


Fig. 5. The voltage transfer characteristics of the CCII.

Figure 6 shows the current transfer characteristics from the node X to the node Z. The transfer gains I_{+z}/I_x and I_{-z}/I_x are 1.00 and -1.09, respectively, and the offset currents in I_{+z} and I_{-z} are 0.93 nA and 1.98 μA, respectively.

The frequency characteristics of the voltage gain when the node X is terminated by R_X = 1 kΩ are shown in Fig. 7. The –3 dB bandwidth extends beyond 150 MHz.

Figure 8 shows the frequency characteristics of the current transfer gain. The bandwidth extends again beyond 150 MHz and no degradation due to the differential stage is observed.

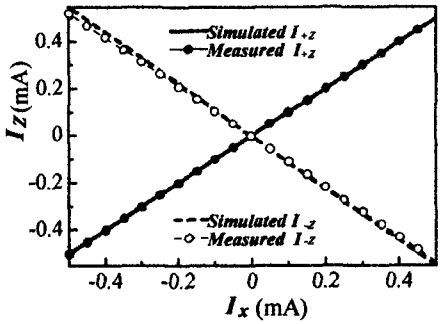


Fig. 6. The current transfer characteristics.

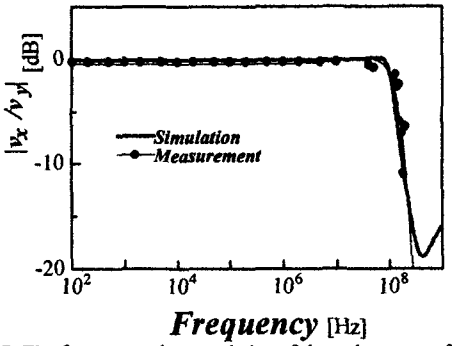


Fig. 7. The frequency characteristics of the voltage transfer gain.

Figure 9 shows the frequency dependence of the input impedance at the node X when the nodes Y and Z are grounded. The input impedance increases with the frequency in the frequency region above 1 MHz. This is due to the gain reduction in the differential stage.

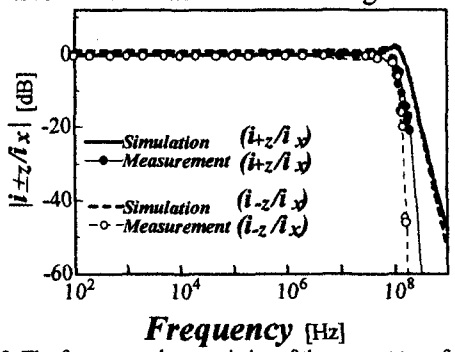


Fig. 8. The frequency characteristics of the current transfer gains.

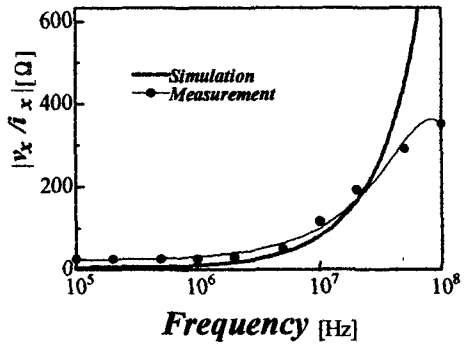


Fig. 9. The frequency dependence of the input impedance.

3.2 Measured Performances

The proposed CCII was implemented using a double-poly, triple-metal 0.6 μm n-well CMOS process. The microphotograph of the prototype chip is shown in Fig. 10. The chip measures 150 μm × 150 μm. All the measurements are done under ±2.5 V supplies. Measured performances are indicated by dots in the relevant figures.

In Fig. 4, the measured input impedance r_x is 53.2 Ω in the push-pull region. The simulated value is 4.22 Ω. The large difference is attributed to the wire resistance between the node X and the ponding pad. The voltage transfer characteristics are plotted in Fig. 5, which demonstrates the exact voltage-following performance and the rail-to-rail input and output capabilities. The offset voltage at the node X when the node Y is grounded is less than 40 μV.

In Fig. 6, the exact current-following performances in good agreement with the simulations can be seen over the wide current range. The transfer gains I_{+z}/I_x and I_{-z}/I_x are 1.00 and −1.05, respectively. The offset currents in I_{+z} and I_{-z} when the node Y is grounded are 5 nA and 440 nA, respectively.

The frequency characteristics of the voltage gain when the node X is terminated by R_X = 1 kΩ are plotted in Fig. 7. The −3 dB bandwidth of the voltage gain v_X/v_Y extends beyond 100 MHz. The frequency characteristics of the current transfer gains are plotted in Fig. 8. The bandwidth extends again beyond 100 MHz.

The measured input impedance, which is plotted in Fig. 9, is higher than the simulated one in the low frequency range. This is due to the wire resistance from the node X to the ponding pad. In the high frequency range, on the other hand, the measured impedance is lower than the simulated one. This is due to the parasitic capacitance of the ponding pad.

Fig. 10. A microphotograph of the prototype chip.

4. Applications to Current-Mode Filters

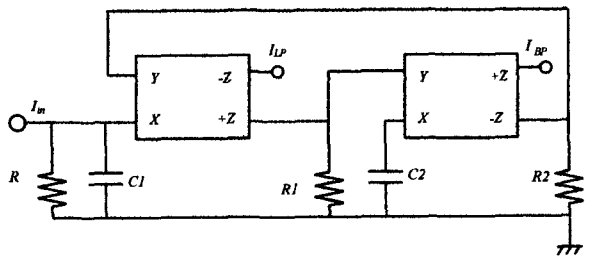


Fig. 11. A circuit diagram of the current-mode filter.

Figure 11 shows the second-order low-pass and band-pass filter [11]. The low-pass and band-pass current transfer functions are given by

$$\frac{I_{LP}}{I_{in}} = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}, \quad (9)$$

$$\frac{I_{BP}}{I_{in}} = \frac{\frac{\omega_0}{Q}s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}, \quad (10)$$

where ω_0 and Q are given by

$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}}, \quad Q = R\sqrt{\frac{C_1}{C_2 R_1 R_2}}. \quad (11)$$

This filter has been built using CCII developed. RC components used are listed in Table 2. In determining the RC values, the Butterworth characteristics are assumed for the low-pass filter.

Table 2. The set value of the current mode filter.

Filter	*Band-Pass*	*Low-pass*
Specs	$Q = 4, f_0 = 50$ MHz	$Q = 0.7, f_0 = 50$ MHz
R	2.67 kΩ	425 Ω
R_1	615 Ω	615 Ω
R_2	616 Ω	616 Ω
C_1	4.83 pF	4.83 pF
C_2	5.17 pF	5.17 pF

Figure 12 shows the frequency characteristics of the low pass filter. The theoretical cutoff frequency is 51.73 MHz, whereas the simulated and measured values are 22.9 MHz, and 32.5 MHz, respectively.

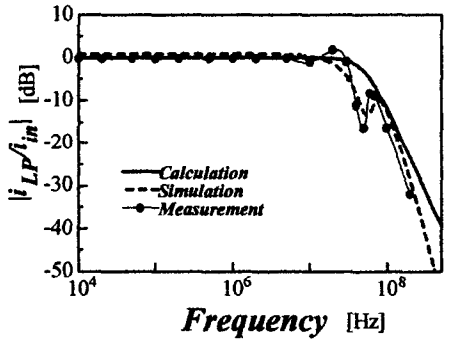


Fig. 12. The frequency characteristics of the current-mode low-pass filter.

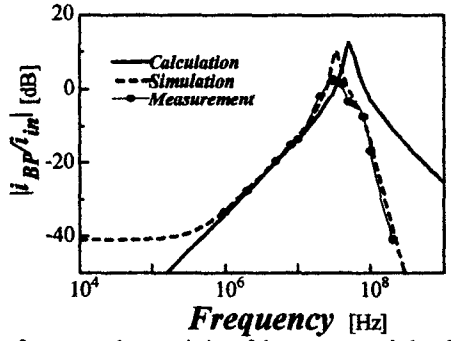


Fig. 13. The frequency characteristics of the current-mode band-pass filter.

Figure 13 shows the frequency characteristics of the band pass filter. The theoretical center frequency is 51.73 MHz, whereas the simulated and measured values are 33.8 MHz, and 33.0 MHz, respectively. The theoretical value of Q is 4.2, whereas the simulated and measured values are 4.1, and 2.0, respectively.

5. Conclusions

A rail-to-rail CCII developed for wideband signal processing under low power operation was described. The prototype chip fabricated using 0.6 μm CMOS process has demonstrated the performances quite satisfactory for a building block of current-mode circuits.

Its applications to current-mode filters have demonstrated the validity for wideband signal processing. The operation under the single supply voltage as low as 1 V has also been confirmed experimentally. Such a low-voltage operation and the small device-count are also quite attractive to ASICs. The commercial chip is now under fabrication using a standard digital CMOS process.

Acknowledgment

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