Flip Chip Technologies

한양대학교 신소재공학부
김 영 호
kimyh@hanyang.ac.kr

Chip Interconnection 방법

1. **Wire Bonding**
2. **Tape Automated Bonding (TAB)**
3. **Flip Chip Bonding**

Wire Bonding

- the most common chip interconnection technique

(특징)

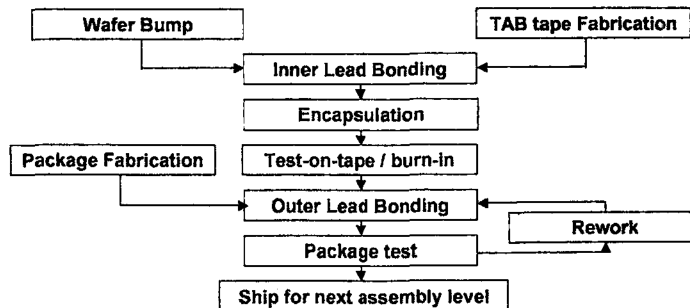
- 경제적, 생산성 우수 (automation)
- good flexibility and reliability
- I/O density의 제한 (< 300)
- inductance 발생 (wire의 길이를 줄여야)

(공정 방법)

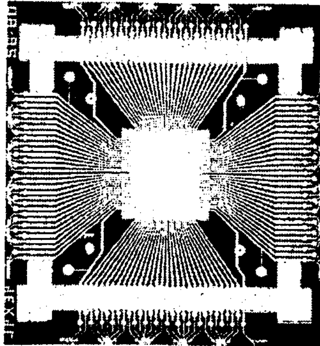
- Thermocompression method
- Ultrasonic method
- Thermosonic method

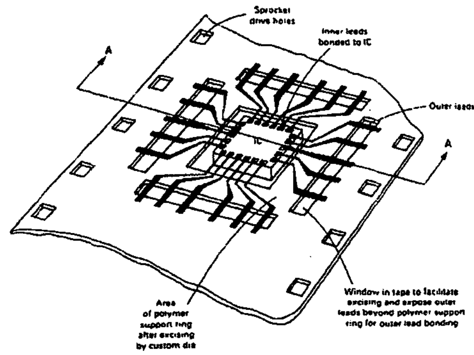
Tape-Automated-bonding (TAB) process

높은 실장 밀도, 다핀화 가능
박막화 가능 (IC Card, LCD용)
일괄 본딩 가능 (gang bonding)
Test와 burn-in등을 assembly 중간에 가능
Module 화 가능



Tape Automated Bonding (TAB)



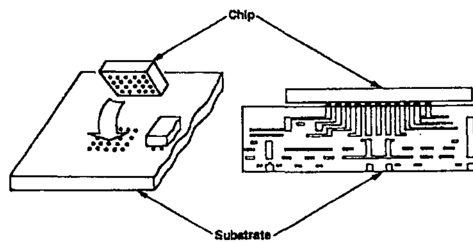


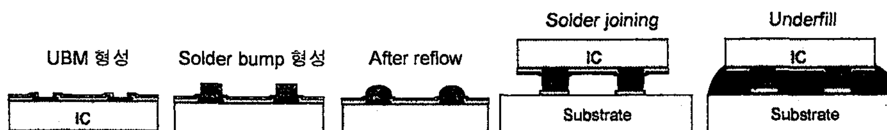
TAB tape

Bonding 된 모양

Flip Chip Technology

- **IBM C4 Process** (Controlled-Collapse Chip Connection)





Flip Chip Technology

- **Definition**

  the direct electrical interconnection of electronic components onto substrates by means of bumps

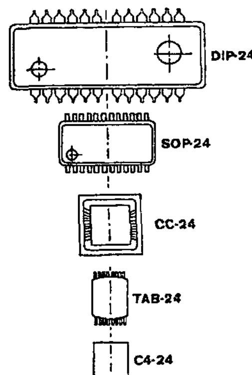
- **Application**

  Flip chip components
  - **Semiconductor device**
  - **Passive component**
  - **Detector arrays**
  - **MEMs device**

- **Characteristics**
  - **Smallest Size**
  - **Greatest I/O Flexibility**
  - **Highest Performance**
  - **Reliable**

- **Function**
  - **electrically conductive path between the chip and the substrate rate**
  - **thermally conductive path to carry from the chip to the substrates**
  - **mechanical mounting of the die to the substrate**
  - **a spacer preventing electrical conduct between the chip and substrate conduct**

Space Efficiency by IC Package Type



Package Space (16K CMOS SRAM)

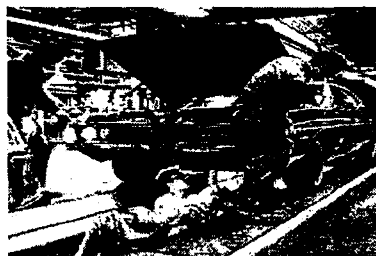
	DIP-24	SOP-24	CC-24	TAB-24	C4-24
mm X mm	31.0 X 15.24	15.4 X 10.24	11.18 X 11.18	5.65 X 8.87	5.65 X 6.57
mm^2	472.44	157.70	124.99	50.12	37.12
Ratio	12.73	4.25	3.37	1.35	1

History of Flip Chip Technologies (IBM)

- **1st Generation**
  - Solid logic Technology
    - Cu micro-ball / high mp solder
    - Application to the transistors (1961)
    - Production in the IBM system 360 (1964)
- **2nd Generation**
  - Controlled collapse Chip Connection (1970)

History of Flip Chip Technology (GM)

- **GM's Delco Division (now Delphi Delco in Kokomo, Ind.)**
  - Electroplated Ag bumps
  - Au/Cr UBM on the passivated die
  - Voltage regulator under the hood of 1969 Pontiac automobile



(Source : Chip scale Review)

Flip Chip Solder Joining 기술

- **Chip surface (active area) facing to the substrate**
- **Solder bump : electrical and mechanical interconnection**

장점

- **High I/O density**
- **Chip packaging** 밀도 높음
- **Short interconnection length** ➡ 전기적 특성 우수
- 신뢰도가 큼 **(under fill** 공정적용**)**
- **Self alignment**

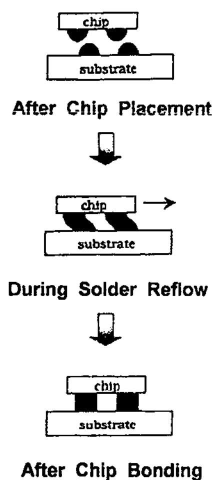
단점

- **Process complexity** ➡ **Higher Cost**
- ***Thermal strain*** ➡ ***fatigue***
- **Joining**후 **optical inspection** 불가

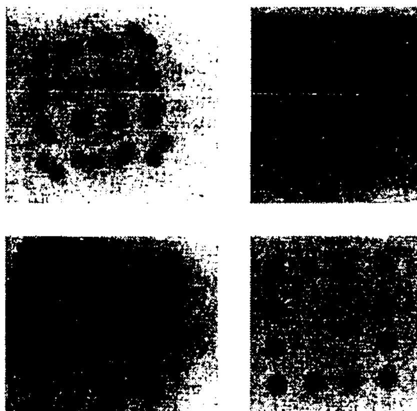
SEM Image of Solder Joints

√ **In-Ag solder on Au/Cu/Cr (50 ㎛ pitch)**

Solder의 Self-Alignment Effect

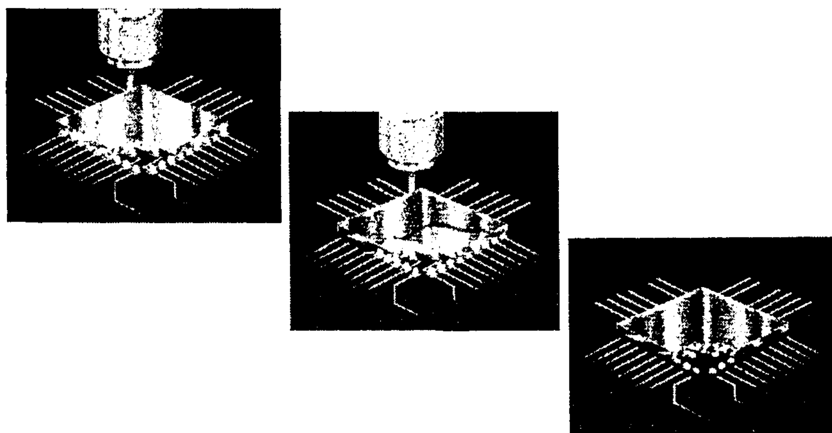


X-ray images



(Source : Flip Chip Technologies)

Underfill Process



Under Bump Metallurgy(UBM) or Ball limiting Metallurgy(BLM)

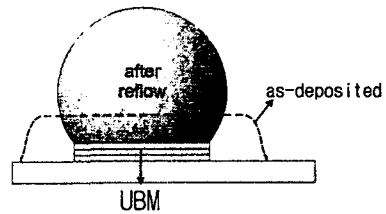
Solder를 Al Pad위에 Wetting

- Adhesion/ Barrier layer, Wetting layer, Oxide Prevention layer로 구성
- 제조방법 : Evaporation, Sputtering, Plating
- Metallurgy

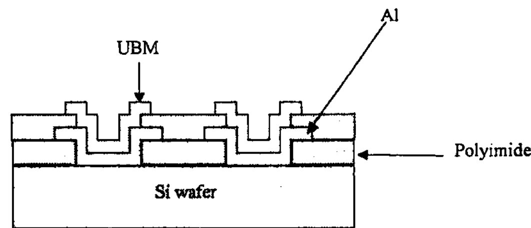
  Adhesion layer : Cr, Ti, TiW, Al

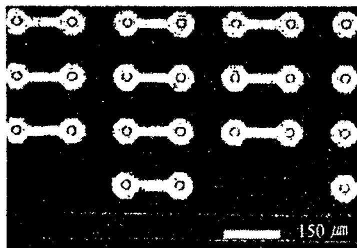
  Wetting layer : Cu, Ni, Pd, Pt

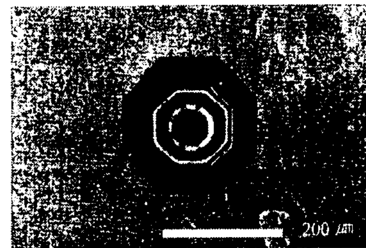
  Oxide Prevention layer : Au



형성된 UBM pad

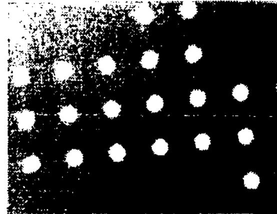




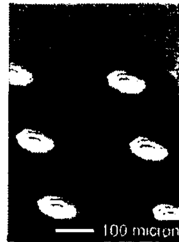


UBM patterns

- Optical image



- SEM images



Solder Bump

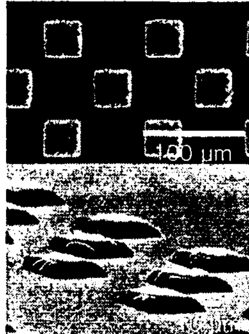
- 기 능
  - Chip과 Substrate 사이의 Electrical and Mechanical Connection
  - Chip으로 부터의 Heat Dissipation Path
- 재 료
  - Eutectic Pb-Sn, Pb-Sn-Ag
  - High Pb-5～10 %Sn
  - Pb-In(50/50)
  - In
  - Pb-Free solders (Sn-Ag-Cu, Sn-Cu 등)

Figure 1. Standard flip chip array with eutectic Sn/Pb solder bumps

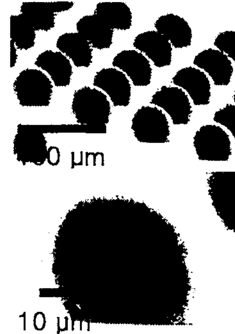
주요 Solder bump 제조 방법

- Evaporation
- Electroplating
- Solder paste print
- Jetting
- Stud bumping

Before Reflow



After Reflow



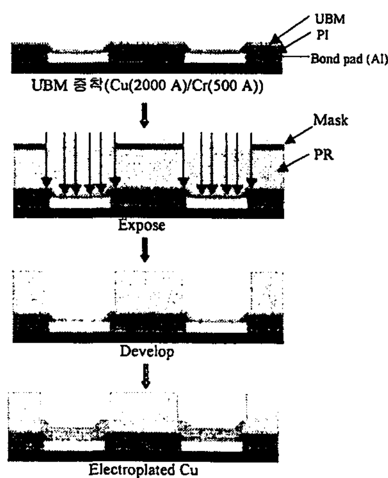
Evaporation을 이용한 Solder Bump 형성

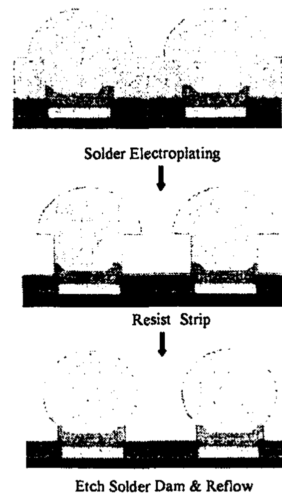
- **UBM과 솔더를 금속 마스크를 이용하여 순서대로 evaporation**
  - 가장 오래된 방법, 신뢰성 있음
  - 두께, 조성 조절이 쉽다.
  - 고가의 장비 필요, 공정 비용이 비쌈
  - 3상이상의 합금 조성제어가 힘듬 ➡ reflow 필요

전기도금 방법에 의한 Solder Bump 형성

- Evaporation 방법에 비해 시설비가 적게 들고 가격이 싸다.
- 미세 범프 형성이 용이
- 도금 공정에 의한 응력 발생 가능 ➡ 신뢰도 저하
- 위치에 따른 솔더 두께, 조성 차이 발생 가능성
- 도금 중 수소 기체가 솔더 내에 trap ➡ pore 발생가능

전기도금에 의한 Solder Bump Formation Process





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Stencil Printing 방법에 의한 Bump 형성 방법

- **Stencil mask를 이용하여 Solder Paste를 도포**
  - 3상 이상의 솔더 범프 형성 가능하며 조성 조절이 쉽다.
  - Reflow공정 생략 가능
  - 가격 경쟁력 큼
  - 미세 피치 힘들다.

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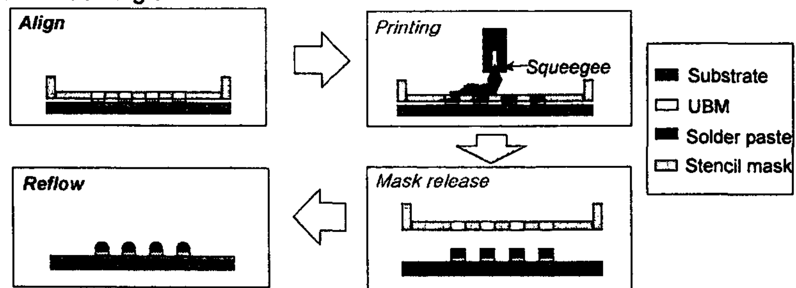
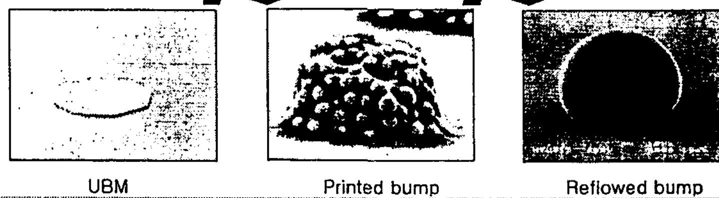
Stencil Printing Process

Schematic Diagram



SEM images



UBM　　Printed bump　　Reflowed bump

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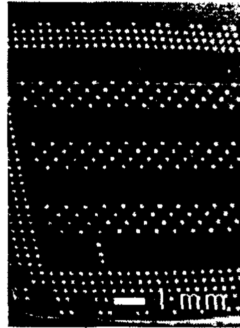
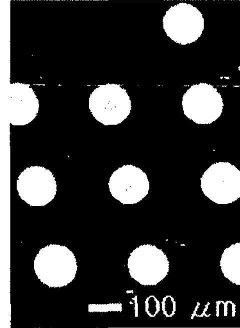
SEM image of the solder bumps after reflow





Height : 107 μm, Diameter : 124 μm

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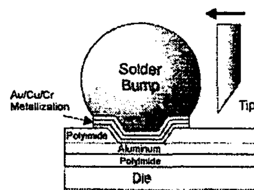
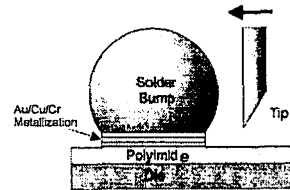
Shear Test Methods





Dage BT-2400
Tip speed : 0.11 mm/s
Tip height : 10 μm

Process capability

$$C_{pk} = \left| \frac{\bar{x} - s}{3\sigma} \right|$$

$\bar{x}$: the average value
s : the specified value
σ : the standard deviation

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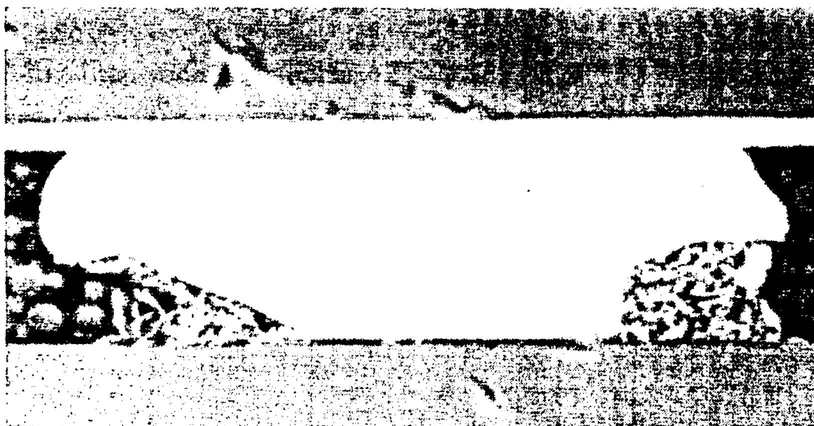
Stud Bump Flip Chip Technology

- **Bumping**
  - Stud bump material
    - Au, Pt, Cu
- **Connection to the substrate**
  - Conductive adhesives bonding
  - Non-conductive adhesive bonding
  - Ultrasonic or thermosonic bonding
  - Solder paste, plated solder reflow
- **Advantage and limitations**
  - Stud bump formed easily by wire bonders
    - Bumping equipment is widely available and well characterized
  - UBM not required
    - Fast, efficient, and flexible for low to medium production
    - Easy to scale up to high volume production
  - Serial process
    - Increasing bumping time with the number of bumps
    - More precise die bonder than self-aligning solder assemblies

Stud Bump Technology with Conductive Adhesive



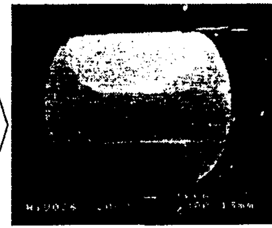
(Source : Flipchips.com)

Stud Bump Bonding Process

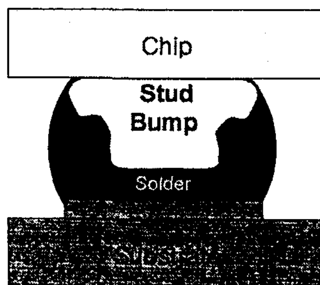
- Create conductive bumps on the die bond pads
- Coined (Flattened) the stud bumps by mechanical pressure
- Connect the die to the substrate
- Underfill

Stud bump formation

After Leveling


After Joining and Underfill

Stud Bump Bonding with Solder Paste



- Maskless process without special tooling costs
- Under bump metallurgy not necessary
- Fine pitch & chip level bumping possible
- Self-aligning possible

➡ Low cost Flip Chip Technology

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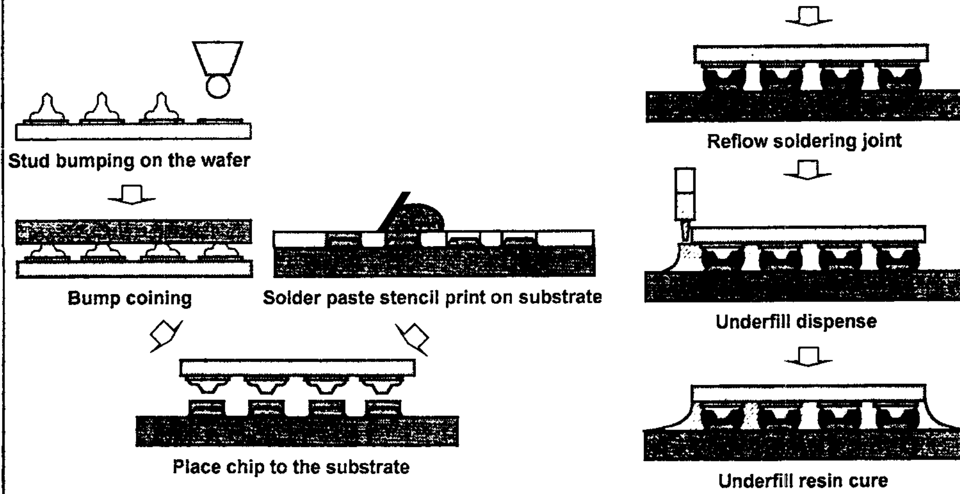
Overall process



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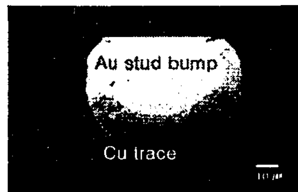
Cross sectional view of solder joints (BSE images)

The 1st reflow

Specimen # 1

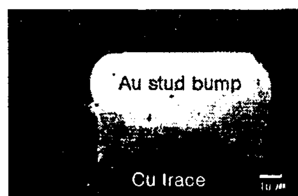


Specimen # 2

Specimen # 3

Multiple reflows

The 2nd reflow



The 3rd reflow

The 5th reflow

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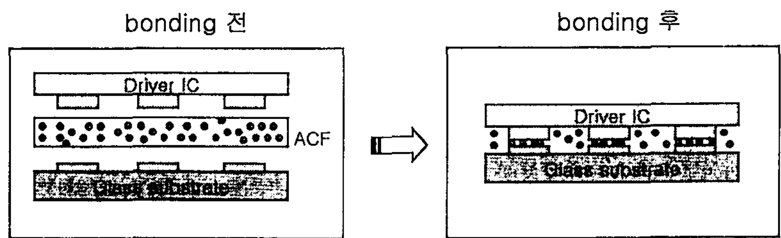
Chip On Glass (COG) Technology

- **Driver IC interconnection on LCD module**
- **Anisotropic Conductive Adhesive Film (ACF)** 이용
- 특 징
  - **Fine Pitch**
  - **Low Cost**
  - **Low Profile**
  - **Low Temperature Process**



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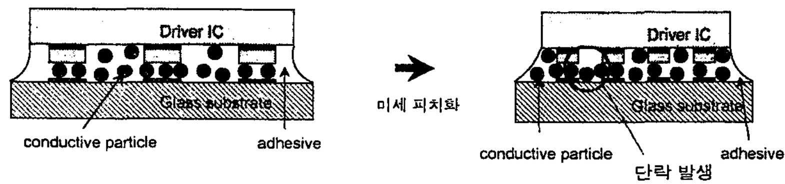
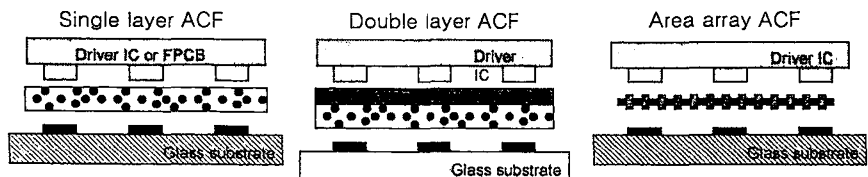
Pitch의 미세화에 따른 문제점과 해결책

- **Pitch**의 미세화에 따른 문제점

  ➡ 인접 전극간의 단락



Pitch의 미세화에 따른 문제점의 해결책



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