고전류 스트레싱하에서의 ACF 플립칩의 신뢰성 해석에 관한 연구

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Abstract

In this paper the maximum current carrying capability of ACAs flip chip joint is investigated based on two failure mechanisms: (1) degradation of the interface between gold stud bumps and aluminum pads; and (2) ACA swelling between chips and substrates under high current stress. For the determination of the maximum allowable current, bias stressing was applied to ACAs flip chip joint. The current level at which current carrying capability is saturated is defined as the maximum allowable current. The degradation mechanism under high current stress was studied by *in-situ* monitoring of gold stud bump-aluminum pad ACA contact resistance and also ACA junction temperature at various current level. The cumulative failure distributions were used to predict the lifetime of ACAs flip chip joint under high current stressing. These experimental results can be used to better understand and to improve the current carrying capability of ACA flip chip joint.

1. Introduction

In today's microelectronic systems, flip chip technology is being used more and more in high performance applications replacing wire bond technologies because of its improved electrical performance and smaller package size.

The continuing downscaling of structural dimensions in flip chip packaging has given rise to another problem. In detail, as the bump size is reduced, the current density through bump is also increased and increased current density causes new failure mechanism, electromigration phenomena in flip chip solder bumps [1,2].

There have been a few papers published about the electromigration study of flip chip joint during constant current density and temperature. However, constant current stressing conditions in those papers do not provide the constant current density at flip chip joint. Current stressing can damage the flip chip joint. For example, if there exist depleted UBM or interface crack during current stressing, between chip and substrate, actual flip chip joint could result in increased current density due to the decreased flip chip joint area. So, Black's equation as described in Eq. (1) can be only used for modeling current dependence of lifetime at the constant current density. Because of this reason, in this experiment, bias was stressed for the constant current density.

$$t_{50} = \frac{A}{J^n}\exp(\frac{E_a}{kT}) \qquad (1)$$

In addition, very few studies on high current stressing have been reported about the reliability of adhesive flip chip joint.

In this paper, the current carrying capability of ACA flip chip joint is investigated. In particular, discussion will be focused on degradation mechanism and lifetime prediction of ACAs flip chip with gold stud bumps joint under high current stress.

2. Experiment

Au stud bumps between Al pad on Si and thick Cu/Ni/Au pad on PCB were current stressed with various current levels. The stud bump has an acute tail, as shown in Fig. 1 (a), to provide good metal to metal contact during thermal compression. It was previously reported that an acute tail bump was more stable than a flat tail bump [3].

As the bonding strength of the metal to metal contact was not strong enough to hold a test chip on a PCB test substrate, interconnect material called ACF (Anisotropic Conductive Film) was used to mechanically hold a chip and a substrate. Bonding pressure of 2 ~ 3 kgf/cm^2 and temperature of 180 °C for 30 sec was applied.

A schematic cross-sectional diagram of joint for current stressing is shown in Fig. 1 (b). In the diagram, intermetallic compound of Au-Al has been sketched to depict the possible intermetallic compound formation during flip chip assembly and test.

For current stressing test, the special test equipment was designed to interpret current stress induced failure of ACAs flip chip joint. For the determination of maximum allowable current, bias stressing was applied to a pair of Au stud bump joints.

The current level at which current carrying capability is saturated is defined as the maximum allowable current.

The degradation mechanism under high current stress was studied by *in-situ* monitoring of gold stud bump-aluminum pad ACA contact resistance and ACA junction temperature at various current levels. In particular, the temperature distribution inside joints was measured to analyze current induced failure mechanism of adhesive flip chip joint. During constant current stress below critical current, *in-situ* resistance and temperature were measured to understand the behavior of adhesive flip chip joint.

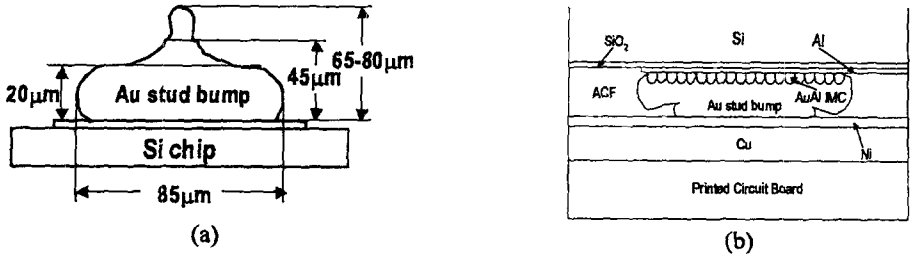


Fig. 1. A schematic diagram of (a) Au stud bump, (b) stud bump joint for high current stressing

Time to failure(TTF) was measured by monitoring the resistance of adhesive flip chip joint. At least ten independent tests were conducted for each current stressing condition. Each failure causes a step-shaped increase in the resistance.

The data of TTF collected were used for evaluating the lifetime of ACA joint failure. And then cumulative failure distributions were used to predict the lifetime of ACAs flip chip joint under high current stressing.

3. Results

3.1 Current stressed failure analysis

Fig. 2 shows a typical curve of current carrying capability of a pair of Au stud bumps joint with increasing voltage. At the low bias, measured current is linealy increased with increasing bias. However, current through stud bumps joint becomes saturated, and then start decreasing at higher voltages due to joint degradation followed by failure. Although measured current decreases after the saturation, the current density per unit area of bump joint is kept constant.

From Fig. 2, it was found that the maximum allowable current through a pair of stud bumps joint was about 4A.

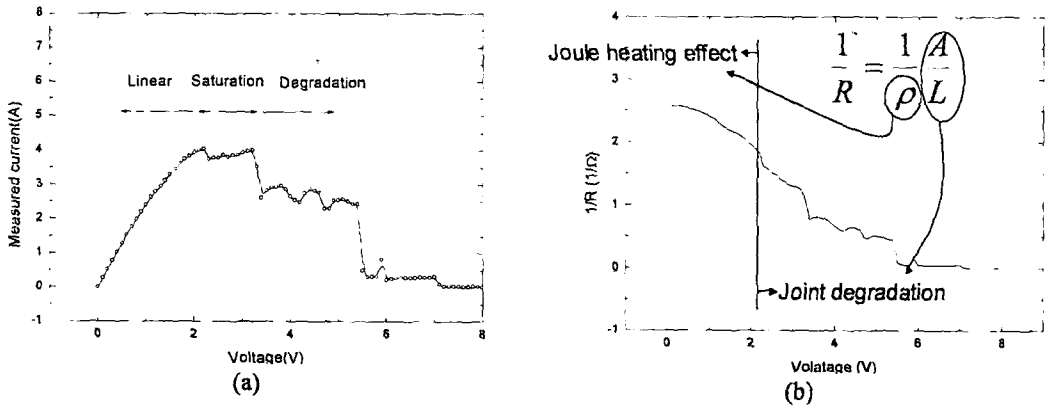


Fig. 2. A measured curve of current carrying capability of Au stud bump joint with applying bias voltage

Below the maximum current, current stressing were applied to stud bumps joint. Fig. 3 (a) shows resistance change (ΔR/R) of joint under constant current stress of 3.7A. In all of resistance change vs. time curves, there are always three resistance increase steps. However, the only difference in resistance change vs. time curves under different current stress is the TTF.

Initial resistance increase is due to junction temperature rise between a Si chip and a PCB. As shown in Fig. 3 (b), junction temperature is increased and then saturated within 20 min. This resistivity increase is related with acoustic lattice scattering [4]. For a metal, resistivity is increased at high temperature where scattering by acoustic lattice waves is dominant.

Intermediate resistance increase in Fig. 3 (a) is presumably due to intermetallic compound formation and Al-depletion as shown in Fig. 4.

Fig 4. shows SEM photographs of stud bumps joint under current stress of 3.7A for 150min before failure (Intermediate

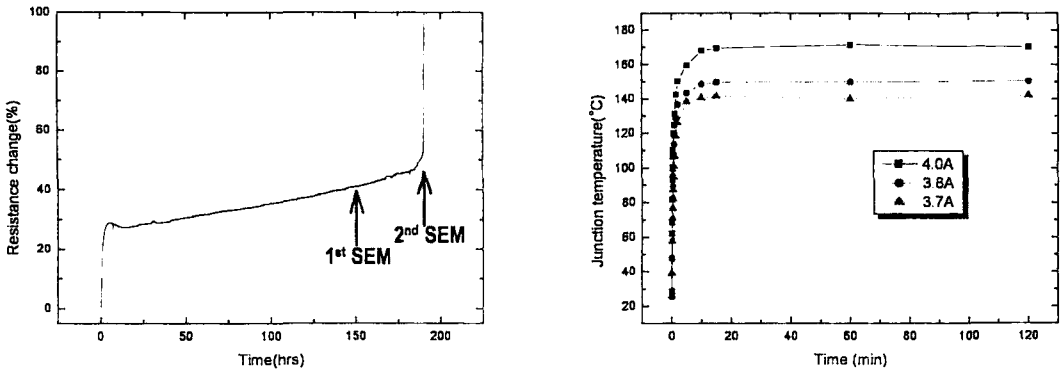


Fig. 3. (a) Resistance change, (b) temperature change vs. time curve of stud bumps joint under current stress

R-increase). After 150min current stress, Al_2Au_5 intermetallics compound formation and Al-depletion between Al pad and stud bump were observed. Especially, colse to the bond pad, the high current density causes Al-depletion presumably due to a net Al-flow away from the bond pad. However, there is no influence of the current direction on Al_2Au_5 intermetallics compound formation and Al-depletion. Al_2Au_5 intermetallic compound of lower conductivity is formed due to annealing effect by the Joule heating. And effective contact surface area is reduced due to Al-depletion. Because of these reasons, joint resistance increases confirmly during intermediate current stressing time.

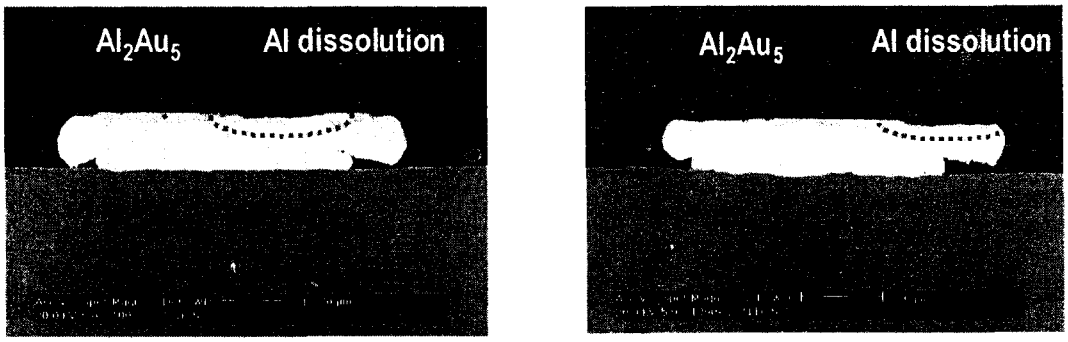


Fig. 4. BS-SEM photographs of stud bumps joint at 1st current stress step (1st SEM, intermediate resistance increase)

Fig. 5 shows SEM photographs of stud bumps joint after final failure (100% resistance increase). As shown in Fig.5, a large portion of aluminum pad was depleted and crack was formed between Au-rich intermetallic compound and stud bumps. That is, during current stressing, sudden resistance increase may occur at the joint, possibly due to significant Al-depletion and crack formation.

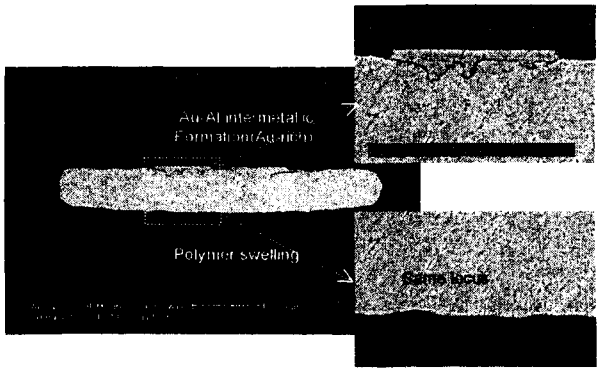


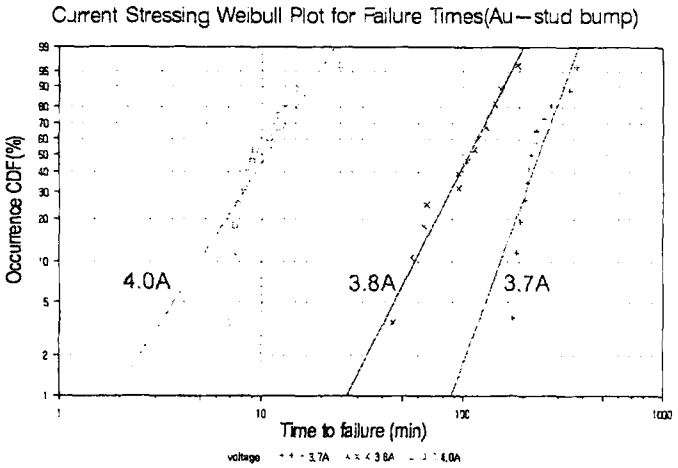
Fig. 5. BS-SEM photographs of stud bumps joint at 2nd current stress step (2nd SEM, sudden R-increase)

The other cause of resistance increase with adhesive joint may be the bottom interface delamination due to adhesive creep as shown in Fig. 5. Both bottom surface of stud bumps and top surface of Cu/Ni trace on PCB have the same interface trace and 45° shear direction. This could be presumably due to thermally induced shear motion of component and visco-plastic deformation of the adhesive.

3.2 Lifetime prediction

Al-Au intermetallic compound formation and delamination of adhesives are time and temperature dependent. So, for each current stress condition, there are two possible reasons for the current and temperature dependence of the failure time.

Fig.6 shows a time to failure (TTF) plot as a function of current stressing. As shown in Fig. 6, the time to first failure is a particularly strong function of stress current. When 4A stress current is compared with 3.7A stress current for lifetime prediction, it will be clear that different degradation rate determines the lifetime of stud bumps joint. At high current density, intermetallic formation and Al-depletion due to electromigration are faster than at low current density.



Stress current	Parameter	Estimate
4.0A	MTTF(min)	12.28
	n	2.45
3.8A	MTTF(min)	120.91
	n	3.03
3.7A	MTTF(min)	261.78
	n	4.20

Fig. 6. Time to failure distribution as a function of current stressing for stud bumps joint

Since stress current should be associated with temperature and electron flow, important factors such as Al depletion, crack formation and adhesive creep dominate the the lifetime of stud bumps joint under different stress condition.

The distribution parameters (n, MTTF) of Weibull distribution function under different sress current can be estimated as shown in the above table.

The time to failure of each condition are plotted as a function of current and temperature in Fig. 7 (a), (b). It is found out that the lifetime of stud bumps flip chip joint strongly depends on the stress current.

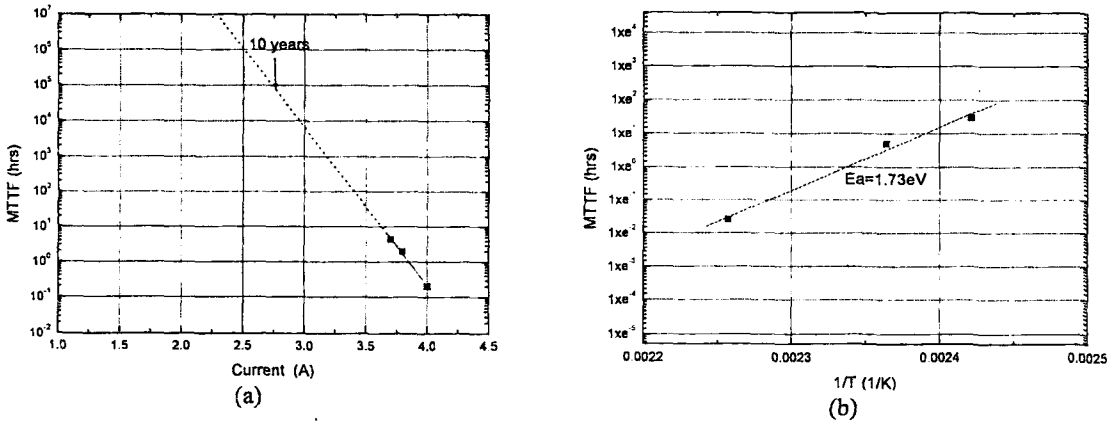


Fig. 7. (a) Current dependence, (b) Temperature dependence of the MTTF for a failure criterion 100% resistance increase

From [5], we learn that in the absence of a stress current the degradation mechanism at elevated temperature is as follows: initially the layer of Au-Al compound grows thicker until it has reached the bottom of the Al-layer. This explains the parabolic

behavior with time. Then, it changes gradually into a more drastic behavior caused by the formation of the Kirkendall voids and cracks propagation in the Al-layer. In contrast, a stress current is applied to stud bumps ACF flip chip joint, the followings are observed:

- Au-Al compound formation due to joule heating
- Al depletion due to electromigration
- Crack formation between Au-Al compound and stud bumps
- Adhesive delamination due to visco-plastic deformation

From the Fig. 7 (a), the lifetime was predicted more than 10 years under the current being 2.75A/pair of stud bumps.

The activation energy depends on the failure mechanism that causes the end of life. When different degradation mechanisms are combined, each with their own activation energy, the extraction of E_a must be done very carefully because the result may depend on the failure criterion that is used. It has already been shown that 100% resistance increase failure criterion is reasonable for the extraction of E_a [5].

Fig. 7 (b) shows time to failure dependence of junction temperature. Due to current induced Joule heating, junction temperatures are different.

4. Conclusions

The current handling capability and degradation mechanism of stud bumps flip chip joint were investigated. The degradation mechanism was consisting of many steps, which were Au-Al compound formed, Al pad depleted, crack formed and adhesive visco-plastic deformed The lifetime of stud bumps flip chip joint under different stress current was estimated. It was found out that the lifetime of stud bumps joint strongly depends on the stress current related with temperature and electron flow. The lifetime was predicted more than 10 years at 2.75A/pair of stud bumps.

Acknowledgments

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