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An Analysis of Optimal Link Voltage of VS-SVPWM for Current Harmonics Reduction

Dong-Hee, Lee*, Han-Woong, Park**, Jin-Woo, Ahn***, Young-Ahn, Kwon****
*Koje College, **Korea Naval Academy, ***Kyungsung Univ., ****Pusan National Univ.

ABSTRACT

In recent, complex SVPWM (Space Vector PWM) algorithm can be easily implemented by high performance microprocessor and DSP. Various SVPWM techniques are widely studied due to the advantages of low harmonic distortion and high use ratio of D.C. link voltage.

Most of various studies for improving of VS-PWM inverter performance are concentrated about switching pattern and zero pulse pattern split algorithms. However, dc link voltage that is determined at rated load and speed conditions is not proper in the low speed and under rated load.

In this paper, analysis of current ripple with digitally implemented SVPWM inverter is introduced according to link voltage. The optimal link voltage in the designed inverter system and load condition is provided in order to suppress output voltage error and current ripple. As remaining the effective voltage vector interval per sampling period sufficiently, additional voltage error and current ripple are suppressed. The proposed algorithm is verified through digital simulation and experimental results.

1. INSTRUCTIONS

VS-PWM(VS-Pulse Width Modulation) method are much used in the industrial applications such as variable speed AC motor drives. For the excellent control performance of industrial machines with AC motors, the use of high performance PWM inverter is essential. Due to ability of output voltage and frequency control and low harmonic distortion, PWM method is widely used in the motor control and factory automation[1-2]. In recent, complex SVPWM (Space Vector PWM) algorithm can be easily implemented by high performance microprocessor and DSP. Various SVPWM techniques are widely studied due to the advantages of low harmonic distortion and high use ratio of D.C. link voltage[3-5].

Most of various studies for improving of VS-PWM inverter performance are concentrated about switching pattern and zero pulse pattern split algorithms[6]. However, dc link voltage that is determined at rated load and speed conditions is not proper in the low speed and under rated load.

Current ripple does not only depend on the performance of the PWM, but in addition on the internal load impedance and back EMF. Especially, low speed and under rated load condition rated dc link voltage pulse produces serious current harmonics. The ripple and harmonic currents basically determine the copper losses of the machine and produce additional torque harmonics.

In this paper, analysis of current ripple with digitally implemented SVPWM inverter is introduced according to link voltage. The optimal link voltage in the designed inverter system and load condition is provided for suppress output voltage error and current ripple. As remaining the effective voltage vector interval per sampling period sufficiently, additional voltage error and current ripple can be suppressed. The proposed algorithm is verified through digital simulation and experimental results

2. ANALYSIS of VS-SVPWM INVERTER

PWM techniques have the advantages of low harmonic distortion and high use ratio of dc link voltage. The reference voltage is explained as a vector on the space voltage vector diagram. The output voltage of inverter can be determined by the

summation of zero and effective voltage vectors. From the structure of 3-phase inverter, six effective and two zero voltage vectors are possible. Two zero vectors have the state of all turn-on of the upper power switches or turn-off the lower power switches. Hence during two zero vector, voltage doesn't apply to the load. Six effective voltage vector can supply power to the load such as Fig. 2. For example, Applying of six effective voltage vector to the ac machine step by step, rotating voltage is obtained.

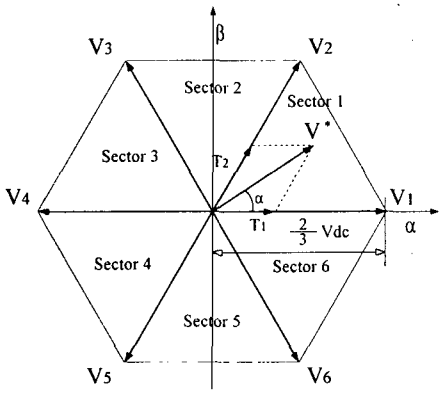


Fig. 1 Space voltage vector of 3-phase inverter

The effective voltage vector can be obtained as follows.

$$\int_0^{T_S} V^* dt = \int_0^{T_1} V_n dt + \int_{T_1}^{T_1+T_2} V_{n+1} dt + \int_{T_1+T_2}^{T_S} V_o dt \quad (1)$$

where, T_S : sampling period

T_1, T_2 : durations of effective voltage vector

V_n, V_{n+1}, V_o : effective and zero voltage vector

In a sampling period, the reference voltage vector is obtained by the average of effective and zero voltage vectors.

Assuming of 3-phase symmetry and ignoring of nonlinear characteristics of inverter drive, The reference voltage of each phase can be derived as follows.

$$V_{MAX}^* = \frac{2}{3} V_{dc} \frac{T_1}{T_S} + \frac{1}{3} V_{dc} \frac{T_2}{T_S} \quad (2)$$

$$V_{MID}^* = -\frac{1}{3} V_{dc} \frac{T_1}{T_S} + \frac{1}{3} V_{dc} \frac{T_2}{T_S} \quad (3)$$

$$V_{MIN}^* = -\frac{1}{3} V_{dc} \frac{T_1}{T_S} - \frac{2}{3} V_{dc} \frac{T_2}{T_S} \quad (4)$$

$$V_{MAX}^* + V_{MID}^* + V_{MIN}^* = 0 \quad (5)$$

where, V_{MAX}^*, V_{MID}^*, V_{MIN}^* mean the sorted phase reference voltage by magnitude. Using (2)-(5), SVPWM algorithm can be easily implemented with a simple sorting of reference voltages.

3. ANALYSIS of CURRENT RIPPLE and OPTIMAL LINK VOLTAGE

The current harmonics and ripple due to the high frequency switching produces additional loss and reduces the control performance. In some applications, additional low pass filter is used for reduction of current ripple. Fig. 2 shows the current and voltage shapes of V_{MAX}^* phase applied by VSI.

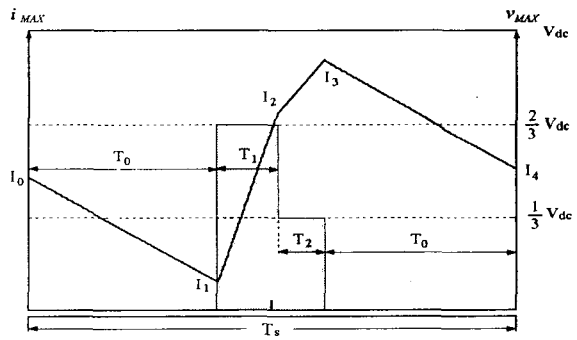


Fig. 2 Switching voltage and current in a sampling period

The shadow area denotes the actual effective voltage of V_{MAX}^* phase from the PWM switching pattern. The load current changes according to applied voltage and system impedance. The peak values of load current at each the switching instance are expressed as follows.

$$I_1 = \frac{(V_0 - e_{MAX})}{R_a} \cdot (1 - e^{-T_0/\tau}) + I_0 e^{-T_0/\tau} \quad (6)$$

$$I_2 = \frac{(V_1 - e_{MAX})}{R_a} \cdot (1 - e^{-T_1/\tau}) + I_1 e^{-T_1/\tau} \quad (7)$$

$$I_3 = \frac{(V_2 - e_{MAX})}{R_a} \cdot (1 - e^{-T_2/\tau}) + I_2 e^{-T_2/\tau} \quad (8)$$

$$I_4 = \frac{(V_0 - e_{MAX})}{R_a} \cdot (1 - e^{-T_0/\tau}) + I_3 e^{-T_0/\tau} \quad (9)$$

Where, I_0 denotes the initial value of load current at the starting point of sampling period. V_0, V_1 and V_2 are the zero voltage and effective voltage vectors of V_{MAX}^* phase respectively. e_{MAX} is the back e.m.f. of the same phase. The τ is load time-constant, that is $\tau = L_s/R_a$. Because back e.m.f. of each phase depends on the electromagnetic parameters of the AC machines and speed, the ripple of load current is unproportional to the interval of zero voltage vector. The interval of zero voltage vector T_0 increases with reduction of V_{ref}^*/V_{dc} in the fixed sampling period. This phenomena is general operating condition in low reference voltage with high link voltage. The reference voltage was determined by control condition and obtained by (1). The ripple of load current can be minimized at the condition of non zero voltage vector. The optimal link voltage for minimum current ripple can be obtain as following conditions.

$$T_1 + T_2 = T_S \quad (10)$$

$$V_{dc\ optimal} = V_{MAX}^* - V_{MIN}^* \quad (11)$$

4. DIGITAL SIMULATION RESULTS

The proposed optimal link voltage was simulated with Y-connected 3-phase R-L load. Fig. 3 shows load current waveform and current ripple in the stationary reference frame. In the simulation, fixed link voltage for rated power was set by 300[V] and optimal link voltage was determined by the load conditions. A 10 [Ω]-30[mH] load and 50[Hz] reference frequency f_{ref}^* was used in the Fig. 3.

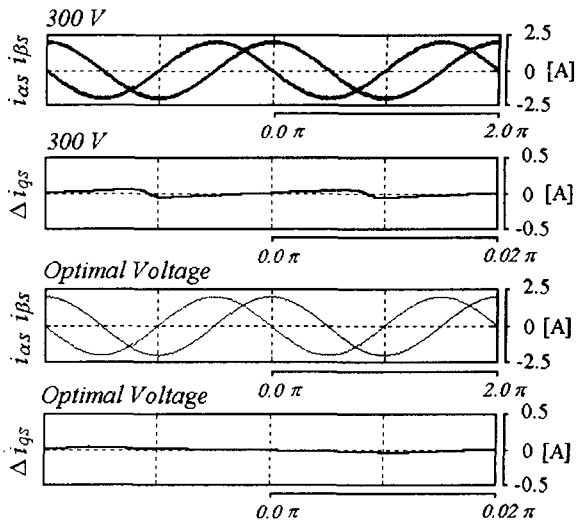


Fig. 3 Simulation of current ripple in case of R-L load(10[Ω]-30[mH])

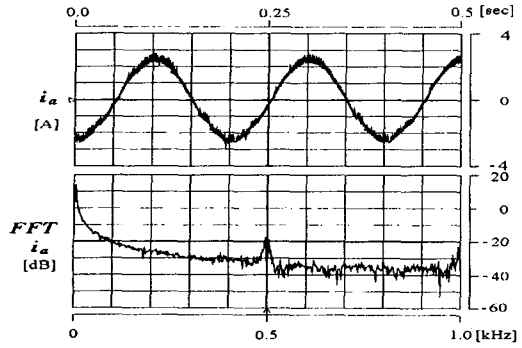
From the simulation results, optimal link voltage for current ripple minimization can be determined by the load condition. A fixed high link voltage produces large current ripple in the load condition. Higher current harmonics can be the additional source of torque and speed ripple in addition increasing of copper loss.

5. EXPERIMENTAL RESULTS

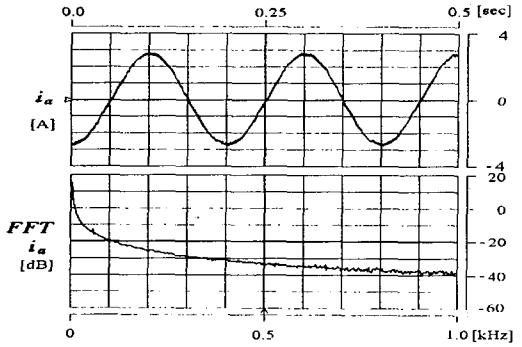
The proposed optimal link voltage for current ripple reduction was verified through SVPWM inverter with R-L load. The 10[Ω] - 30[mH] impedance, R-L load has Y-connected as load system.

Fig. 4 and 5 show load currents and their FFT analysis as experimental results. With the fixed rated link voltage, load currents have much harmonic and less fundamental component than applied reference at under rated condition such as Fig 4(a) and 5(a).

Hard switching of higher link voltage introduces more current ripple. Additional voltage error and dead-time effect are more serious in those cases. With the optimal link voltage determined at certain load condition, current ripple of the load can be reduced shown as Fig 4(b) and 5(b).

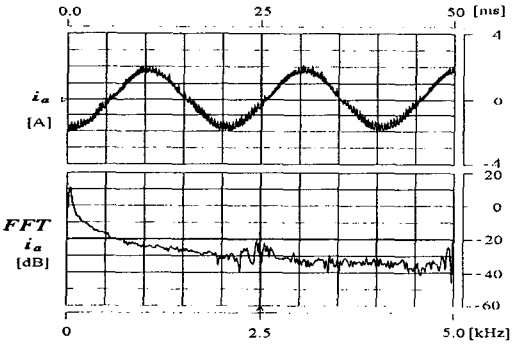


(a) In case of V_{dc} = 300[V]

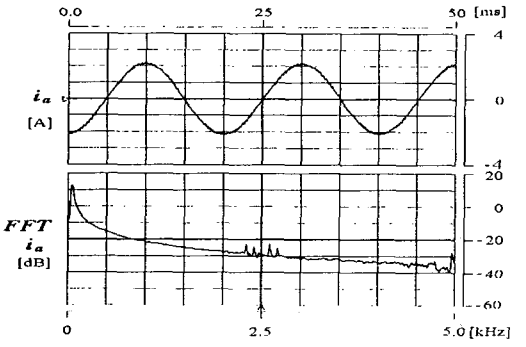


(b) In case of optimal link voltage

Fig. 4 Load current and FFT analysis
(V_{peak}^* = 30[V], f_{ref}^* = 5[Hz])



(a) In case of V_{dc} = 300[V]



(b) In case of optimal link voltage

Fig. 5 Load current and FFT analysis
(V_{peak}^* = 50[V], f_{ref}^* = 5[Hz])

In addition, voltage error due to the inverter resolution and dead-time effect can be reduced. The FFT analysis results show that fundamental component error of the load current between actual and reference is likely to be zero.

6. CONCLUSIONS

PWM inverter is widely used in the industrial applications. For the high efficiency and control performance, current ripple of inverter has to be minimized.

In this paper, the optimal link voltage for load current ripple minimization was analyzed. According to the reference voltage, the optimal link voltage for the load current ripple minimization can be determined. The actual reference voltage depends on the load and control commands. The optimal link voltage can be obtained at each load and control conditions in instant sampling period in order to minimize current ripple.

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